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F.Celani, M.Baffa, S.Catà, R.Falcioni and S.Pace:  
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D.C. AND LOW FREQUENCY CHARACTERIZATION OF HIGH  
IMPEDANCE TUNNEL JUNCTIONS

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**A SIMPLE, LOW NOISE, TRUE INSTRUMENTATION AMPLIFIER FOR D.C. AND LOW FREQUENCY  
CHARACTERIZATION OF HIGH IMPEDANCE TUNNEL JUNCTIONS**

F. Celani, M. Baffa, S. Catà, R. Falcioni  
INFN - Laboratori Nazionali di Frascati, 00044 Frascati, Italy

and

S. Pace<sup>(\*)</sup>  
Dipartimento di Fisica dell'Università di Salerno, 84100 Salerno, Italy

ABSTRACT

It has been developed a composite Fet-input True Instrumentation Amplifier (TIA) based upon a new type of monolithic high performance operational amplifier (OPA 111 BM). The operating feature and the main drawbacks of the TIA configuration are discussed in some details, particularly in the case of a low leakage fet-input front-end (few pA in all the operating range). It has been underlined the importance of very low values of input currents to minimize the total output noise for large values ( $R_g > 10 \text{ K}\Omega$ ) of input source resistance like that involved in high impedance tunnel junction. The circuit can be betterly operated and  $\bar{2}$  independent TIA are housed in an unity-width standard NIM module.

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1.- INTRODUCTION

We have experimentally studied Nb/Pb junctions for the final purpose of using superconducting tunnel junctions as ionizing particle detectors (SCODET experiment of INFN, Italy) with an expected energy resolution about 30 times better than that presently allowable with semiconductor detectors<sup>1)</sup>.

If the Josephson current can be neglected, tunnel junctions can be modeled by the equivalent circuit shown in Fig. 1<sup>2)</sup>. These junctions show a rather high

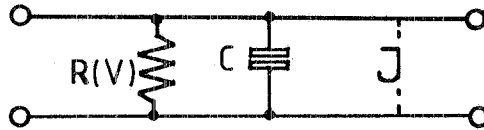


Fig. 1 - Equivalent circuit of superconducting tunnel junctions.

capacitance ( $C \approx 30 \mu F/cm^2$ ), and a non-linear resistance  $R(V)$ . For voltages lower than the sum of gap voltages  $e(\Delta_1 + \Delta_2)$  of the two superconducting electrodes, the voltage dependence of  $R(V)$  is determined, at low temperature, by the density of states of the two superconducting materials (Fig. 2a). At larger voltages, at any temperature,  $R(V)$  is determined by the tunnel barrier (Fig. 2b)<sup>3)</sup>. The value of  $R(V)$  in the normal state at few mV ( $R_{NN}$ ) is proportional to the single electron tunnel probability, and it increases as the temperature decreases.

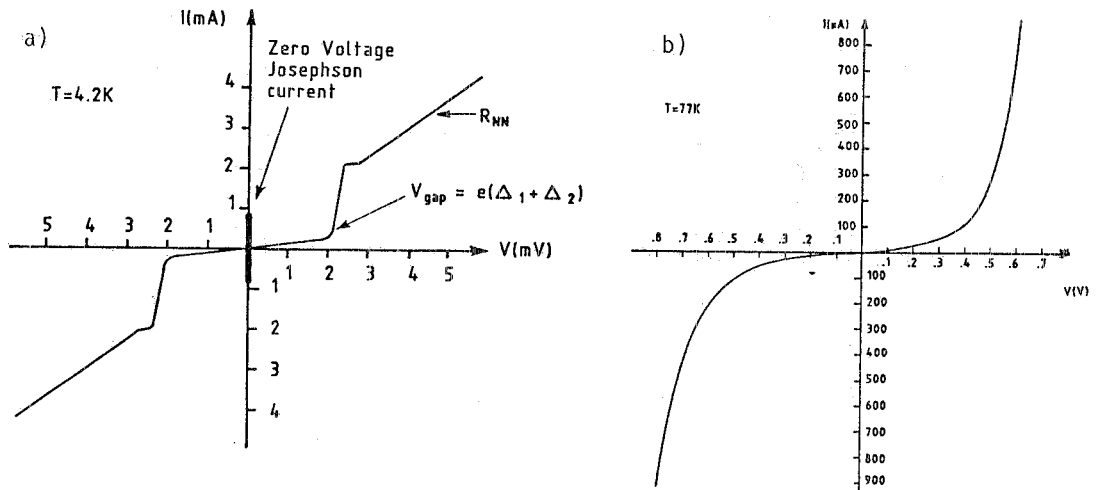


Fig. 2 - a) Low voltage d.c. I-V characteristic of a Nb/Pb Josephson tunnel junction. b) d.c. I-V characteristic of a Nb/Pb high resistance normal tunnel junction.

In order to study:

- a) the details of the tunnel barrier<sup>4)</sup>,
- b) the output noise from the detector-amplifier system,
- c) the possible excess noise generated by the tunnel barrier,

we have varied the junction impedance in a rather wide range of capacitance and resistance ( $R_{NN}$ ) by changing both the junction area and the parameters of the oxidation process of the first electrode (i.e. the tunnel barrier) usually used at the Physics Department of the University of Salerno.

In particular, in some cases, junctions having high values of  $R_{NN}$  at room as well as at the cryogenic temperature have been studied<sup>3)</sup>. Usually the analysis of the current-voltage (I-V) characteristic is performed in D.C. or at very low frequency (0.01-100 Hz) in the "four contact" configuration to avoid effects generated by spurious resistances of the contacts (Fig. 3). The junctions are usu

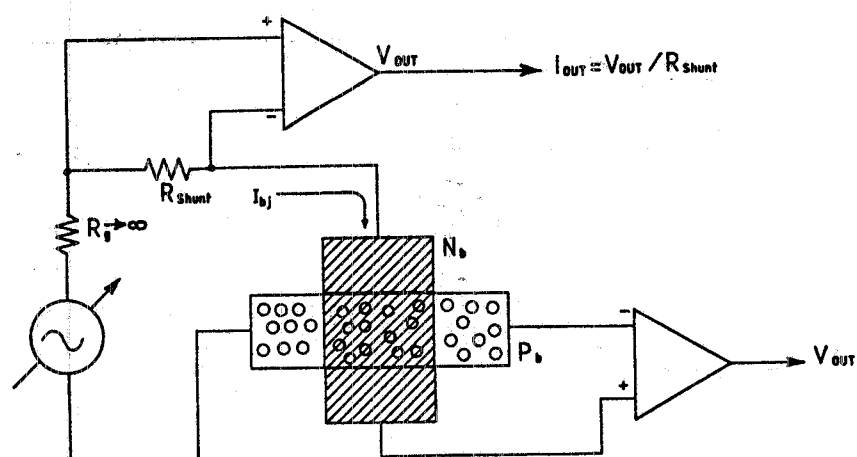


Fig. 3 - Sketch of the experimental set-up for the analysis of the I-V characteristic of tunnel junctions in the 4 contacts configuration.

ally biased at a constant current  $I_{bj}$  and voltages are measured by differential amplifiers. These amplifiers are in single (Fig. 4) or three Operational Amplifier configuration. In the latter case they are connected in the True Instrumentation Amplifier (TIA) configuration (Fig. 5).

For the requested measurement accuracy, in the low resistivity junctions one can neglect the input currents of the voltage amplifiers. In the case of TIA amplifiers (Fig. 5) these currents are just the input bias currents of BJT transistors usually used in input sections. On the contrary, in the case of the single amplifier configuration the main contributions to input currents ( $I_{i1}$ ,  $I_{i2}$ ) are the currents circulating in networks R2-R4 and R1-R3 (Fig. 4); moreover both

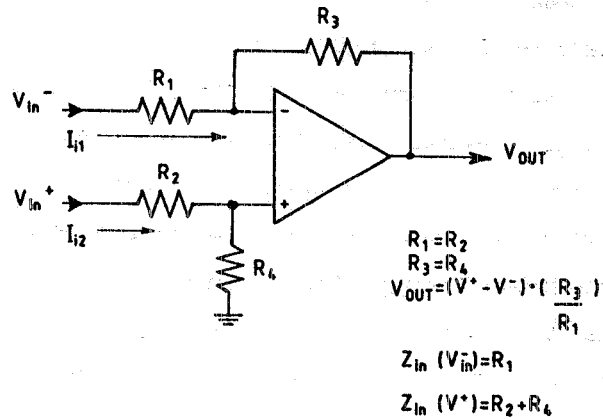


Fig. 4 - Differential amplifier in the single O.A. configuration.

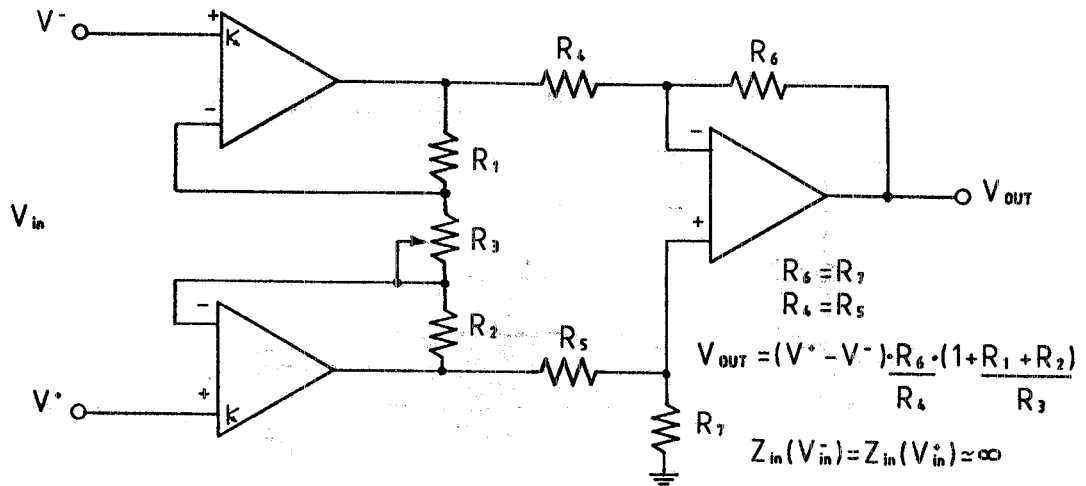


Fig. 5 - True instrumentation amplifier in the 3 O.A. configuration.

the input impedances and input currents of inverting and noninverting inputs are different. For these reasons we have optimized, for our purpose, the TIA configuration.

In our experimental conditions, at low temperatures, the maximum dynamic resistance  $dV/dI$  of some high resistance junctions can be up to 1 Mohm so that the resulting  $I_{bj}$  value can be particularly low (10 pA- 1  $\mu$ A). In this way, the study of these junctions requires the following cares:

- a) current errors should be avoided to measure the I-V characteristics with good resolution and absolute accuracy;
- b) even though resistances as large as 1 Mohm are used to measure  $I_{bj}$ , the  $S/\Delta$

ratio has to be kept high and then the input current noise of the amplifier ( $i_n$ ) has to be kept low.

Moreover, in some cases, the I-V characteristic of the junction can change by applying, at room temperature, few tenths of mV for rather long times (tens of minutes) or larger voltages (500 mV) for shorter times (10  $\mu$ sec). Then, we must avoid biasing high resistance junctions for long times with the spurious input bias current of amplifiers and also decouple junctions against external sources of spikes<sup>5</sup>).

For these reasons we have used a TIA configuration with a FET as front-end input. In this case the input bias currents are very low and determined only by the JFET gate leakage current.

## 2.- OPERATION, ERROR SOURCES AND NOISE OF A TIA

We recall some elementary considerations for both ideal and real TIA and its internal components, as pointed out with great details in ref.6).

### 2.1.- Ideal TIA

An instrumentation amplifier is a closed-loop, differential input gain block. The properties of the ideal TIA may be summarized as:

- a) infinite input impedance;
- b) zero output impedance;
- c) output voltage  $V_{od}$  equal to the product of the amplifier differential gain ( $A_d$ ) and the difference between input voltages (Fig. 6):

$$V_{od} = A_d \cdot V_{id} \quad \text{with } V_{id} = V_2 - V_1 ; \quad (1)$$

- d) a precisely known constant gain implying linear response;
- e) unlimited bandwidth.

This amplifier would completely reject signal components common to both inputs, and would exhibit no D.C. offset voltage or drift.

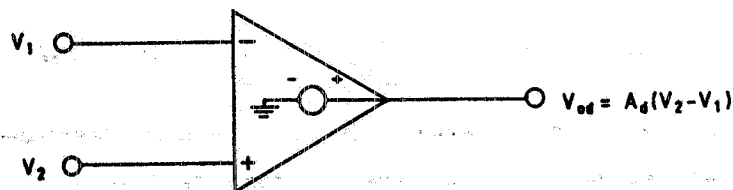


Fig. 6 - Idealized model of an instrumentation amplifier.

2.2.- Real TIA

A simple model of realistic instrumentation amplifier is shown in Fig. 7.

Its main drawbacks are:

2.2.1.- Finite Input Impedance ( $Z_{icm}$ ,  $Z_{id}$ )

The common mode impedance  $Z_{icm}$  is the ratio between the common mode voltage and the total input currents and it is represented as two equal components  $2Z_{icm}$  from each input to ground.

The differential input impedance ( $Z_{id}$ ) is the apparent impedance between the two input terminals and it is a function of  $Z^*$  and  $Z_{icm}$  (Fig. 7).

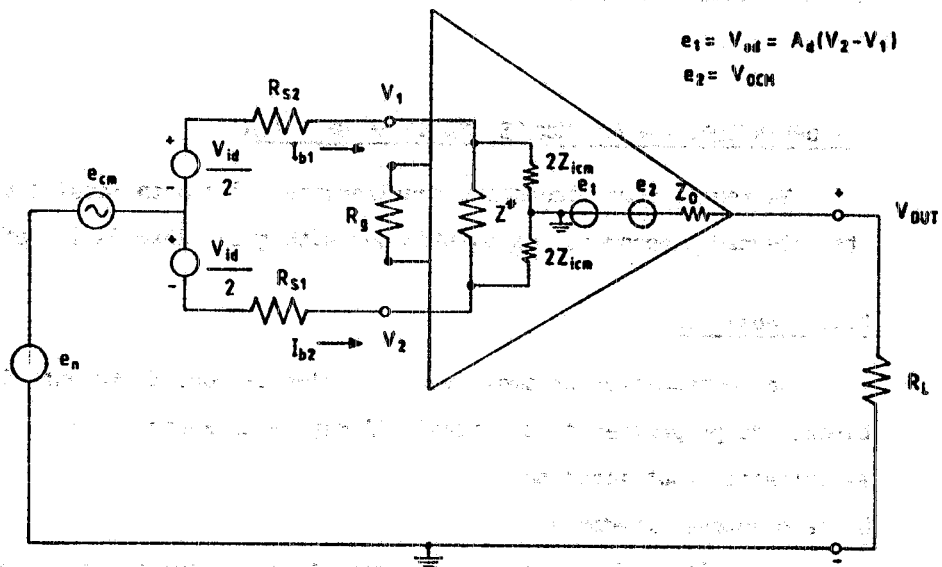


Fig. 7 - Simple model of a real instrumentation amplifier.

2.2.2.- Gain errors

The instrumentation amplifier provides a load  $Z_{id}$  on the source. The load leads to a gain error which is the difference between the actual gain and the gain predicted for an infinite input impedance amplifier. If the total source impedance is  $R_S = R_{S1} + R_{S2}$ , the gain error caused by this loading is:

$$\text{Gain error} = 1 + \frac{Z_{id}}{Z_{id} + R_S} \approx \frac{R_S}{Z_{id}} \quad \text{if } Z_{id} \gg R_S \quad (2)$$

The D.C. common input impedance  $Z_{icm}$  will be gain independent. The D.C. differential input impedance  $Z_{id}$  may vary as a function of gain. The nonzero output impedance of the amplifier will also create a gain error, whose value depends on the load resistance ( $R_L$ ).

In most cases the gain linearity is more important than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. Moreover, in some cases, for high source resistances  $R_S$  the gain error can be significant if the value of  $R_S$  shows large variations. The nonlinearity is usually specified to be the maximum deviation from a "best fit" straight line (curve fitting on input-output graph), expressed as a percent of peak-to-peak full scale output.

### 2.2.3.- Finite Rejection of Common Voltages (CMRR)

As illustrated in Fig. 7, the output voltage  $V_O$  has two components:

$$V_O = V_{od} + V_{ocm} \quad (3)$$

The second component  $V_{ocm}$  is proportional to the common mode input voltage  $E_{cm} = (e_2 + e_1)/2$ , and it is equal to:

$$V_{ocm} = E_{cm} \cdot A_{cm} \quad (4)$$

where  $A_{cm}$  is the common mode gain.  $E_{cm}$  may consist of some common-mode voltage in the sources  $e_{zm}$ , plus any noise voltage,  $e_n$ , between the common source and the reference voltage point of the signal source-amplifier system.

The Common Mode Rejection Ratio (CMRR) is the ratio of differential gain to common-mode gain:  $CMRR = A_d/A_{cm}$ . Thus CMRR increases as differential gain  $A_d$  increases. Hence, CMRR is usually specified for maximum and minimum gain values of the amplifier. For a realistic instrumentation amplifier the CMRR, though very high, is still not infinite and so it will cause an error voltage  $(E_{cm}/CMRR) \times A_d$  to appear at the output.

### 2.2.4.- Error due to Source Imbalance ( $E_{si}$ )

If the source impedances ( $R_{S1}$ ,  $R_{S2}$ ) are different, the common mode source voltages ( $e_{cm} + e_n$ ) are unequally divided between  $R_{S1}$  ( $R_{S2}$ ) and the input impedance of differential inputs. Then a differential signal (error due to source imbalance,  $E_{si}$ ) is developed at the amplifier's input. This error signal cannot be separated from the desired signal.

### 2.2.5.- Offset Voltages ( $V_{off}$ )

Most instrumentation amplifiers are two stage devices. They have a variable gain ( $G_1$ ) input stage and a fixed gain ( $G_2$ ) output stage. If  $V_{off1}$  and  $V_{off2}$  are the input offset voltages of input and output stages respectively, then the input offset voltage ( $V_{off}$ ) of the TIA (Voltage Referred to Input, RTI) is equal to:

$$V_{off} = V_{off1} + V_{off2}/G_1$$



The initially offset voltage is usually adjustable to zero and therefore, the existence of a temperature-dependent voltage drift is the more effective source of errors since it cannot be nulled. The offset voltage drift also has two components. One due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage is the dominant term of the total drift; at low values of gain, the drift of the output stage will be the main component of drift due to usual larger values of power consumption generated by the load  $R_L$ . When the total output drift is referred to the input, the effective input voltage drift is larger for low values of gain. The absolute value of output voltage drift will always be lower at low gains.

#### 2.2.6.- Error due to input offset current ( $E_{co}$ )

The input offset current ( $I_{os}$ ) is the difference between the two bias currents ( $I_{os} = I_{b1} - I_{b2}$ ), respectively  $I_{b1}$  and  $I_{b2}$ . The bias currents flowing into the source resistances will generate offset voltages of  $E_{os2} = I_{b2} \times R_{s2}$  and  $E_{os1} = I_{b1} \times R_{s1}$ . If  $R_{s1} = R_{s2} = R_s/2$  the offset voltage at the input is:  $E_{co} = E_{os2} - E_{os1} = I_{os} \times R_s/2$ . These offset errors referred to the input are usually of the same order of magnitude as the input offset voltages when BJT are used in the inputs.

#### 2.3.- Noise

As far as noise is concerned we recall the following:

- a) The minimum total voltage noise for an unity bandwidth of one O.A. connected in the configuration of unity-gain voltage amplifier (Fig. 8a), is:

$$E_n = \sqrt{e_n^2 + (i_n R_s)^2 + 4KTR_s} \quad (5)$$

where  $e_n$  and  $i_n$  are the usual "intrinsic" voltage and current noise of the active device while  $R_s$  is the absolute resistance value of signal source.

- b) The general expression of the output total noise of an O.A. connected in the non-inverting voltage amplifier configuration (Fig. 8b)<sup>7)</sup> is:

$$E_o = \sqrt{4KTR_{IN} \left(\frac{R_F}{R_{IN}}\right)^2 + 4TR_S \left(\frac{R_F}{R_{IN}} + 1\right)^2 + 4KTR_F + (i_n R_F)^2 + \left[ i_n^2 R_S \left(\frac{R_F}{R_{IN}} + 1\right) \right]^2 + \left[ e_n \left(\frac{R_F}{R_{IN}} + 1\right) \right]^2} \quad (6)$$

- c) The value of  $i_n$  is related to the absolute value of  $I_{bias}$  ( $I_b$ ) of the O.A. according to the well known relation of the shot noise of any active device:

$$i_n = \sqrt{2qI_b} \quad (7)$$

The total output noise of a TIA is generally dominated by the noise of the two O.A. in the first stage. Each O.A. is almost equivalent to the circuit shown in Fig. 8b, so that it contributes with a term given by eq.(6). Moreover, in such configuration, it is possible to minimize the noise contributions due to  $R_F$  and  $R_{IN}$  by a careful selection of proper devices and their operating point. Practi-

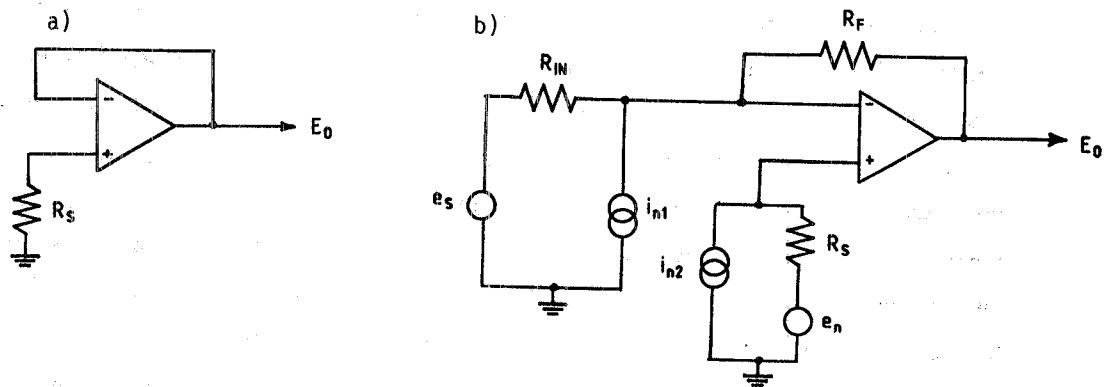


Fig. 8 - a) Noise analysis, unity-gain voltage amplifier configuration. b) Noise analysis, equivalent noise sources of the non-inverting voltage amplifier configuration.

cally, it is necessary to reduce as much as possible the absolute values of  $R_{IN}$  and  $R_F$  to minimize their Johnson noise (terms 1 and 3 of eq.(6)), and to keep low enough the value of  $i_n$  (terms 4 and 5 of eq.(6)). In such a case, with the conditions:  $R_{IN} < R_S$ ,  $R_{IN} < R_F$ ,  $i_{n1} = i_{n2} = i_n$ , the noise expression of eq.(5) is accurate enough for most applications, especially when the input stage is JFET type, so that it is possible to neglect  $i_n R_F$ .

### 3.- CIRCUIT DESCRIPTION AND PERFORMANCES

We have chosen the TIA configuration because it is the best one from the point of view of input loading and versatility. As shown in Fig. 5 the differential gain is equal to:

$$A_D = \frac{R_6}{R_4} \left( 1 + \frac{R_1 + R_2}{R_3} \right) \quad (8)$$

so that it is possible to change the gain continuously just by turning the potentiometer  $R_3$ . Moreover, we used as front-end operational amplifiers with FET input to improve the performances related to the value of input bias current.

According to eqs. (5) and (7), for studying high resistance junctions it is necessary to minimize the noise term  $i_n R_s$ , then we consider only the devices with  $I_{bias} < 50$  pA in all the operating ranges. The main drawback of a monolithic or even a hybrid FET input O.A. is the large value of input voltage noise ( $e_n$ ), particularly at low frequency (1/f excess noise). Commercially available monolithic Bifet technology LF 156 O.A. has an  $e_n$  of  $50$  nV/ $\sqrt{\text{Hz}}$  at a central frequency  $f_0 = 10$  Hz and of  $12$  nV/ $\sqrt{\text{Hz}}$  at 1 kHz. At the same frequency the hybrid "high performance" LH 0022 has noise values as high as respectively  $80$  nV/ $\sqrt{\text{Hz}}$  and  $20$  nV/ $\sqrt{\text{Hz}}$ . Luckily, since about 1 year, a new type of monolithic O.A. (mod. OPA 111 BM)<sup>8)</sup> is commercially available at a reasonable cost (about 30 US\$) from BURR BROWN Company. This O.A. has a Difet input (Fet with Dioxide isolation) with an extremely low bias current (less than 1 pA in "normal" operating conditions) and a guaranteed enough low value of voltage noise ( $30$  nV/ $\sqrt{\text{Hz}}$  at 10 Hz and  $7$  nV/ $\sqrt{\text{Hz}}$  at 1 kHz); moreover, it is specified its value at 1 Hz (less than  $100$  nV/ $\sqrt{\text{Hz}}$ ). Its input current noise density ( $i_n$ ) is very low and has a value of just  $0.4$  fA/ $\sqrt{\text{Hz}}$  from 0.1 Hz to 20 kHz; it reaches a value of  $10$  fA/ $\sqrt{\text{Hz}}$  at 1 MHz (the unity gain roll-off is at a frequency of 2 MHz). Another advantage of this device, when used as instrumentation amplifier, is a value of the input bias current almost constant (practically less than 3 pA) for variations of both common mode voltage ( $\pm 10$  V) and ambient temperature from 0 C to 50 C. Such a low value of current noise allows us to use large values of source resistance without a dramatic increase of total noise as is usual for bipolar input O.A. (Fig. 9).

The details of the TIA circuitry are shown in Fig. 10. As "third" amplifier we have chosen an O.A. mod. OPA 27EZ (Burr-Brown) because the conventional unity gain buffer mod. BB 3627, suggested from the B.B. Company<sup>9)</sup>, is not stable enough, for our purpose, from the point of view of initial offset voltages and vs. temperature voltage drift. The model BB 3627 has offset and drift values of  $250$   $\mu\text{V}$  and  $10$   $\mu\text{V}/\text{C}$  respectively, while those of the OPA 27EZ are  $10$   $\mu\text{V}$  and  $0.2$   $\mu\text{V}/\text{C}$ . Moreover, the dynamic response of BB 3627 (8 kHz at - 1% flatness) is too poor, while for the OPA 27EZ it is equal to  $\approx 40$  kHz.

For the OPA 27EZ one has to add the gain-setting and feedback resistors ( $R$ ,  $R^*$ ,  $R_3$  in Fig. 10), which must be selected with a relative accuracy of 0.05%, to obtain large values of the d.c. CMRR.

The same accuracy and stability are necessary for the first-stage feedback resistors ( $R_2$ ,  $R_2^*$ ). For these reasons metal film, high stability resistances (SFERNICE, type RCME K8) have been used.

The bandwidth (BW) of the total circuit is large enough to allow a flat

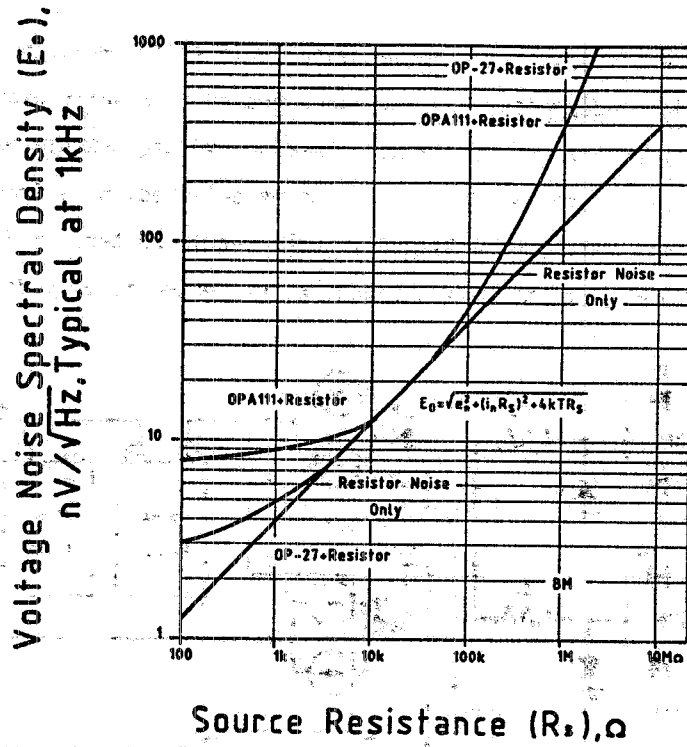


Fig. 9 - Total voltage noise spectral density vs source resistance, configuration of Fig. 8a.

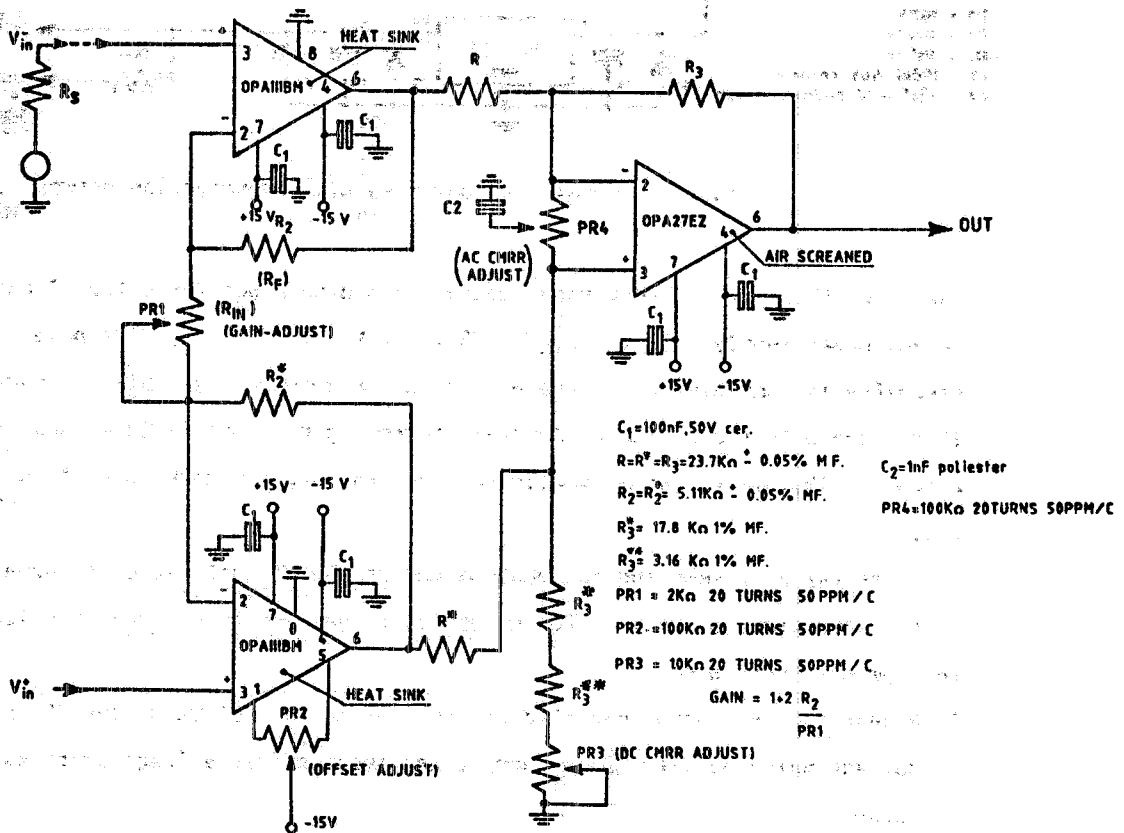


Fig. 10 - Details of the TIA.

response (-1%) up to a frequency of about 20 KHz when the gain is 10.

Two independent TIA have been housed in a unity width standard NIM unit. They are powered (Fig. 11) with internal voltage regulators ( $\pm 15$  V, 1 A). The "main" comes from NIM bin or it can be selected, by a front panel switch, from an internal array of 4  $NiCd$  9 V rechargeable battery (mod. RX22) to minimize ground loop effects, which cannot be neglected in very delicate measurements.

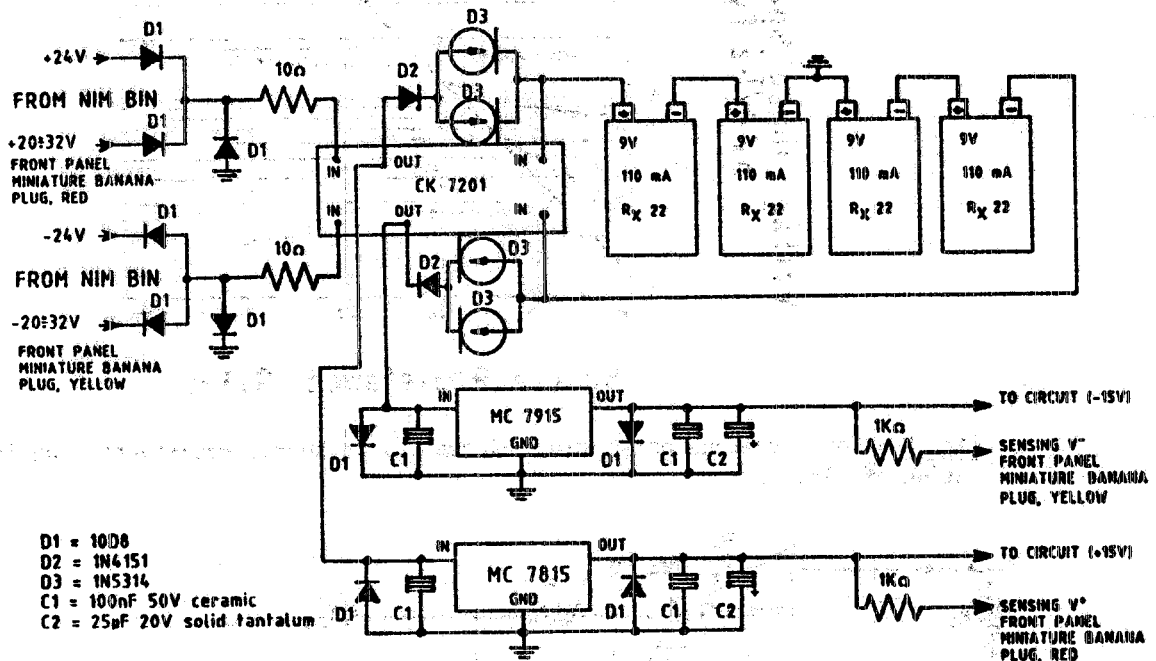


Fig. 11 - Details of power supply and protection networks.

Moreover, there are 3 front panel miniature banana plugs for external connection to any power supply ( $-20$  V  $< V_{in}^- < -35$  V,  $20$  V  $< V_{in}^+ < 35$  V). The power supply circuitry is completed with several protection networks (essentially diodes type 10 D8) and with the system of constant current generators (1N5314) and decoupling networks (1N4151) to automatically recharge the battery pack when it is not in use.

As far as assembling and maintenance of the circuitry are concerned we used, at the same time, several different skills to get and to preserve for long time the nominal performances:

- 1) A heat-sink has been connected to the case of the FET OA to keep "constant" voltage noise density, bias current and input offset voltage drift vs. temperature.
- 2) To avoid any thermal instability the OPA 27EZ has been screened against "air

- flow", keeping, as constant as possible, the voltage offset and drift. This contribution is significative in the case of low gain of the first stage.
- 3) The ceramic blocking capacitor (Fig. 10, C<sub>1</sub>) must be put as close as possible to the power supply terminal of the O.A. to avoid H.F. spurious oscillations.
  - 4) The power supply section has been screened from the amplifying section with copper foil.
  - 5) The layout of the printed board must be checked carefully, before and after soldering, against any type of leakage or noise pick-up in the non-inverting inputs of the front-end O.A.
  - 6) All input and output connections are performed by coaxial cable. Much care has to be used with input connectors (LEMO 00 model RRA. 00250.NTC) well clean and with "regularly round" soldering to minimize leakage. Input as well as output connectors are provided with protection head (LEMO mod. GCD.00020.LN) to avoid any external or internal pick-up or "emission".
  - 7) It is necessary to use low-profile Teflon sockets for any O.A.
  - 8) After assembling all components, except the 3 O.A. in the predisposed sockets, it is necessary to clean the circuit by ultrasound bath in FREON 113 for at least 5 minutes. After the circuit is completely dry it is necessary to put it in a bath of Isopropilic Alcohol for 5 minutes.
  - 9) During "switch ON" and "switch OFF" conditions and when it is not operating it is safe to terminate the inputs with 50 ohm to ground.

#### 4.- CHARACTERISTICS AND PERFORMANCES

The differential gain is adjustable in the range 7-1000 according to the gain equation:  $A_d = 1 - 2 R_2 / PR_1$ . Initial Offset Voltage, d.c. CMRR, and a.c. CMRR can be compensated and regulated by internal trimmers. The performances of the battery operated TIA with  $A_d = 100$  (unless otherwise noted) at an ambient temperature  $T_a = 25$  C are summarized in Table I.

#### 5.- CONCLUSIONS

We have realized a rather simple and economical TIA that, thanks to the new Difet technology developed from B.B. has an overall performance better than similar circuits available today. Some care has to be spent both in components selection, in proper layout and final calibration to get the good nominal performances. A comparison with the very high performance discrete module PARR 113<sup>9)</sup> does not show large performance differences, even in the total voltage noise source with

TABLE I - Performances of the TIA

|   |
|---|
| Rated output voltage : $\pm 12$ V, with $R_L > 2$ K $\Omega$  |
| C (load) < 2000 pF  |
| Input offset voltage : initially adjusted to 0.3 $\mu$ V  |
| Nominal input offset voltage drift with temperature, RTI, arising by only<br>1 OPA 111 BM : + 0.5 $\mu$ V/C                                   |
| Short time (few minutes) input offset voltage instability = + 0.25 $\mu$ V  |
| Nominal input Bias current at $V_{cm} = 0$ $V_{dc} = + 0.7$ pA  |
| Nominal input offset current at $V_{cm} = 0$ $V_{dc} = + 0.3$ pA  |
| Nominal input impedance : $10^{13}$ $\Omega$ /1 pF plus cable connection  |
| Nominal offset voltage due to input bias current with $R_S = 1$ M $\Omega$ source<br>impedance imbalance : $E_{S1} = 1$ $\mu$ V               |
| Nominal offset voltage due to input current offset with $R_{S1} = R_{S2} = 1$ M $\Omega$ :<br>$E_{CO} = 0.5$ $\mu$ V                          |
| Total input offset voltage with source impedance imbalance 20 M $\Omega$ = +25 $\mu$ V,<br>- 30 $\mu$ V                                       |
| Gain-error due to $Z_{id}$ with $R_S = 1$ M $\Omega$ : $10^{-7}$  |
| Total noise spectral density (RTI) with $R_{S1} = 1$ M $\Omega$ , $R_{S2} = 0$ $\Omega$ , $f_o = 1$ Hz:<br>$E_n = 180$ nV/ $\sqrt{\text{Hz}}$ |
| Total noise density (RTI), with $R_{S1} = 1$ M $\Omega$ , $R_{S2} = 0$ $\Omega$ , $f_o = 10$ Hz :<br>$E_n = 130$ nV/ $\sqrt{\text{Hz}}$       |
| Total noise density (RTI) at gain = 10, $R_S = 10$ K $\Omega$ , $f_o = 1$ KHz :<br>$E_n = 20$ nV/ $\sqrt{\text{Hz}}$                          |
| Dynamic response, - 3 db flatness, = 20 KHz   |
| Dynamic response, - 3 db flatness, G = 10, = 230 KHz  |
| D.C. CMRR (with $V_{id} = \pm 10$ V) = 120 db   |
| A.C. CMRR (at 100 Hz, $V_{id} = \pm 10$ V $_{sin}$ ) = 116 db   |
| A.C. CMRR (at 1 KHz, $V_{id} = \pm 10$ V $_{sin}$ ) = 98 db   |
| Short circuit duration = indefinite   |
| Nominal power dissipation for each TIA with $R_L = \infty = < 220$ mW   |
| Power supply for each module (2 TIA) voltage regulators, protection net-<br>works, etc.) : I(+15V) = 20 mA; I(-15V) = 21 mA                   |
| Autonomy with internal battery > 4 hours  |

enough large value of resistance ( $R_S > 10 \text{ Kohm}$ ) the total value of noise  $E_0$  is practically the same because the main contribution, according to eq.(5), arises from both thermal noise of  $R_S$  itself and shot noise of  $i_n$ , not from  $e_n$ .

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