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1 Introduction

The user's needs are growing day by day, which require more and more powerful and sophisticated computer systems. With the recent advances in the integrated circuit technology it is now possible to build powerful computer systems with lower cost. It is more cost effective to have systems with multiprocessors sharing global resources. In addition, these systems require extra memory for storing data and program, since computers have limited memory. Memory banks and backup store are also required for archiving data and programs. Sometimes it is also necessary for a computer system to exchange information with another computer system, either directly or indirectly. There has always been a problem to interface a computer system with another computer system with ease in a multiprocessor environment.

The data can be exchanged either serially or in parallel. The serial communication is cheaper but slower as compared to parallel data communication. However, the parallel data communication is expensive to implement specially for long distance transmission.

2 The VME-bus

In 1981 a joint effort by Mostek, Motorola and Signetics/Philips introduced the VME-bus specification. In all three separate buses were defined, the VME-bus, the VMX-bus and the VMS-bus. Each may be used independently of other or collectively used to produce a highly capable multiprocessor system architecture [1]. A short description of VME-bus is as follows.

The VME-bus specification [2] defines an interfacing system for use in interconnecting data

processing, data storage and peripheral control devices in a closely coupled configuration. The VME-bus interface consists of four groups of signal lines called 'buses' and a collection of functional modules which can be configured as required to interface devices to the buses.

A functional module which is capable of initiating data bus transfer on the VME-bus is called DTB (Data Transfer Bus) master. At an instant there is only one DTB master, bus arbitration is required to make a decision as to which VME-bus module will be the master during the next data transfer cycle, this prevents a simultaneous access of the bus by two or more masters. The DTB requesters and DTB arbiters are used for the transfer of control to another master if there is any. The functional modules involved in data transfer are always classified as a master and a slave. The master is the module controlling the transfer and the slave is the responding or addressed module. Some boards may be designed to act both as master and/or slaves.

The slaves can interrupt the normal operation of the VME-bus master. The master will suspend current program execution and will perform an interrupt routine. The functional modules are called interrupters and interrupt handlers. The interrupts are requested on the interrupt bus.

The data exchange takes place over the data transfer bus (DTB) which can be logically sub-divided into data, address and associated control signals. The DTB is a high speed asynchronous parallel data bus. The data bus can be 8-bits, 16-bits or 32-bits wide. Each data transfer on the DTB occurs between a functional DTB master and a functional DTB slave. The data transfer is always initiated by the DTB master. After each data transfer the slave must generate a data acknowledge (DTACK, active low) signal before the Bus Time Out (BTO). The bus time out is controlled by the master, which indicates that the master will abort the current read/write cycle after n microseconds, if the slaves do not acknowledge the data transfer. This protects the system against invalid addresses or malfunctioning slave(s). The asynchronous nature of the DTB allows the slave to control the amount of time taken for the data transfer. However, when a data acknowledge is received by the master from the slave, the current data transfer cycle is terminated.

The smallest addressable unit of storage is called a 'byte' and is equal to 8-bits. The location in which the byte is stored is called a byte location. Two consecutive bytes i.e. even and odd (next high order byte) is called a word location.

The VME-bus provides 31-bit address bus for extended addressing of up to 4 Gigabytes. Extra address decoding logic is required if all the 31-bits are decoded. However, short addressing provides 16 Mbytes of addressing. All the address lines need not be decoded for short or standard addressing.

During the data transfer additional information is passed to the slaves by the master through Address Modifier (AM0-AM5) lines. Separate codes are set aside for each type of addressing. The information provided by the address modifier lines can be used in several ways [2]. For example, slaves receiving address modifier codes for short addressing ignore address lines A16-A31, for standard addressing slaves ingore address lines A24-A31 etc. The address modifier codes are driven by the master and are classified into three categories defined by: VME-bus specification, user, reserved. Care must be taken when choosing and implementing the address modifier codes.

A 16 MHz clock signal (SYSCLK) is also available on the VME-bus specification with a 50 percent (nominal) duty cycle. This signal can be used to generate on-board timings and delays. The SYSCLK has no fixed phase relationship with other VME-bus timings. The SYSCLK driver is normally located on the system controller board. The driver is a special (high current) totempole device and only one receiver per board is allowed.

System reset and initialisation is performed by a power monitor module and/or by a manual switch. On powerup the master performs a selftest and tests non intelligent boards. If all the boards are functioning normally the master then performs initialisation of the peripherals etc.

Address Strobe (AS) line when low indicates the presence of a valid address on the address bus. Data Strobes DS0 and DS1 lines when low indicate valid low order and high order data byte respectively. For 16-bit data DS0 and DS1 are low simultaneously.

A write line (WRITE) when high indicates a read operation on the memory or peripheral. While a low level indicates a write operation. A Bus ERRor (BERR) signal indicates a bus error if data transfer either read or write is not achieved.

3 Memories

Since the advent of computers several types of memories are available. Some memories are faster hence expensive than others. Some are cheap but slow. The choice depends upon a particular application. Memories can be classified in several ways eg: volatile, non-volatile, static, dynamic etc. A volatile memory is that which looses its contents when the power is switched off. However, a non-volatile memory retains its contents even when there is no power. Some examples of memories are magnetic disc, magnetic tape, magnetic drum, magnetic core, thin film, semiconductor, magnetic bubble and plated wire etc.

Different memory technologies are used to fabricate and make various memory devices. The MOS (Metal Oxide Semiconductor) technology is used to fabricate integrated memory cells. The MOS memory cell can either be dynamic or static. The basic difference between a dynamic and static memory cell is the way in which the data are stored in the memory cells. The static memory cell uses a conventional flip-flop to store a bit of information. However, a dynamic memory cell uses a capacitor to store a bit. The choice of the type of memory depends upon several factors eg: ease of use, access time, power dissipation, size of memory chip, memory requirements, price and standby power etc.

The static RAMs are easier to use since their operation is static and no memory refresh logic is required. In addition it is easier to generate the control signals. However, the storage element in a dynamic memory is a dynamic charged capacitor. The storage capacitance is actually the parasitic capacitance of the transistor. The charge of this capacitor leaks off with time, which must be restored or refreshed periodically. The refresh rate depends upon temperature and must be done once every 2 msecs at 70 degrees centigrade. The external hardware refresh circuitry requires a binary counter depending upon the size of the RAM eg: 4k, 16k RAM requires 64, 128 cycles respectively. In addition, multiplexing of the binary counter into RAM row and column addresses, and a timer to indicate when the refresh should be performed. Some dynamic memory chips have an on-chip refresh circuitry, this automatic refresh is controlled by an external pin. The static memories consume more power and hence are of low density and are more expensive than an equivalent dynamic memory. The MOS memory element is also economical in chip area and requires less processing steps to fabricate as compared to their bipolar counterparts.

4 Design and Construction of the Memory Expansion Board

The prototype memory expansion board is a double height VME-bus board (233 x 160 mm) which consists of 256k 16-bit words of dynamic memory. The memory expansion board is used in conjunction with the MVME110 [3],[4] (VME-bus module) which is a MC68000 based monoboard microcomputer system. Figure 1 shows a block diagram of the arrangement, user's interface is a Visual Display Unit (VDU). The MC68000 is an 8 MHz Central Processing Unit (CPU) when operating as a system controller. The MVME110 is a high performance processing module designed to function as either a stand alone microcomputer, as a single system controller in a VME-bus system

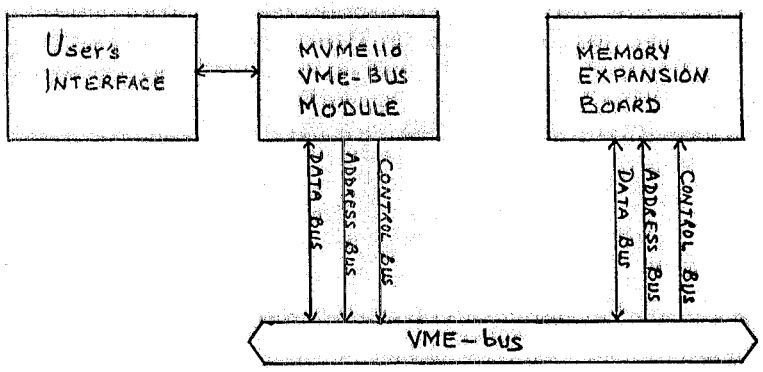

Figure 1: Block diagram of the memory expansion board.

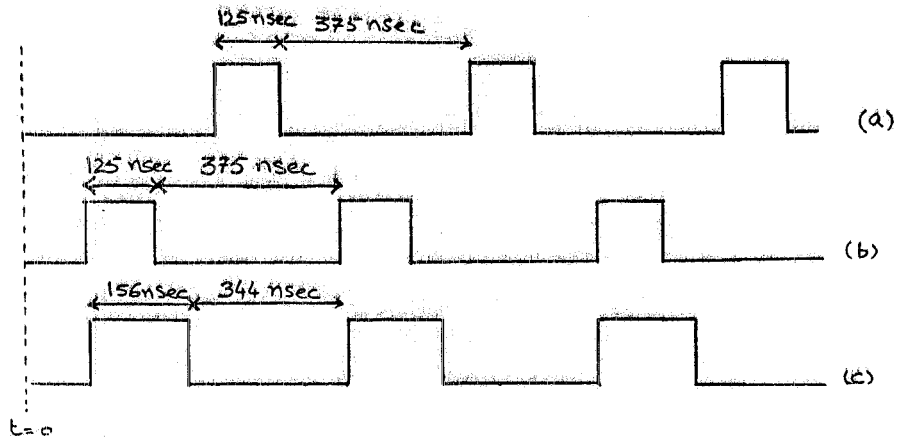

Figure 2: (a) Clock pulses for the counter U7
(b) Refresh pulses 125 nsec wide, jumper J1 position 1
(c) Extended refresh pulses 156 nsec wide, jumper position 2.

or as one of several CPU elements in a multiprocessor VME-bus configuration. The MC68000 is capable of addressing 16 Megabytes of memory.

The MVME110 provides full support for the VME-bus addressing and control logic. The on-board local memory can be accessed without effecting the operation of the VME-bus being used by another system controller, DMA (Direct Memory Access), high speed I/O (Input/Output) or by another CPU module. The connection to the VME-bus is through a DIN41612 triple row 96 pin P1 connector to the backplane of the VME-bus module. Table 1 shows pin connections for the P1 connector.

TABLE 1. VMEbus Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA BUS (bits 0-7) - Eight of 16 three-state bidirectional data lines which provide the data path between VMEbus master and slave.
A9,A11,A15, A17,A19 B20,B23, C9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - 16-MHz signal used as timing reference. When system controller, this signal is provided by the VME110 to the VMEbus.
A12	DS1*	DATA STROBE 1 - Bidirectional signal that indicates a data transfer on data bus lines D08-D15. When system controller, this signal enables the bus timeout counter.
A13	DS0*	DATA STROBE 0 - Bidirectional signal that indicates a data transfer on data bus lines D00-D07. When system controller, this signal enables the bus timeout counter.
A14	WRITE*	WRITE - Output signal that indicates the direction of data transfers.
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - Input signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A18	AS*	ADDRESS STROBE - The falling edge of this bidirectional signal indicates a valid address is present on the address lines. During bus arbitration, a high level indicates that the previous master has released its signal lines.
A20	IACK*	INTERRUPT ACKNOWLEDGE - Output signal indicates a VME interrupt acknowledge cycle.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKIN* input signal is connected directly to IACKOUT*.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKOUT* output signal is connected directly to IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of five three-state output lines used to provide additional information about the address bus.
A24	A07	ADDRESS bus (bit 7) - One of 23 three-state driven output lines which specify an address in the memory map
A25	A06	ADDRESS bus (bit 6) - Similar to pin A24.
A26	A05	ADDRESS bus (bit 5) - Similar to pin A24.
A27	A04	ADDRESS bus (bit 4) - Similar to pin A24.

TABLE 1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A28	A03	ADDRESS bus (bit 3) - One of 23 three-state driven output lines which specify a memory address. During an interrupt acknowledge cycle, address bus lines 1-3 are used to indicate the interrupt level which is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - Similar to pin A28.
A30	A01	ADDRESS bus (bit 1) - Similar to pin A28.
A31	-12V	-12 Vdc power - used by logic circuits.
A32 B32 C32	+5V	+5 Vdc power - used by logic circuits.
B1	BBSY*	BUS BUSY - This bidirectional signal is driven low when the VME110 is the VMEbus master. Also an input to the arbiter to indicate that the bus may be arbitrated.
B2	BCLR*	BUS CLEAR - Input signal that causes the release of bus mastership in the RBC mode.
B3	ACFAIL*	AC FAILURE - Input signal that indicates a power failure has occurred and generates a level seven interrupt request.
B4,B6, B8,B10	BG0IN*- BG3IN*	BUS GRANT (0-3) IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. A grant received at the jumpered level indicates the VME110 may become the bus master. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5,B7, B9,B11	BG0OUT*- BG3OUT*	BUS GRANT (0-3) OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus-grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.
B12-15	BR0*-BR3*	BUS REQUEST (0-3) - The bidirectional bus request of the jumpered level is true when the MPU requires bus mastership. When one or more of the bus request lines is true in the ROR mode, bus mastership is released. When the VME110 is the system controller, bus request level three is monitored by the arbiter.
B16-19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - Similar to pin A23.
B21	SERCLK	Not used.
B22	SERDAT	Not used.
B24-30	IRQ7*- IRQ1*	INTERRUPT REQUEST (7-1) - Seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.

TABLE 1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B31	+5V STDBY	Not used.
C1-8	D08-D15	DATA BUS (bits 8-15) - Eight of 16 three-state bidirectional data lines which provide the data path between VMEbus master and slave. Similar to pins A1-8.
C10	SYSFAIL*	SYSTEM FAIL - Reflects state of FAIL bit in MCR and FAIL indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - Indicates an error has occurred during data transfer cycle. The cycle is terminated and the MPU starts exception processing. When the VME110 is the system controller, this bidirectional signal is generated when a data transfer cycle did not complete within 200 us.
C12	SYSRESET*	SYSTEM RESET - Causes a board level reset when received from the VMEbus. When system controller, a board level reset causes this bidirectional signal to be generated to the VMEbus
C13	LWORD*	LONGWORD - Not driven. This terminated signal remains at a high level when the VME110 is bus master.
C14	AM5	ADDRESS MODIFIER (bit 5) - This output line is not driven by the VME110. AM5 always appears as a high (true) level on the VMEbus because of the backplane termination.
C15	A23	ADDRESS bus (bit 23) - One of 23 three-state driven output lines which specifies an address in the memory map Similar to pin A24.
C16	A22	ADDRESS bus (bit 22) - Similar to pin A24.
C17	A21	ADDRESS bus (bit 21) - Similar to pin A24.
C18	A20	ADDRESS bus (bit 20) - Similar to pin A24.
C19	A19	ADDRESS bus (bit 19) - Similar to pin A24.
C20	A18	ADDRESS bus (bit 18) - Similar to pin A24.
C21	A17	ADDRESS bus (bit 17) - Similar to pin A24.
C22	A16	ADDRESS bus (bit 16) - Similar to pin A24.
C23	A15	ADDRESS bus (bit 15) - Similar to pin A24.
C24	A14	ADDRESS bus (bit 14) - Similar to pin A24.
C25	A13	ADDRESS bus (bit 13) - Similar to pin A24.
C26	A12	ADDRESS bus (bit 12) - Similar to pin A24.
C27	A11	ADDRESS bus (bit 11) - Similar to pin A24.
C28	A10	ADDRESS bus (bit 10) - Similar to pin A24.
C29	A09	ADDRESS bus (bit 9) - Similar to pin A24.
C30	A08	ADDRESS bus (bit 8) - Similar to pin A24.
C31	+12V	+12 Vdc power - used by logic circuits.

The memory expansion board occupies 256k 16-bit words of dynamic memory from address $1000 to $3FFFF ($ shows hexadecimal values) in the VME-bus memory space for the MVME110 VME-bus module. The memory is arranged in four banks, each bank consists of 64k 16-bit words. The memory refresh is transparent to the CPU since the operation of the CPU need not be suspended to perform the refresh, except for the time out which is described later. Memory refresh can be hardware or software oriented [5],[6].

Table 2: Components list

U1,U2,U3,U4	SN74158	2-to-1 line multiplexer
U5,U6	SN74245	Bidirectional bus transceiver
U7,U8,U9	SN74393	Dual cascadable 4-bit binary counter
U10,U11,U21 U22,U23,U24	SN7474	Dual positive edge triggered D-type flip-flop
U12,U13,U14 U15,U16	SN74266	Quad two input exclusive NOR with open collector
U17,U18	SN7421	Dual four input AND
U19	SN74260	Dual five input NOR
U20	SN74138	3-line-to-8-line decoder
U25,U26,U27	SN7408	Quad two input AND
U28,U29	SN7400	Quad two input NAND
U30,U31,U32	SN7432	Quad two input OR

Figure 3 shows a schemetic diagram of the memory expansion board. The portion enclosed in the dotted area in figure 3 is equivalent to 256k 16-bit words of dynamic memory as shown in figure 4 (all the memory chips are not shown in the figure). Values in brackets in figures 3 and 4 correspond to signals on the VME-bus pin connector P1 (see table 1). While the other numbers describe the pin numbers of a particular component. When the memory board is not being accessed the multiplexers U1 and U2 are disabled, thus isolating the memory board's address lines from the VME-bus. The address lines of the dynamic memory MCM6665 are connected to a 7-bit binary counter U7 through U3 and U4. Input B of the multiplexer U3 and U4 is selected since the output of U17(a) is high (letters in brackets correspond to logic gates as described in their respective data sheets). Only 7-bit address is required for the RAS-only refresh, with data input/output and CAS in don't care

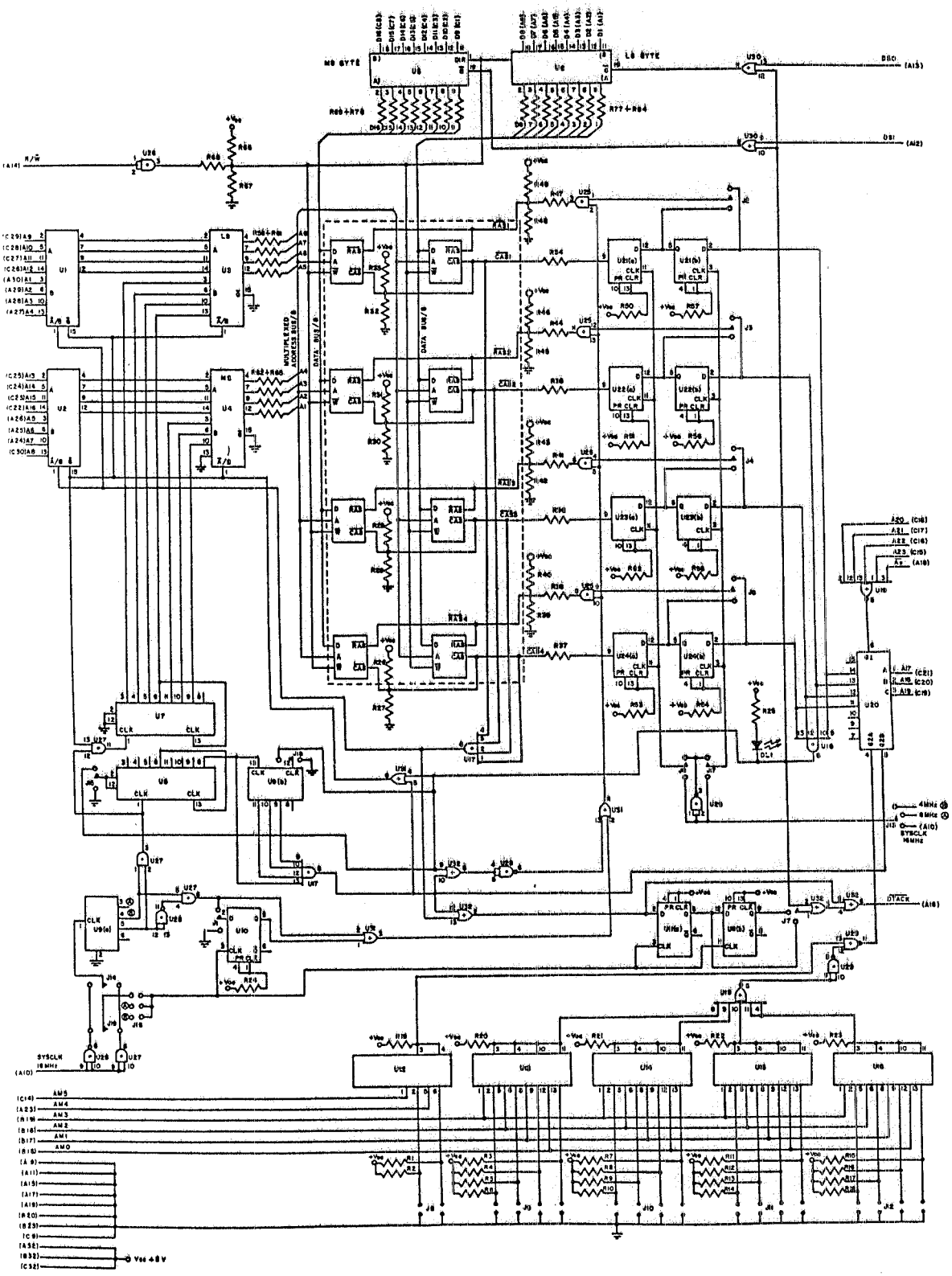

Figure 3: Schemetic diagram of the memory expansion board.

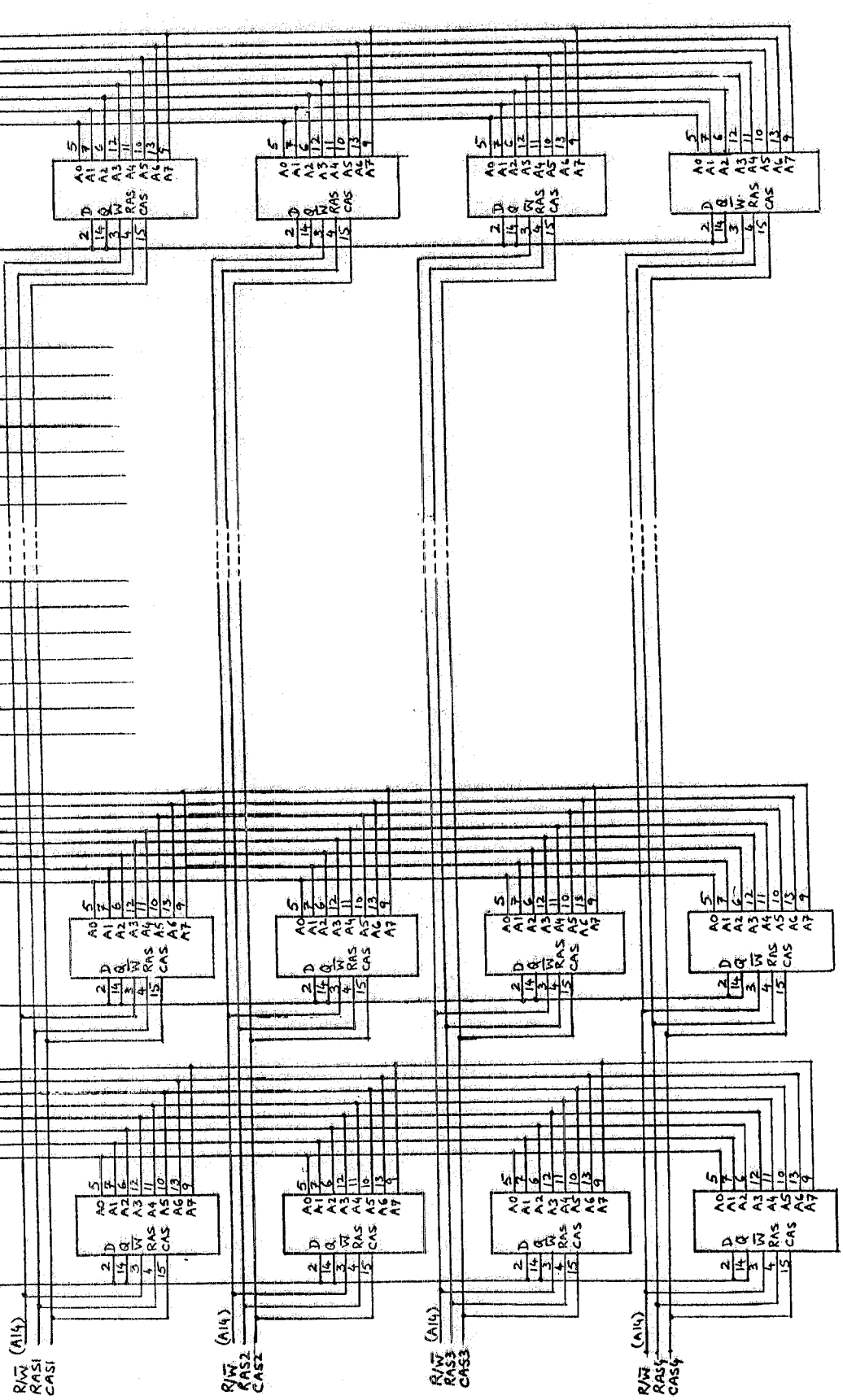

Figure 4: 256k 16-bit word dynamic memory.

condition. The MCM6665 is a high speed dynamic memory organized as 65536 1-bit words, and fabricated using HMOS high performance N-channel silicon gate technology. The access time is of the order of 150 nsec. The refresh cycle is 2 msec. The RAS refresh pulses are generated by ANDing the 4 and inverted 8 outputs of the binary counter U9(a). The RAS signal appears at the output of U31(a) and U31(d). The pulses for counter U7 are obtained by ANDing 4 and 8 signals at the output of U9(a). Jumper J1 provides an extended RAS pulse if required, the extended pulse is 156 nsec wide whereas the normal RAS pulse is only 125 nsec wide. When the memory board is disabled the gate U31(d) is enabled thus connecting the RAS refresh pulses to the memories through U25(a), U25(b), U25(c) and U25(d) to the four banks of memories simultaneously and continuously as RAS1, RAS2, RAS3 and RAS4 respectively. The gates U25(a), U25(b), U25(c) and U25(d) are enabled since U20 is disabled. The counting pulses for the address counter U7 and RAS pulses are out of phase with each other, see figure 2. This arrangement ensures that the addresses are stable before the RAS refresh pulse arrives. Since the memory board is not being accessed by the VME-bus the data acknowledge signal is always high. Since the DS0 and DS1 lines are high so the VME-bus data bus is also isolated from the memory board. The CAS inputs are always high during the memory refresh cycles and go low only during a memory access by the VME-bus. In addition the address modifier lines are also high thus disabling U20. The gates U27(c) and U28(c) provide either in phase or out of phase SYSCLK to the counter U9(a).

When the memory board is accessed one of the following address modifier codes are applied to the AM0-AM5 lines. The valid addess modifier codes are:

AM5	AM4	AM3	AM2	AM1	AM0	Function
1	1	1	0	0	1	Standard non-previlege data access
1	1	1	0	1	0	Standard non-previlege program access
1	1	1	1	0	1	Standard supervisor data access
1	1	1	1	1	0	Standard supervisor program access

The address modifier codes are selected by a combination of jumper J8 along with either J9, J10, J11 or J12. The jumper J8 is left unconnected to give a 3 and jumpers J9, J10, J11 and J12 are connected to give codes 9, A, D and E. These codes now correspond to address modifier codes as shown above 39, 3A, 3D and 3E. AM5 is the most significant bit and AM0 is the least significant

bit. The address modifier codes are compared with the above selected jumpers. When any of the above address modifier codes appear at the AM0-AM5 lines the output of the U29(d) goes low which is connected to G2A input of U20. U12, U13, U14, U15 and U16 are open collector exlcusive NOR gates. The G2B input is always low except for the refresh time out which is described later. The G1 enable of U20 is obtained by gating the address lines A20-A23 and the Address Strobe (AS) line. Once the U20 is enabled the address lines A17-A19 are decoded and appropriate low signal output appears at pins 14, 13, 12 or 11, which makes the output of U18(b) to go low. When the output of U18(b) is low the output of U31(d) goes high since it is disabled thus enabling the gates U25(a), U25(b), U25(c) and U25(d). The low output of U18(b) also enables U1 and U2. Since the output of U17(a) is high, B input of the multiplexer U1 and U2 is connected to the output. Input A of U3 and U4 is selected which connects the address lines of the VME-bus to the memory address lines. This connects the address lines A1-A8 to the appropriate memory bank. The counter U7 stops since the gate U27(d) is disabled, this arrangement remembers the previous memory location which was refreshed. The output pins 14, 13, 12 or 11 of U20 are low depending upon which bank of memory is to be addressed by decoding address lines A17-A19. This low signal provides a RAS pulse to that particular bank of memory through U25(a), U25(b), U25(c) or U25(d) respectively. Jumpers J2, J3, J4 and J5 provide a delayed RAS1, RAS2, RAS3 or RAS4 by one clock cycle if desired, after the output of U20 is low. Since the address lines are already connected to the memory bank, the RAS thus appearing latches the row addresses in the memory. The RAS1, RAS2, RAS3 or RAS4 pulse is delayed by one or two clock cycle(s) to generate the CAS1, CAS2, CAS3 or CAS4 pulse to latch the column addresses. U21, U22, U23 and U24 act as delay lines, this delay can be controlled by appropriately connecting jumper J13. Inverted or true clock for the delay lines U21, U22, U23 and U24 can be obtained by appropriately connecting jumpers J6 and J17. Any of the low CAS pulse makes the output of U17(a) to go low thus selecting A input of the multiplexer U1 and U2 which connects the address lines A9-A16 to the memory bank, since U3 and U4 are already enabled (memory requires RAS before CAS). This latches the column addresses in the memory. Simultaneously either DS0, DS1 or both low are to connect the data bus to the memory bank. U5 and U6 are bidirectional bus drivers. U6 provides the least significant byte and U5 provides the most significant byte of data. A read/write signal (WRITE) provided by the VME-bus is used to control the direction of the data flow through U5 and U6. This write line is buffered through U26(a). Series resistors are used on the data and address buses to act as current limiting resistors (approx. 30 Ohms) and to provide an interface between the TTL and MOS. Several pull-up and a combination

of pull-up and pull-down resistors are adjusted for optimum performance.

If the memory is continuously being accessed a time out counter consisting of U8 and U9(b) generates a signal at the output of U17(b) to indicate that the memory board needs refreshing, this time is about 1.9 msec. When this condition occurs the DTACK signal is forced high and the decoder U20 is disabled by making G2B high. Thus indicating a non memory access condition. When this is achieved then a normal 128 cycle memory refresh takes place. This time out counter can be disabled by appropriately connecting J15 and J18. A data acknowledge signal is generated by delaying the CAS (low) signal by one or two clock cycles using U11(a) and U11(b). This delay can be controlled by appropriately connecting jumpers J14, J16 and J19. During the refresh time out this is over ridden by the output generated by the U32(b) which forces data acknowledge into logic high. After the refresh the memory board returns to normal operation. A Light Emitting Diode (LED) is connected appropriately to show a memory access condition.

Figure 5(a) shows a layout of the printed circuit board. Figure 5(b) and 5(c) show the component and solder side of the printed circuit board. Decoupling capacitors (100 nF) are connected to each memory integrated circuit. Each row of power supply is decoupled using 10 uF capacitor. This provides maximum decoupling for efficient operation.

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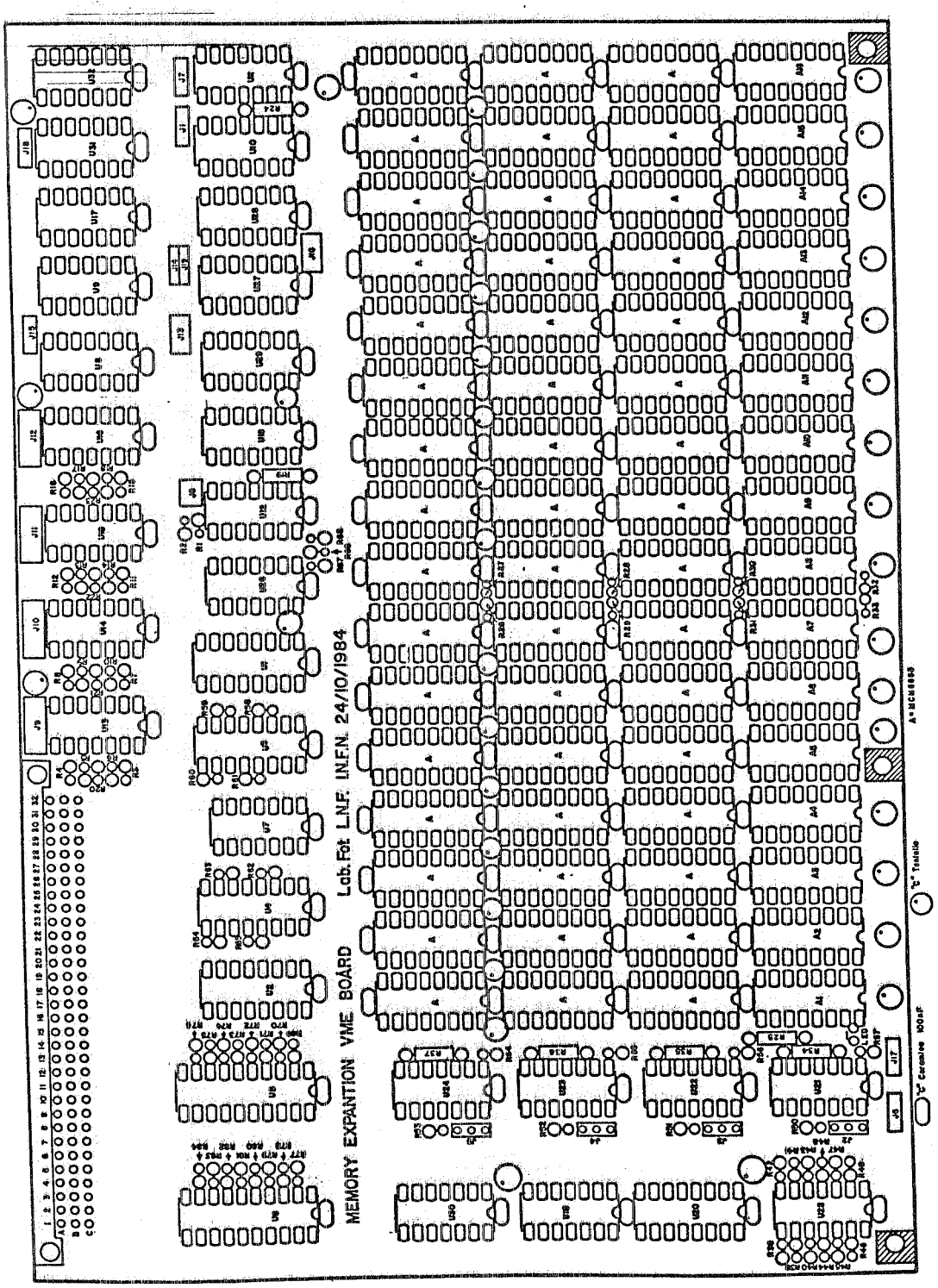

Figure 5(a): Layout of the printed circuit board.

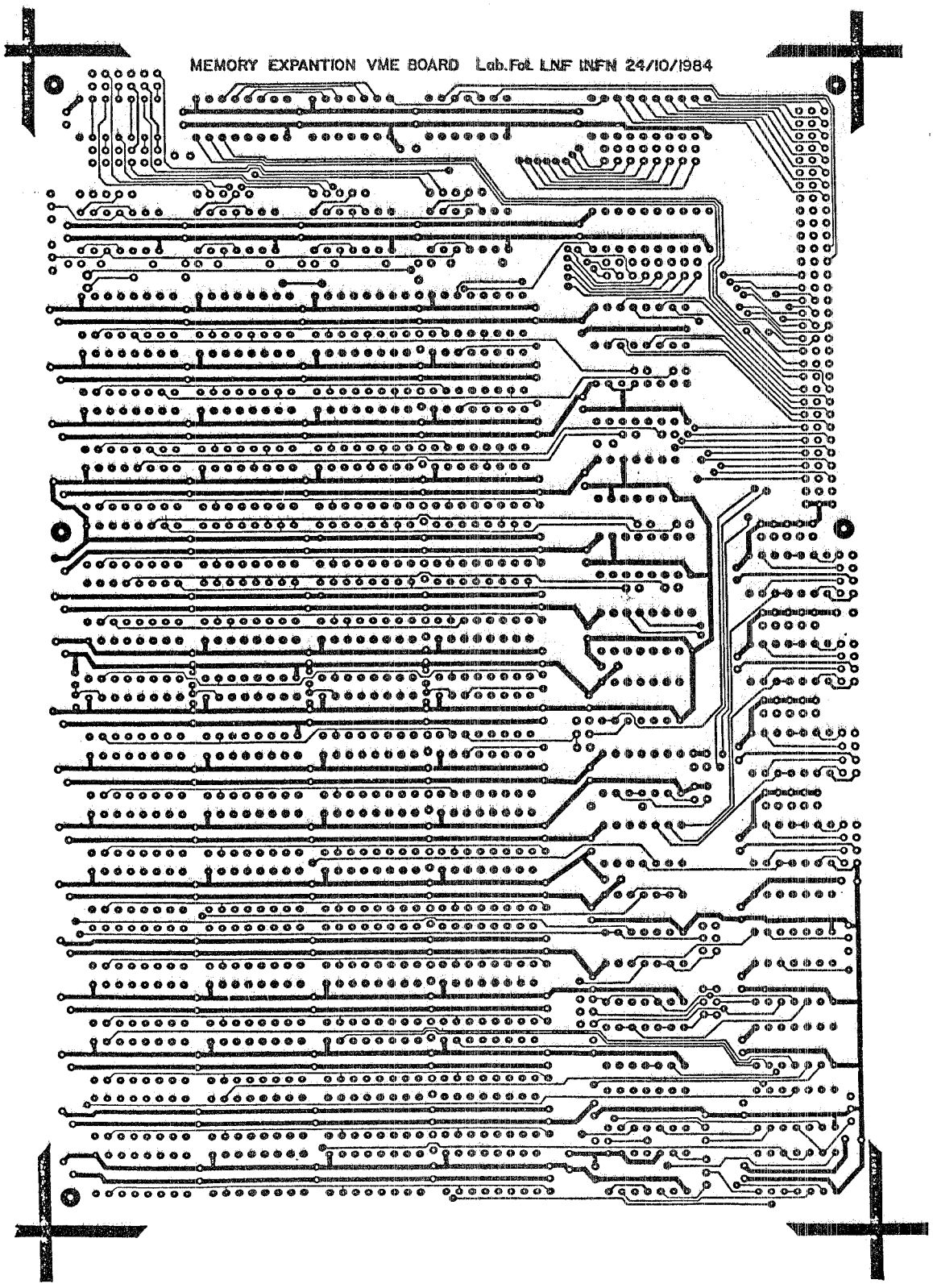

Figure 5(b): Printed circuit board (component side).

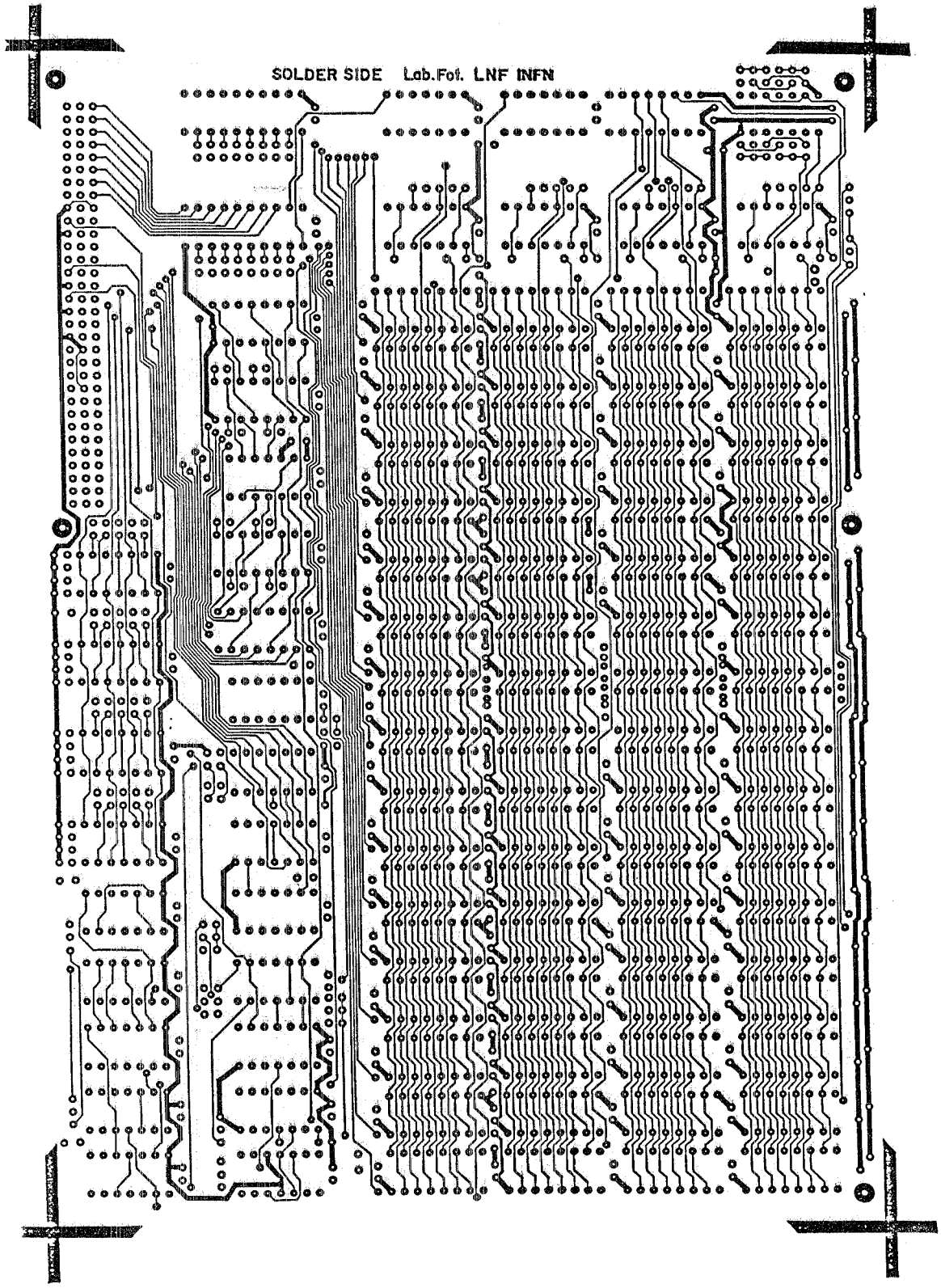

Figure 5(c): Printed circuit board (solder side).

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