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4 Dicembre 1980

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ABSTRACT

We describe design, circuitry and performances of a programmable system (FRAM 77 HV System) to supply and control high voltages in a large scintillation counter system.

Sixty four HV channels are housed in a single crate preserving modular construction.

A programmable CAMAC unit controls remotely the HV system through a high speed serial link; manual control is provided by a special purpose unit.

In the HV crate the analog-digital interface uses a time-multiplexed technique. Each HV generator is a switching DC-DC converter with pulse-width modulation. It supplies up to 2 mA from 0.3 to 3 KV.

Digital resolution, both in setting and reading operation, is 1 V; overall stability is better than 0.1%.

(+) Also at Istituto di Fisica dell'Università di Torino, and Laboratorio di Cosmogeofisica del CNR, Torino, Italy.
(°) Also at Laboratorio di Cosmogeofisica del CNR, Torino, Italy.
(x) This is a full version of the LNF-77/36 (1977).

1. - INTRODUCTION

At present high energy physics experiments employ often such an amount of elements (wires, photomultipliers ....) that they have to be remotely handled by a computer.

In designing and building the NA1 experiment which is presently taking data at the CERN SPS on photoproduction of charmed mesons[1], special systems[2,3] have been developed at LNF to control serially and remotely each independent channel of drift chamber, MWPC, light diode drivers and PMs high voltages. The apparatus, described elsewhere[4], consists of a forward spectrometer and a vertex detector devoted to measure photon energy and detect charged particles between 6 and 45 degrees. In this paper we describe the high voltage power supply system (FRAM 77 system) designed to supply and control the nearly 500 PMs of the vertex detector.

This system represents an important achievement in compactness (both in the digital control section and in HV generators) and in voltage setting resolution. Compactness is achieved by assembling 8 channels per generator module and up to 8 modules per crate with only one control unit and one multiplexed DAC-ADC unit. Output current can reach 2 mA in the negative voltage range 0.3 - 3 KV. The system is controlled by a standard CAMAC interface through a high speed serial link (four coaxial cables) extendible up to some hundreds meters between apparatus and control room. Among other, this solution saves the cost for HV cables(*).

The modular structure of this system allows the use of its logical section for different purposes, when the high voltage modules (see block diagram, Fig. 1) are substituted by other devices. As an example, LEDs to check stability of PMs of the vertex detector are driven by modules[3] handled by the same system.

(*) The FRAM 77 System is being manufactured and commercially distributed by Pulsar S.r.l., Guidonia, Italy.

2. - GENERAL DESCRIPTION

The block diagram is shown in Fig.1. The system constists of:

1 - Eight HV modules with eight independent generators
2 - A conversion module (MCS)
3 - A Timing-ON/OFF module
4 - A remote control module (RCU)
5 - A CAMAC interface called Master Control Unit (MCU)

Items 1 + 4 are housed in a crate and linked by a special bus preserving maximum modularity. Full manual control and display capabilities are provided by the Control Display Unit (CDU) which can support up to eight complete systems.

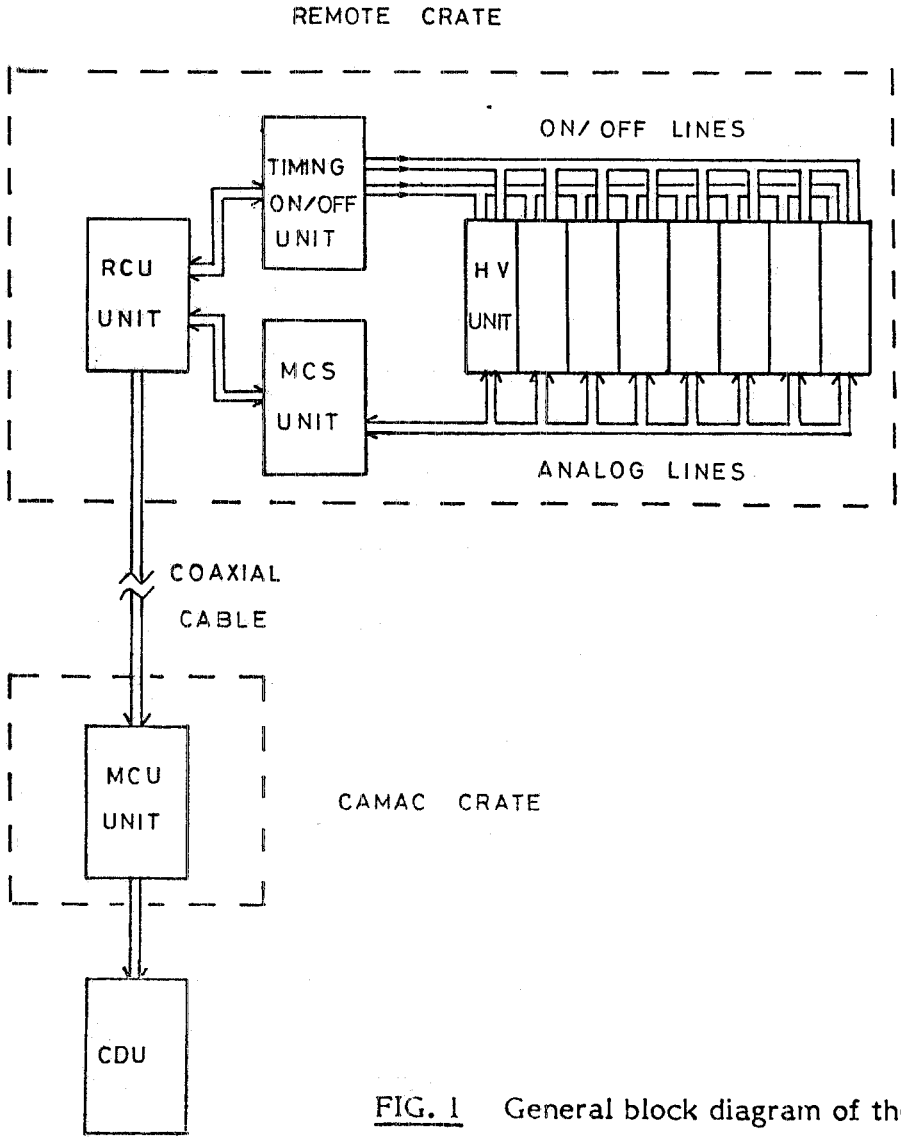

FIG. 1 General block diagram of the system.

3. - MASTER CONTROL UNIT (MCU)

The MCU is a double width standard CAMAC module which interfaces the remote system to the computer and the Control Display Unit (CDU). This module includes two independent sections (Fig. 2).

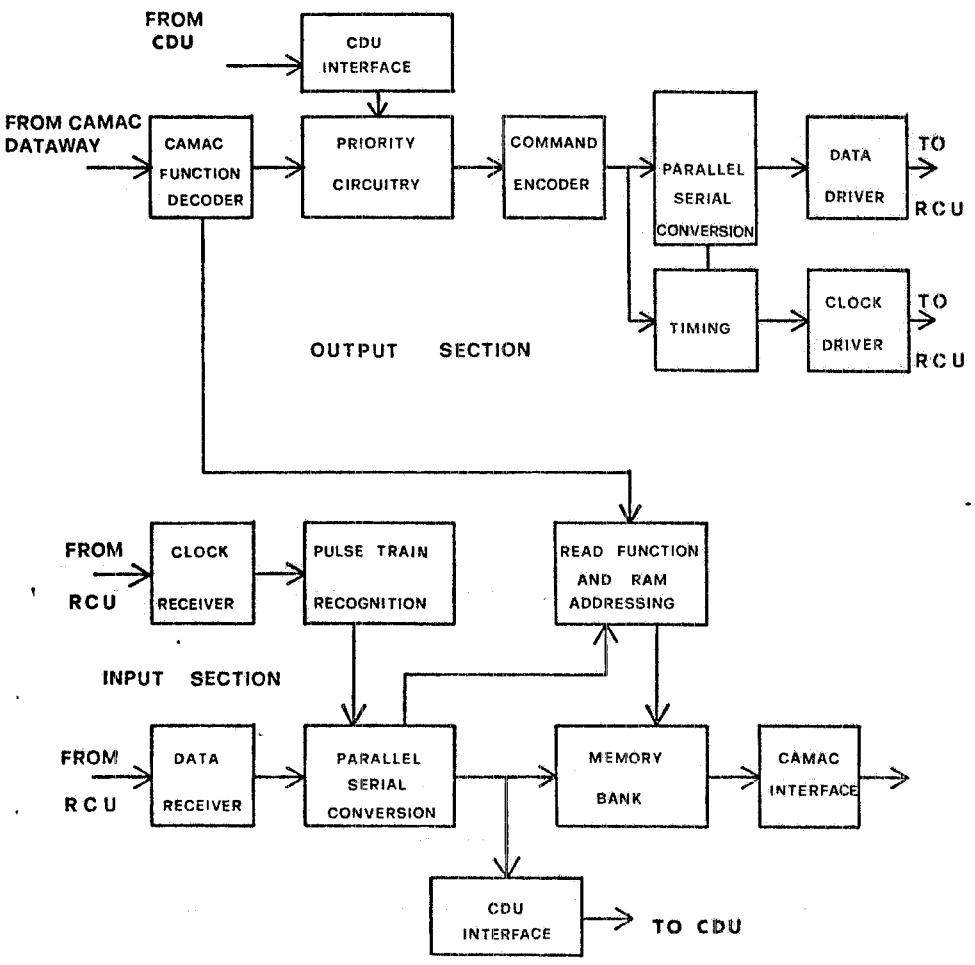

FIG. 2 Functional diagram of the Master Control Unit (MCU).

The output section allows to encode the commands coming from CAMAC or from CDU and to transmit them to the Remote Control Unit (RCU). The commands are sent in a serial format to RCU together with a main clock signal (1 MHz) for data recognition. The data are structured in words of twenty bits using two different formats. The first one specifies the CAMAC commands, which include: 12 bit-field for the set voltage value, 6 bit-field for the addresses and 2 bit-field for the operation code (increase-decrease-write). The second one specifies the CDU commands. They include: 6 bit-field for the

addresses and 6 bit-field for the operation code (increase-decrease, enable-disable computer, on-off switching, master reset).

The input section houses a bypolar RAM memory which stores a copy of the system status. Appropriate CAMAC functions make it available for read-out.

The 64 channels status is sequentially and cyclically updated by the serial data coming from RCU. The status data include for each channel: the set voltage value (12 bits), the read voltage value (12 bits), the underflow bit, the ON/OFF status bit, the COMPUTER ENABLE (CE) status bit.

Table I shows the CAMAC addressing format and function code.

TABLE I

CAMAC FUNCTION	St.*	CHANNEL+	
F(0)	N N+1	1 : 16 33 : 48	READ SET VOLTAGE VALUE
F(1)	N N+1	17 : 32 49 : 64	READ ACTUAL VOLTAGE AND THE 3 STATUS BIT
F(4)	N N+1	1 : 16 33 : 48	READ SET VOLTAGE
F(6)	N N+1	17 : 32 49 : 64	READ ACTUAL VOLTAGE AND THE 3 STATUS BIT
F(16)	N N+1	1 : 16 33 : 48	WRITE TROUGH CAMAC LINES W1÷W12 THE CHOSEN HIGH VOLTAGE DIGITAL VALUE
F(17)	N N+1	17 : 32 49 : 64	
F(12)	N N+1	1 : 16 33 : 48	INCREASE BY ONE STEP THE PREVIOUS HIGH VOLTAGE DIGITAL VALUE
F(19)	N N+1	17 : 32 49 : 64	
F(28)	N N+1	1 : 16 33 : 48	DECREASE BY ONE STEP THE PREVIOUS HIGH VOLTAGE DIGITAL VALUE
F(30)	N N+1	17 : 32 49 : 64	

* The 64 channels are divided in two blocks of 32 channels each, accessible by two individual N CAMAC lines, respectively N and N+1.

\+ The subaddress A selects a channel within the indicated range.

4. - REMOTE CONTROL UNIT (RCU)

This module accepts and decodes commands coming from MCU and sends data relevant to each HV channel to MCU. The functional diagram of the module is given in Fig. 3.

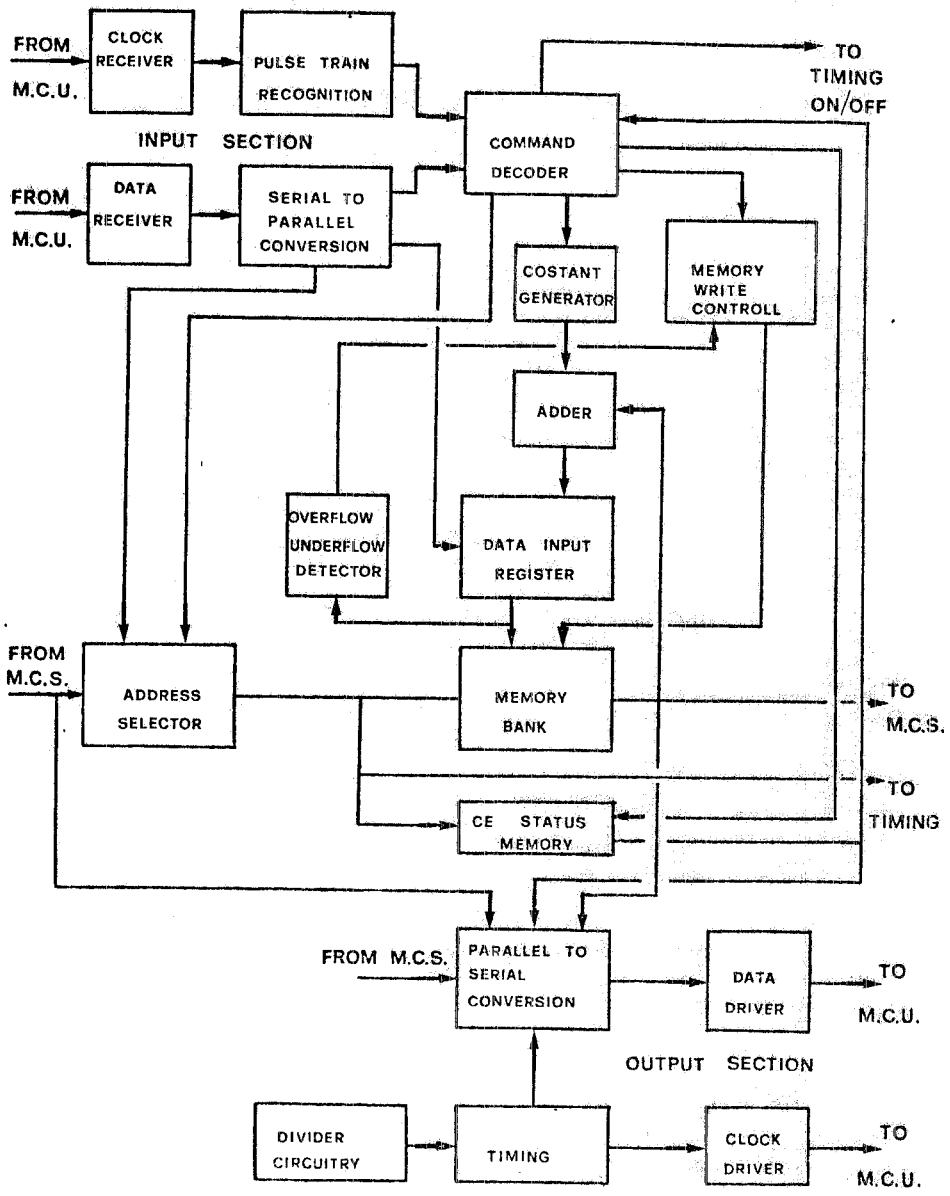

FIG. 3 Functional diagram of the Remote Control Unit (RCU).

One or more of the following actions concerning the addressed channel are performed:

a) setting or clearing the ON STATUS BIT, located within the register in the ON/OFF timing unit.
b) setting or clearing the computer enable status bit, located in a 64 x 1 RAM.
c) modification of the voltage stored in a 64 x 12 bit memory bank.

The memory contents can be modified by two different operations

- a direct transfer from the command data field to the memory (overwrite)
- a read-modify-write cycle using the adder to increase or decrease the voltage value by 1 or 10 steps.

Every command concerning the set voltage will be rejected, if it doesn't come from the source enabled by the CE status bit. A command will be also rejected if out-of-range condition is detected. In the output section the whole status of each channel (read-out voltage value, underflow bit coming from MCS, set voltage value as well as other status bits) is assembled and serially transmitted to MCU.

A pulse generated by the divider circuit starts data transmission, which occurs continuously. More details on RCU operation will be found in the description of MCS module.

5. - THE TIMING ON/OFF UNIT

Timing ON/OFF unit (Fig. 4) is an extension of the RCU, split into two independent sections. The first one forms a continuous pulse train (33 KHz) distributed on eight lines. These signals drive the DC-DC converter into the HV modules. The multiphase structure helps in decreasing the cross-talk among channels. It also improves the system behaviour as far as noise problem is concerned .

The second section houses the registers which store the ON/OFF status bit of each channel. This structure allows the ON/OFF command to be sent individually to each channel. The 64 latched outputs are linked to the respective HV generators.

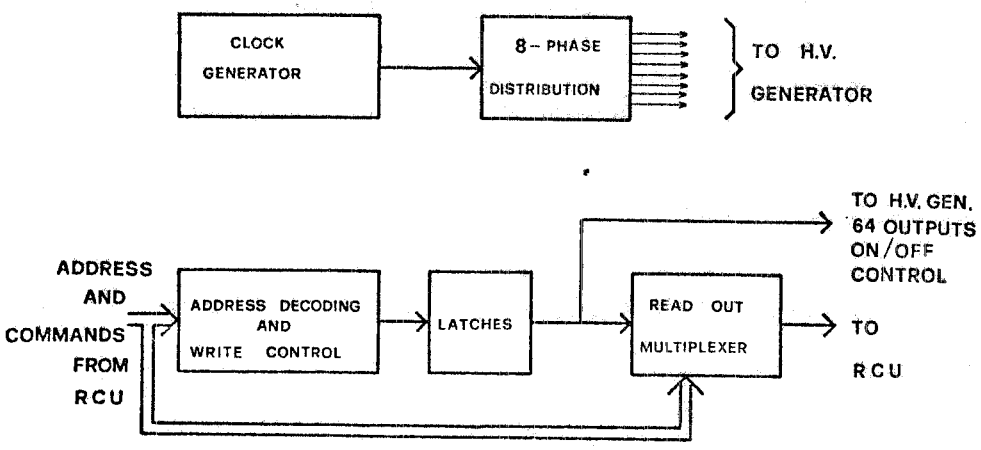

FIG. 4 Block organization of the ON/OFF unit.

6. - MULTICHANNEL CONVERSION SYSTEM (MCS)

This module interfaces the Remote Control Unit (RCU) to the analog units (HV generators). This requires a 64-input ADC and 64-output DAC, assembled onto separate boards.

Basically, a "time division" (a well established technique) relying upon analog multiplexers has been used in both sections.

Thus the ADC section is rather simple. As the number of channels is so large, a similar method becomes necessary in the DAC section.

Another advantage over separate (one per channel) converters is that no individual zero and full-scale trimming is required.

Fig. 5 shows a simplified block diagram of the module. The multiplexing-demultiplexing functions are implemented with four 16-channels device (MOS type 4067 B). Channel selection is done through the address lines that cycle continuously over the 64 positions. Actually these lines are not common to the two boards, since different rates are required.

On the analog side the setting and sensing voltages are normalized in the 0÷10 V range. Therefore inputs and outputs are fully compatible: HV modules can be bypassed and testing procedures are made easier by means of a properly wired edge-connector card.

6.1. - ADC BOARD

The ADC converter (Fig. 5a) uses the well proved dual ramp technique. Most of the analog circuitry is contained into an MC1405 device, capable of working accurately at clock frequency near 1.5 MHz. Linearity is good but zero calibration is less stable than that quoted by the factory[5]. The digital subsection includes counters, timing and sign detection logic as well as an output shift register. A conversion cycle is initiated by a start pulse, causing a new channel address to be loaded into the address register. At the same time

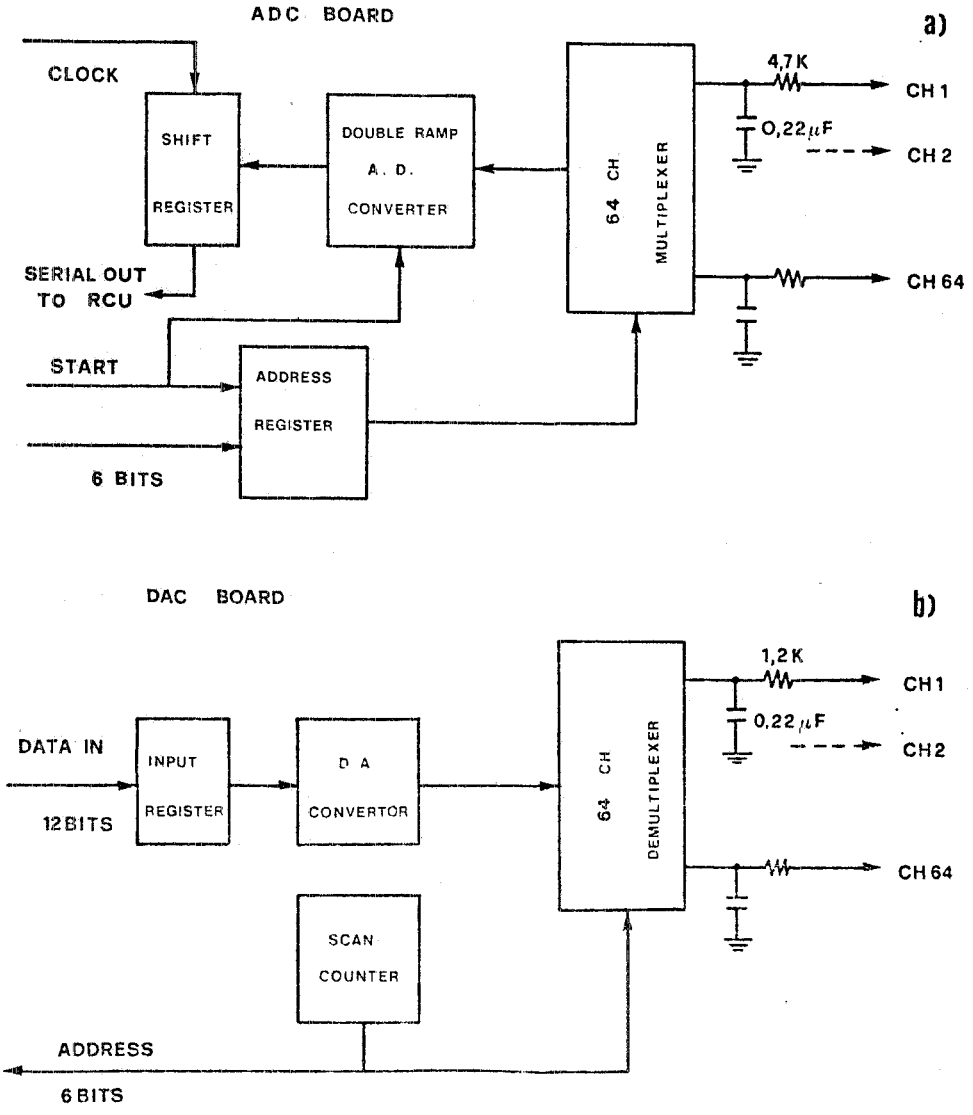

FIG. 5 Simplified block diagram of the Muntichannel Conversion System (MCS). ADC converter is shown in section a; DAC converter in section b.

the latest converted value is loaded into the shift register when it is ready to be serially output to RCU, in response to a clock signal. The maximum digital count is 3000, this occurring when the analog input is on its highest value. It yields the required 1 V resolution over a 3 KV range. Taking into account the clock frequency ($\simeq$ 1.5 MHz) and other delays, about 4 ms must be allotted to each conversion cycle. The time between successive readings at any channel is 250 ms which is adequate for a real time display of the high voltage.

6.2. - DAC BOARD

The operating principle of DAC board is shown in Fig. 5b.

A single 12 Bit DAC converter has the output voltage routed through the demultiplexer to 64 holding capacitors. This yields directly (whithout buffering) the signal programming the HV generators. The 64 analog memories must be periodically refreshed, even if the digital data are not changing. To comply with this fundamental requirement, a scan counter generates an address that controls the demultiplexer and the external RAM (in the RCU module) from which the data are taken; accordingly, no external logic is required. The operation of the system is actually more involved; in fact the converted data would not be accurate, as the capacitor looses charge during the time in which the channel is not selected. To minimize this effect the following technique exploits the bidirectional nature of the demultiplexer; the capacitor voltage is read at the beginning of each refresh operation. Generally this voltage will not be the correct one since load and stray currents are drawn continuously from the capacitor. Then an overcompensating charge is injected into it, proportional to the voltage error. This leaves the capacitor with a voltage error of nearly equal magnitude but opposite polarity.

The cycle is repeated for each channel. The net effect is that, while some ripple does occur at the output, the mean value is less affected by output loading. The ripple is then easily filtered out in the HV modules.

7. - HV GENERATOR

This unit houses 8 independent HV generators. Each one (Fig. 6) contains a DC-DC converter built around transitor Q3, transformer T1 and voltage doubler (D3, D4 and related capacitors). When Q3 is driven into saturation, the

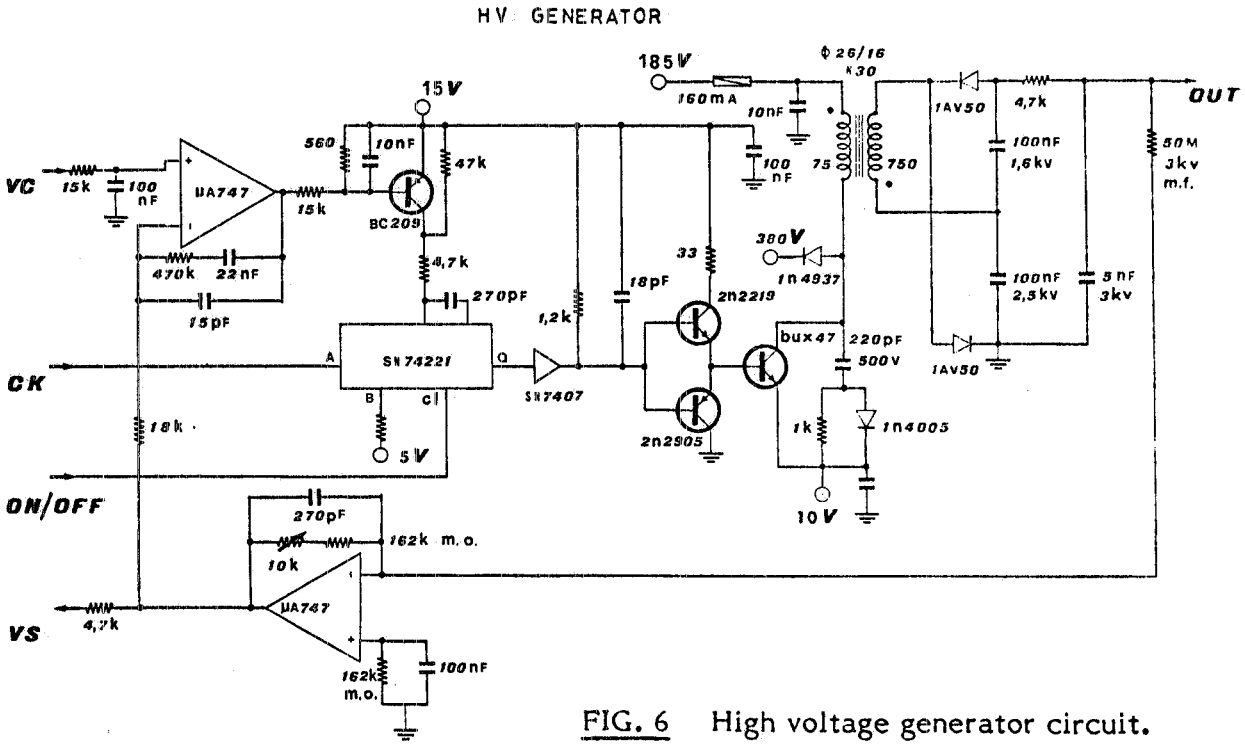

FIG. 6 High voltage generator circuit.

supply voltage (185 V) is applied to the primary winding of T1. The core magnetic energy is then transferred to the output, via D4, when Q3 opens. This is the "flyback" operating mode, but here it is somewhat modified by addition of the diode D3, giving rise to an asymmetric voltage doubler. The configuration shows good (≃ 75%) efficiency as well as simplicity.

The output power is modulated by varying the width of the pulse driving Q3 (from 0.45 to 4.5 μs). To this aim a monostable, externally triggered at a constant frequency (33 KHz), has its pulse-width controlled by transitor Q4.

The high-voltage resistor R6 is used to monitor the output voltage. Amplifier IC3 yields a scaled-down, buffered positive signal (VS), used by the MCS unit in read-out. In addition this signal is fed to the amplifier IC4, closing the feedback loop (with control input VC).

Some protective measures have been taken with respect to output overloads or short-circuitry, although no true current limitation is implemented. First, the switching transistor Q3 is oversized, and second, a fuse (F1) blowns after a sustained overload.

Each generator can be switched ON/OFF by an individual line, controlling the CLEAR input of the monostable. In addition a front-panel switch, with LED indicators, can turn off the whole unit.

Interchannel cross-talk effects have been virtually eliminated, by means of a shielded internal construction.

8. - CONTROL AND DISPLAY UNIT (CDU)

The CDU provides visual display and manual control capabilities. It can be used in three distinct modes:

1) Plugged into the HV crate (in a reserved location) to allow local dedicaded control.
2) As a remote system controller. The CDU is then plugged in a CAMAC crate (only for powering purpose). Communication occurs via 4 coaxial cables to RCU.
3) In the largest configuration, the CDU is an extention of MCU. One CDU is plugged into a CAMAC crate with one or several MCU, each one controlling a 64-channel system.

In any configuration, the user interacts with the system by selecting one channel through a set of thumbwheel switches; then the CDU displays:

1) The channel status, through LED indicators (OFF/ON under CAMAC control, ON under CDU control);
2) The set voltage value.
3) The voltage "error", that is the actual voltage reading minus the set voltage value (within the range -9 to +9 volts);

or optionally:

2) The actual voltage reading.
3) A two digits code specifying the physical location of the selected channel within the HV crate.

Pushbutton switches enable the user to change the channel status or set voltage value. This value can be incremented or decremented by an amount entered through a set of thumbwheel switches; a direct set operation is possible as well.

To facilitate the operator task, any command (except the direct set operation) can act on a group of channels at a time: specifically, from the first channel in the crate up to the one selected by the thumbwheel switches.

The CDU uses hardwired (TTL) logic; it features some diagnostic capabilities (loss of communication is signaled) as well as interlocks to prevent false operation.

9. - FINAL REMARKS

The system is presently operative in NA1 experiment at CERN, providing the HV supply of about 500 PMs.

The reproducibility at the output voltage setting is better than 0.1%. Output voltage stability under long time work condition is 0.05%.

Faults have been very rare. Particularly no faults occured for the power switching transistors (BUX 47, SESCOSEM) of the DC-DC converter.

We also used a mixed configuration by exchanging some high voltage modules with Light Diode Drivers[3] without any cross-talk problem.

ACKNOWLEDGEMENTS

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