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R. Baldini-Celio, F. Celani, F. Cirilli, A. Codino, F.L. Fabbri, P. Laurelli, G. Levy, G. Rivellini, L. Satta, P. Spillantini and A. Zallo: A VERY FAST PULSES PROGRAMMABLE GENERATOR WITH INJECTED CHARGE CONTROL.

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ABSTRACT

We decribe an eightfold module for generation of very fast pulses with calibrated charge output. Charge can be varied according to a programmed value with an overall accuracy better than 1%. The pulse width is in first approximation kept constant to 12 ns, while the output charge is controlled via a feedback acting on the voltage amplitude.

The programmable output charge varies from $\sim$ 100 pC to $\sim$ 8000 pC while the voltage, on 50Ω, ranges from $\sim$ -0.5 V to $\sim$ -55 V, with a rise time $\lesssim$ 1.4 ns and a fall time $\lesssim$ 3.4 ns. Frequency can be varied from 100 Hz to 33 kHz with an external or internal trigger. The time spread among channels is less than 200 psec. This generator is particularly suited for calibration with LED and firing LASER DIODE.

1. - INTRODUCTION

The linearity of the transferred charge versus pulse heigth is one of the main problems in generating very fast pulses. Actually the charge is a function of rise and fall time which, moreover, depend on the amplitude. Finally the charge linearity cannot be controlled at a level better than 10% using the pulse height as the only parameter.

Two standard methods are usually employed to generate ultra fast pulses, i.e. the technique of avalanche region transistors and the technique of mercury wetted relays with shaping line. Both methods are affected by severe limitations. Using avalanche transistor a tedious hardware selection in order to equalize pulse height is necessary. Moreover the pulse height control is achieved through complicated and expensive circuits which, generally, destroy the excellent rise time characteristics. The main drawbacks of mercury relay pulse generators are a low maximum rate ($\sim$100 HZ), a few millisecond time jitter between trigger and output and maintenance for its degradation.

A new circuit to solve these problems has been developed controlling the output charge by an automatic feedback on the integral value $\frac{V \cdot T}{R}$.

The main features of this circuit are: wide dynamic range, high frequency, constant delay from trigger time, nominally no maintenance requirement. This circuit has been developed for the test and calibration of PMs (via LED) in a wide angle e.m. shower detector installed in the NA1 experimental set-up presently running at CERN, searching for charmed mesons in photoproduction off nuclei[1]. The detector consists of segmented lead-scintillator sandwiches. Its main features are one thousand scintillator slabs (32 x 1200 x 10) mm^2 and nearly 400 PMs whose linearity has to be kept within 10%. The Led driver system for the control of this apparatus makes use of the same remote control via computer and data transmission system developed for the PM high voltage power supply[2]. In this way high voltage generators and LED drivers can be plugged in the same FRAM 77 CCL6400 crate without any cross-talk problem.

The new pulse generator circuit uses a VMOS, whose gate is driven by a transistor in avalanche region because of the large capacitance gate-source and gate-drain. A variable voltage with a very fast accurate sensing circuit ensures the constancy of the injected charge. The sensing circuit is a fast integrator with automatic reset, followed by a low leakage sample-hold memory. The output level of the sensing voltage in the sample hold-memory is compared with the chosen level. The output of the comparator makes VMOS drain voltage variable in order to close the feedback loop.

This circuit overcomes many drawbacks of standard techniques and achieves a linearity better that 1% between the output charge and the value chosen by the experimenter.

2. - CIRCUIT DESCRIPTION

Eight independent pulse generators are arranged on a standard CAMAC board, together with the timing and oscillating frequency control common sections. The scheme of each generator and the related control circuitry are respectively shown in Fig. 1 and 2.

Fig. 1 is composed of three main blocks: the power section, the injected charge sensing circuit and the drain's VMOS voltage modulator to obtaine the established charge at the power output.

The first block consists of IC6, Q4, Q2, Q3 transistors and related diodes and capacitors. As a signal generated in the main trigger arrives at the gate of 74s08, a positive output signal is applied at the base of Q4(2N2369) according to the ON/OFF switch. The voltage level at Q4 input is current amplified and the Q4 emitter pulse allows capacitor C25 to be loaded with a time constant adjusted by R30 potentiometer. The signal passing through R22 resistor goes to the base of Q2 (2N2222A MOTOROLA) working in avalanche region. The resistor R22 is used to decouple the emitter of Q4 from high voltage at base of Q2. The Zener diode D8 is used in order to help the VMOS internal zener in limiting the voltage to safety levels, taking also care of part of the power dissipation. Resistor R19 (56 Ω) prevents Q2 from autoscillating and guarantees its switching off. The pulse width at the output of Q2 is dominated by C7 capacitor in parallel to C8 to equalize different channels. The pulse height coming from Q2 is chopped to about 14 Volt by Zener diode D9 (ZPD12). The increase of two volts is caused by dynamic impedance of Zener diode. The voltage signal at gate of Q3 (VMOS VN 88AF) has a rise time less than 1 ns, typical of an avalanche transistor, with an amplitude less than 15 Volts (maximum voltage allowed between gate and source of VMOS) and a slew-rate current, just enough to load the large VMOS parasitic capacitance. In this condition the VMOS drain voltage decreases to the value determined by transistor Q1 and diode D6 to nominal zero volts. At the other end of the capacitor C9, placed at the output of the circuit, the voltage level decreases from 0 to $-(V_{Q1}+0.6)$ Volts. The resistor R26 (56 Ω) and inductor L1 (680 nH) have been used to generate a DC restore for pulse output. Some emphasis has to be devoted to the circuit which drives VMOS gate for its simplicity and low cost. Generally, to get the highest speed, expensive STEP RECOVERY

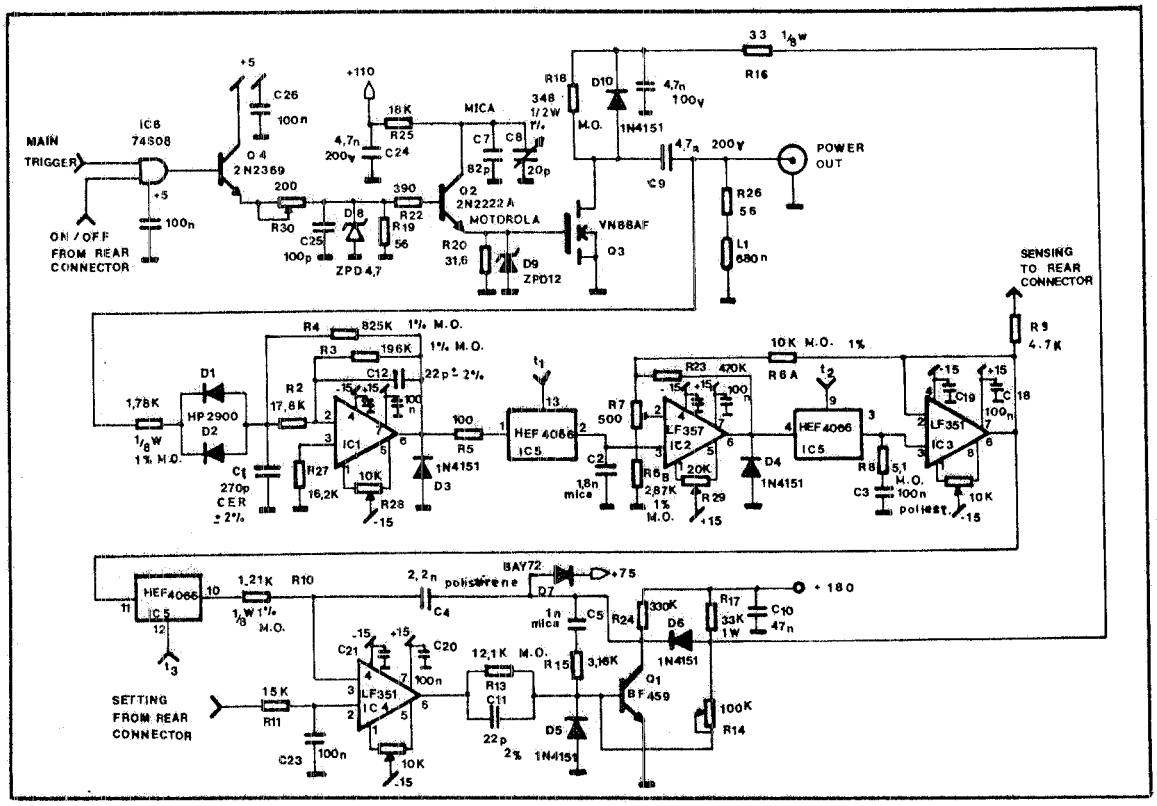

FIG. 1 - Circuit of one channel.

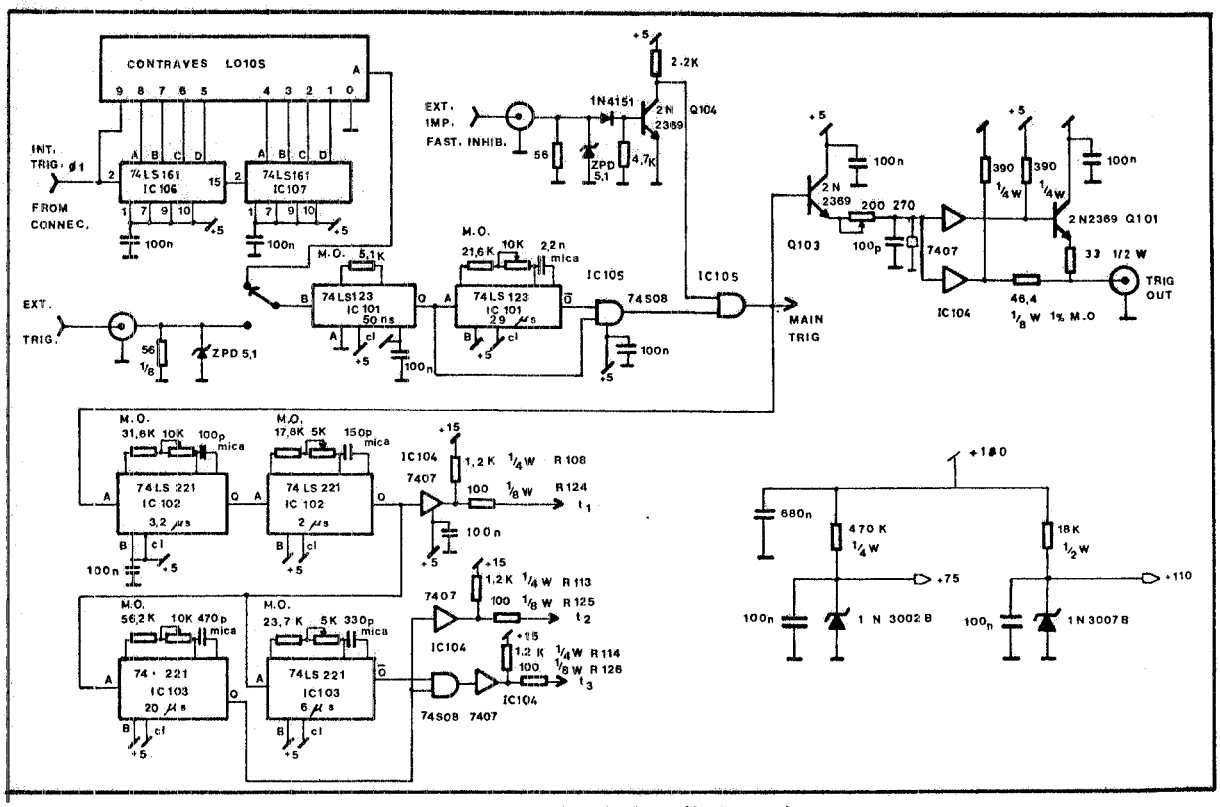

FIG. 2 - Common circuit for all channels.

DIODES driven by microwave transistors shoud be used.

The injected charge sensing circuit consists of hot-carrier diodes D1, D2 (HP 2900), BI-FET operational amplifier IC1 (LF351), IC2 (LF357), IC3 (LF351) and LOCMOS analog gates IC5 (HEF4066) with related diodes, capacitors and resistors.

The circuit block composed by D1, D2, C1 is a high speed integrator of the signal coming from C9. The voltage level on C1 is amplified, inverted and transferred to the IC1 output. When the pulse amplitude coming from IC1 reaches the maximum value, 3.2 μs after the main trigger start, the IC5 gate is opened during 2μs by the control signal indicated as t_1. The top value of the signal from IC1 is thus transformed into a D.C. level at the end of C2 which is the "signal" section of the sample-hold memory circuit. After the capacitor C2 has been loaded the gate of the second section of IC5 is opened for 20 μs by the signal t_2. The voltage level of C2 is furthermore amplified by the high slew-rate BI-FET operational amplifier IC2 and transferred to the large capacitor C3 which is the real holding capacitor of analogic memory. This voltage level is put in a buffer by IC3, transferred by resistor (R9) to the sensing line of the channel and applied to the third GATE IC5. In the third section of the circuit the voltage level at the output of the analog gate is compared by resistor R10 (used for decoupling, safety and filtering) with the positive DC level arising from setting line at the rear connector. The comparison is performed by IC4, a BI-FET, operational amplifier (LF 351). The output of IC4 drives the base of the high frequency power transistor Q1 (BF 459). The modulation of Q1 base varies the voltage to the ends of Q3 closing the feed-back loop. The potentiometer R14 between base and collector of Q1 determines the maximum voltage value for the output of the VMOS. In fact, at low trigger frequency, the feedback loop has large leakage and in the event of a single pulse the voltage across the VMOS could reach 75 V.

The part of the circuit common to the generator is divided into three blocks (Fig. 2). The first block is an interface consisting in a manually selectable divider of the internal clock (IC106, IC107); a safety circuit for trigger frequency larger than 33 KHz (IC101, 1C105); a constant amplitude and width pulse generator for the external trigger (Q3, IC104, Q101); a fast inhibit circuit for the external and internal trigger (Q104, IC105).

The second block contains circuitry for the generation of the three clock times t_1, t_2, t_3 used to open the analog gate of IC5 and the driving circuit for its digital input. It has to be noted that apart from the usual pull-up resistors (R108, R113, R114) of the open collector IC104 (SN7407) the circuit contains also resistors (R124, R125, R126) between the IC104 output and the digital input of IC5 in order to lower commutation spike effects determined by the low OFF impedance of 7407 up on LOCMOS.

In the third part two voltage levels are generated. The first one provides power to the avalanche transistor (110 Volts), the second one limits the drain voltage of the VMOS to 75 V.

3. - PERFORMANCES

The described module generates negative pulses variable from $\sim$ -0.5 V to $\sim$ -55 V on 50 Ω impedance with an overall width of 12 ns, a fall time $t_f \leq$ 3.5 ns and a rise time $t_r \leq$ 1.4 ns. Measurements on output charge stability versus frequency (100 Hz + 33 KHz), temperature (+10° to +40°C) and charge ($\sim$ 100 pC to $\simeq$ 80000 pC) result in better than 1% over the dynamical ranges. The delay between the rise of the input trigger and the start of power output can be chosen via hardware by a potentiometer ranging from 50 ns to 70 ns with an accurancy of 200 ps. The module is provided with an output trigger with TTL level on 50Ω with an accuracy of 1 ns and a constant width of 50 ns for synchronization purpose and with a fast inhibit input, also TTL level on 50 Ω. The module can work with an internal trigger which is selected in frequency up to 33 KHz (nine step*) or

*) $\nu = \nu \max \frac{1}{2^n}$; n = 0,1,2...8.

alternatively with an external trigger selected by a switch on the panel. A safety circuit protects it against higher frequency triggers.

This pulse generator is compatible with the power supply and control system of the PM "FRAM 77 programmable HV system"[2] used in the above mentioned NA1 experiment. It may be plugged in the CCL 6400 crate which usually allocates HV modules for PMs and takes use of the same facilities provided by this system. The FRAM 77 crate controls a large number (64) of channels transferring information among modules in the same crate and performing the digital to analog conversion functions and viceversa, and the CAMAC interface to the computer.

4. - CONCLUSIONS

The generator of very fast pulse described in this paper has the new feature of using charge control. Due to its characteristic it offers

a) wide dynamic range of power output (from about -0.5 V to about -55 V on 50 Ω)
b) very fast and nearly constant rise time (about 1.4 ns)
c) constant, short (60 ns) and accurate (200 ps) delay time from trigger to power out firing
d) constant over-all width (12 ns)
e) large dynamic range of trigger frequency (from about 100 HZ to about 33 KHz)
f) possibility of complete and remote control

it can be profitably used not only to drive LEDS, for which this generator was originally designed, but also for LASER DIODE firing, for any experimental apparatus requiring very accurate timing and finally in all those applications which require remote control.

ACKNOWLEDGEMENTS

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(2) Report LNF-77/36 (1977).