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A. Marini, F. Ronga and M. Spinetti: A MULTIPROCESSOR BASED SCHEME FOR DATA ACQUISITION AND ANALYSIS.

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1. - INTRODUCTION.

Two important aspects in computer system design must be outlined. First, even extrapolating the time performances of the present processors, there is a physical bound connected to signal propagation velocity and second, the rapid progress on medium and large scale integration (MSI/LSI) in semiconductor technology makes available inexpensive small size processors. Nevertheless rapid and continuing advances in high energy physics instrumentation and growth of data flow from experimental apparata lead to a situation in which the processing resources of a standard on-line computer will be soon satured.

In this framework the multiple-processor approach seems to be a suitable trend to speed up the time performances of a computer system in the environment of a high energy experiment.

In this paper, after a brief overview of the multiprocessor systems, we propose the use of a multiminiprocessor now commercially available in alternative to the standard mini-maxi computer network.

2. - MULTIPROCESSOR SYSTEMS: A BRIEF OVERVIEW(1).

Three types of interconnection between sets of processors are commonly known: computer networks, multiple ALU processors and multiple-processors systems. In the last form of organization a set of independent processors share a common memory under integrated control (Fig. 1). Processor coupling further distinguishes multiprocessor systems: processors which interact at subinstruction or instruction level are usually referred to as tightly coupled and processors which interact at no lower than the task level can be referred to as loosely coupled.

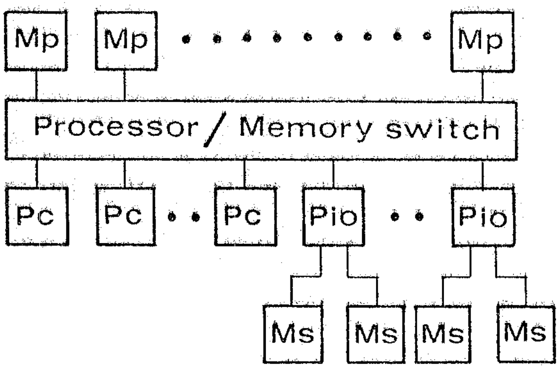

FIG. 1 - Structure of a Multiprocessor (from ref. 1a). Pc: central processor; Pio: input-output processor; Mp: primary memory; Ms: secondary memory.

There are some important figures of merit for the multiprocessor system in comparison with the uniprocessors :

- the (processor-to-memory bandwidth)/cost ratio could be improved owing to the impact of the new technologies on small size processors ;
- the modularity of the organization is the natural framework for parallel processing and has direct effects on system expansion and maintenance ;
- the system reliability is improved by several cooperating processors : fault tolerance internal logic can lead to a reconfiguration of the system without serious degradation of the performances.

The effectiveness of the processor-processor and memory-processor interconnections, the arbitration of the resources among different processors and the utilization of suitable software structures are some important aspects in multiprocessor system design.

In the past years a reasonable number of multiprocessor systems based on processors of mini/micro/computer size have been designed, but not many are commercially available.

An interesting application of multiprocessors can be identified in high energy experimental physics field. Laboratories and Institutions have developed studies on general purpose multiprocessors, like SEM(2) and MUMIE(3), for data acquisition and analysis aims. More precisely, specific tasks in these systems are raw data acquisition, filtering, data reduction, etc.

In the next Sections we suggest the use of a working multiminiprocessor commercially available and we give some general outline for the implementation of a data acquisition and analysis system. The application fields of such a multiprocessor are multiple (pattern and speech recognition, real-time process controls, etc.) and it is employed in configurations of about one hundred cooperating processors.

3. - EMMA SYSTEM(4).

EMMA is a general purpose multi mini-processor with no upper bound in the expansion of the processors and memories.

Main features of EMMA are : complete hardware-software modularity and flexibility, architecture oriented toward hardware-software structured design, fault tolerance and possibility of self-reconfiguration.

Three basic functional modules are the EMMA constituents : miniprocessors (UA's -associative units), memory modules (ME's) and data exchange coordinators (DEC's).

The "family" is the structural element of the EMMA system. From a hardware point of view (Fig. 2) the family is a monobus controlled by a DEC. On this monobus up to 128 UA's and a maximum of 4 Mbytes of memory (16 bits/word) can be allocated. In each monobus DEC manages interprocessor communications and connects monobusses with each other when information exchanges between different families are requested. Protocols for priorities and rates of data transmission are software defined. The instruction set supported by each UA is enriched by special instructions voted to fast associative search on memory : this makes EMMA particularly sui-

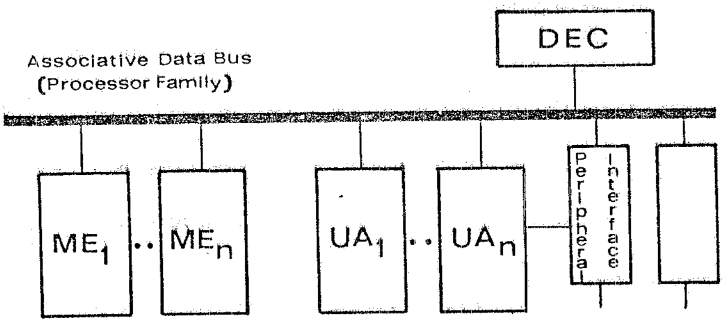

FIG. 2 - Hardware structure of an EMMA family (from ref. 4b).

table for pattern recognition aims. Each UA has its own memory of 4 Kwords size (16 Kwords in the future). Process peripherals (e. g. CAMAC system) can be connected to a specific processor or to the monobus. From a software point of view the family is one of the sets of tasks (family task) in which the global process can be expanded. A proper shape of the family task leads to a situation in which the data exchange is almost confined in each monobus in order to optimize the interprocessor communication capability. The number of AU's and ME's in a family is tailored to the consistence of the family task.

A minicomputer, the MONITOR, is the vertex of the structure, performes system service functions and manages standard peripherals ; according to the temporary needs of computing resources, the MONITOR can also change the configuration of a family.

This organization leads to a hierarchical architecture in the EMMA system : processors are placed at lower levels and families are found at higher levels (Fig. 3). The system expansion is oriented to modular multiprogramming, that can be worked out by high level languages as Concurrent Pascal.

In each family, diagnostic functions performe on-line maintenance to minimize the loss of computing power due to hardware failure. There are two possibilities connected to the detection of an error: an internal logic provides the recovery of a temporary error, or a self-reconfiguration is possible and the faulty module is removed, if a permanent error is detected.

Due to the high computing power, EMMA has been successfully employed in OCR (Optical Character Recognition) systems installed by the French and Italian Post Departments for automatic postal address recognition. In these high reliability systems up to 70 UA's have been involved. The raw data flow is 80 Mbits/sec. and 20 hand-written postal addresses are recognized in one second. This performance has been obtained using a "front-end" family of 20 UA's. This means that each UA could absorb an input data flow of 4 Mbits/sec, a typical rate of the CAMAC, and moreover some simple operation on data is possible ; for comparison the expected data flow for a large experiment on the p-$\bar{p}$ collider is 100 Mbits//sec$^{(5)}$.

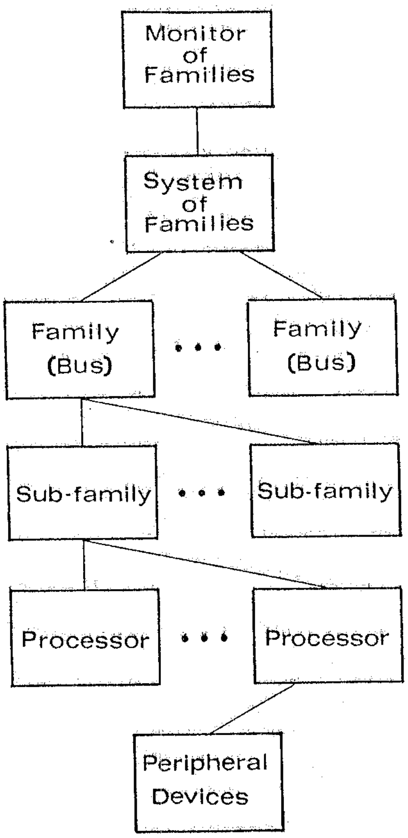

FIG. 3 - EMMA hierarchical structure (from ref. 4b).

4. - A POSSIBLE DATA ACQUISITION AND ANALYSIS SCHEME FOR THE EMMA SYSTEM.

Starting from EMMA features we can suggest some simple and flexible schemes for the use of the EMMA system in the environment of high-energy experiment.

As a first step we must separate the global process in many parallel or logically independent tasks. We list here a set of possible tasks :

a) data acquisition with a small amount of data reduction ;
b) fast filtering and background rejection ;
c) pattern recognition (or slow filtering) ;
d) event analysis ;
e) data formatting and recording on mass storage ;
f) apparatus control and monitoring.

For each of the previous tasks a family could be properly planned in EMMA. In each family a suitable number of UA's should concurrently execute the family task on the event data with the purpose of optimizing the family troughput. Each event flows from a family into the next according to a pipe-line scheme. Due to this type of organization, at each stage event processing attains a degree of accuracy depending on the number of UA's involved by the family.

We have two possible schemes for the data acquisition task. A first scheme implies that all the data of an event are transferred to the ME modules by autonomous intelligent crate controllers and then each UA can have access to its own part of the buffered event. A second scheme seems to be more promising because the limitations of the CAMAC data transfer rate could be easily overcome. The digitized informations coming from the different elements of the apparatus can be suddivided and sent directly to the individual input port of the UA's, so that data belonging to an event can be read in parallel in a time which becomes shorter increasing the number of UA's involved. The processing power of the family can also be used to make a small amount of data reduction (e.g. linear transformations on data) and to structure the data in a suitable way to minimize the time of sorting operations during the next phases of the analysis.

For the efficiency of the on-line fast filter it is important that the system is capable of rejecting undesiderable events in the shortest possible time. Namely the increasing selectivity of the filter is related to the time necessary to take the decision. So, in general, numerical calculations must be performed with a rather low precision and moreover the application of tests which have an increasing selectivity power is recommended. Many of these decisional tests could be made in parallel on the different elements of the apparatus. For example simple tests could involve ADC contents and a higher level test could be based on simple track-finding algorithms. Due to the high degree of parallelism that the family can developed, the total time for event filtering could be kept not far from the characteristic time needed to a hardware processor, 25 μsec(6), and certainly shorter than the typical time of a minicomputer, 5 msec(7).

The purpose of the pattern recognition (or slow filtering) family is the full and accurate reconstruction of the events (selection of track candidates, geometrical reconstruction, vertex definitions). EMMA has ad hoc instructions for this aim. Output of this task could be momemntum, beta, dE/dx, etc. for charged tracks, and energy flow for hadronic and electromagnetic showers.

Using this information the kinematical fitting and the full event analysis for the classification of the topologies are possible.

At each stage of this data processing a data permanent recording is possible if desired. Of course the results of the full event analysis together with the experimental raw data are the most useful recording.

Purpose of the control task is the periodic measurement of the apparatus element efficiencies either on-line using the information carried by sets of fully processed events or off-line by simulating physical processes (for example fiducial pulsing the chambers, LED pulsing the scintillators, etc.). Other tasks of this family are the on-line event data display, the log-booking of the runs and the machine conditions, hardware setting and calibrations.

Although at this level it is difficult to give a more detailed configuration of the whole system, an EMMA structure with about one hundred UA's can reasonably face all the previously described task according to the input data rate. We believe that the use of multiprocessors is a very promising way: the outlined system offers the typical flexibility of a software programmed system, the computing of a large computer and nevertheless it can approach the time performances of the specialized and hardwired systems, used now and in the next future, in the high energy large experiments.

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