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AN AUTONOMOUS CAMAC CRATE CONTROLLER FOR SEQUENTIAL OPERATIONS

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A CAMAC controller especially built for sequential reading, elaborating, storing, and visualizing data on film by the use of displays is described. The special crate controller performs the role of both crate controller, branch driver and computer.

1. Introduction

We describe an experimental apparatus, which was built at the Laboratori Nazionali di Frascati and used by the MEA group in the counting room of ADONE. This apparatus allows us to realize a system for acquisition, elaboration, temporary storage, re-input and permanent storage of the data on photographic film.

In our particular experiment the apparatus substitutes completely both crate controller, branch driver, and computer. The apparatus consists essentially of a "control unit" which gives the suitable commands of acquisition and re-input data, an "elaboration unit" which elaborates the acquired data, a "memory block" (with registers) which stresses temporarily the elaborated data before the final output on the writing lines (W) for loading of the output registers.

2. Logical sequence of the operations performed

The CAMAC equipment with which the system exchanges information consists of:

a) 4 pattern units,
b) 4 analog-to-digital converters (ADCs),
c) 8 output registers.

The fixed logical sequence of the operations performed by the system is:

1) sending the "read" commands in order to acquire the data from pattern units and ADCs;
2) elaboration and storage of acquired data;
3) sending "write" commands in order to output the data previously elaborated and loaded to the output registers;
4) synchronous ignition of all the Nixie displays controlled by the output registers when these have been loaded.
5) permanent storage on film of the display bank.

3. Block diagram

The block diagram in fig. 1 describes the controller. The signal "EVENTO" which is delayed by 130 μs in order to prevent the upsets caused by "discharge" of the spark chambers in the operative room of ADONE initializes the equipment. After a 130 μs delay a one-shot clears and presets the apparatus.

The end of the previous signal controls a flip-flop whose output "sets free" a "gated clock", which together with the circuit "SHAPER" brings the timing in accordance with the CAMAC requests.

A synchronous counter (1–16) counts the pulses of the gated clock. Its four outputs A, B, C, D control the DEMULTIPLEXER (1/16 outputs). These sixteen outputs of the demultiplexer, grouped four by four, gating proper flip-flops and gates, cause the functions of read or write and the strobes S 1 and S 2. The subaddresses A1 and $\overline{A1}$ are also set up in order to select among two sections of each OR. Also the station number is set up. This selection of the module is performed with the assistance of both a 1–4 counter (triggered by the output ripple clock of the synchronous counter 1–16) and of a block decoding the number counted by the asynchronous 1–4 counter. As soon as the writing into the last of the ORs is accomplished, a GATE circuit acknowledges inlet of this situation and stops the system.

In the elaboration process the data coming from pattern units are inverted before the loading into the output registers; the data coming from the ADCs are first inverted and then converted from binary to BCD-code.

The recording of the data was done using D flip-flops organized in a 16-bit register according to the greatest capacity of the patterns. The clock pulse for the registers coincides with the S 1 strobe that occurs during the reading, specified in the diagram by S 1 R.

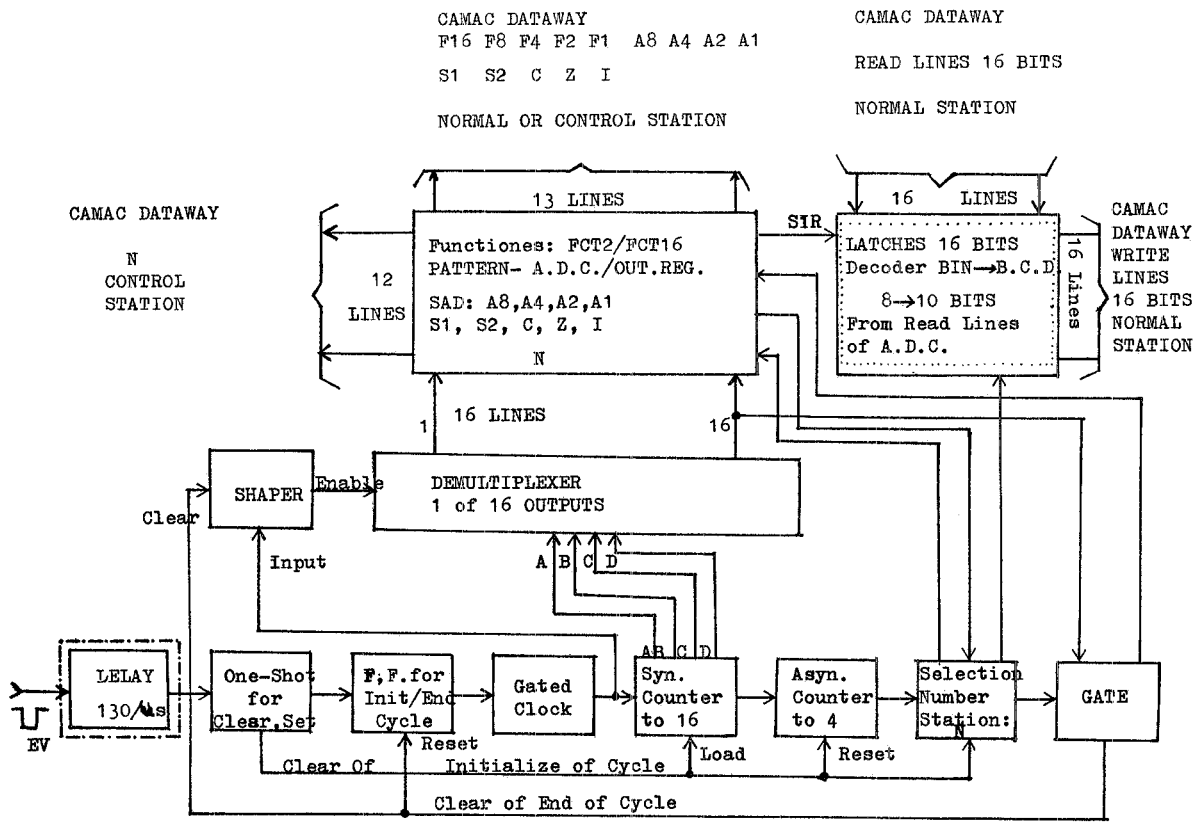

Fig. 1. Block diagram of the controller.

4. Further developments

The system was designed to be very flexible and extendible. In the block diagram (fig. 1) the elements needed to adjust the system to the wishes of the MEA Group, i.e. input- and output-conditions are shown with representation –·– and ···. An increase in the number of modules with which exchange of information is possible can be made by:

a) Altering the reset of the asynchronous 1–4 counter. For every increment of the previous reset it is possible to task with two modules in read mode and two modules in write mode.

b) Using the next outputs of the circuit "Selection Number Station: N".

In order to change the elaboration process it is necessary to replace the elaboration module (the code converter of binary into BCD). For this purpose we have made the period of the strobe (decided from the "SHAPER" circuit) 600 ns followed by 600 ns of "dead time".

In order to change the functions it is necessary to add other proper F.F.s and Gates to the first outputs of every group of 4-outputs of the demultiplexer's 1/16 outputs.