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HIGH VOLTAGE PARTITIONING FOR PHOTOMULTIPLIER PARTICLE DETECTORS

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A manual and computer controlled system to vary independently the high voltage supply of a set of 100 photo multipliers inserted in an experimental apparatus for high energy physics research is described.

1. Introduction

Photomultiplier detectors show, as is well known, a very large spread of output pulse characteristics vs high voltage supply in the linear region of pulse amplitude and timing. The power supply for each P. M. must be carefully chosen to obtain large ranges of proportional dynode-multiplication and to avoid, at the same time, large spreading of the overall delay to the last dynode.

Sometimes it is possible to arrange measurements within limited amplitude ranges and, disregarding timing, to fit with appropriate attention the magnitude of pulses to the measuring instrumentation dynamics.

Anyway this technique cannot be applied extensively as it is successful only after criticism. A general way to follow is to choose each voltage supply and, after measurements, to determine optical values with a cut-and-try method. It seems not to be easy to find the final voltage configuration when the number of P.M.s is over, e.g., ten.

Modern experimental features use thousands of P.M. detectors and the problem would have no solution if a hv partitioning system, controlled by a computer, could not be applied.

This article describes a system in use in the National Laboratories of Frascati and experienced over about one hundred channels of hv supply.

2. Principle of operation of the system

The hv partitioning is obtained by a variable-position, manual or computer controlled sliding contact, each position corresponding to a different voltage in a defined range over a booster high voltage pedestal. For the application of the P.M. detectors we chose a fixed hv pedestal adjusted, for once, between 1.800 and 2.200 V, and a contact comb providing 32 positions, each one of them differing 20 V, or 10 V. This means that we can choose a hv supply for the P.M. detectors ranging from 2.200 to 2.840 V or 1.800 to 2.440 V or, if half-dynamic of the steps is requested, from 2.200 to 2.500 V or 1.800 to 2.120 V. Any other discrete values between these ranges can be obtained by varying the booster hv value.

The 32 different voltages are obtained by busing the output of a 33-terminal (32 hv plus ground) power supply able to handle on each terminal the current of a very high number (100) of independent P.M.s.

The unique power supply can be designed with over-voltage and over-current protections on any single output bus, saving cost and substantially increasing reliability. The lower voltage of the chain (first step or step "0" on the contact comb) corresponds to the hv booster ranging, as we said, from 1.800 to 2.200 V.

All the static contacts (32) are engraved on a printed circuit board equipped with an AMP MODU 32 contact connector, plugged into the hv bus, supplied from a rear support panel, actually a large printed circuit board insulated from the chassis and designed just for busing the hv to any single partitioning set.

The hv sliding contact is driven back and forth on a yoke moved by a dc motor coupled with a worm screw nut system. On the yoke there are also the five contacts for position control whose static contacts, Gray-coded over 5 bits, are engraved on the same P. C. board bearing the static hv contacts. Moreover one sliding contact on the yoke provides the exact centering of the sliding hv contact on the single static hv contact reducing position backlash in moving.

To reduce backlash due to mechanical inertia of the moving parts, the dc motor which drives the yoke is short-circuited when the centering contact is reached. The centering contact comb (one contact for each one of the 32) really acts as a bit-more in the code, enabling the comparison every time a position is attained, independently from the direction of moving.

The P.C. board picture is in fig. 1 and in fig. 2 the whole system described is shown.

3. Control circuit schematic

By "manual control" it is possible to select the position on a two decade rotary-switch whose output is coded as an inverted BCD code. The output signal wires are pulled up through a resistor network in a dual-in-line case. TTL code converter from BCD to binary SN74183 is used to supply the signal inputs A to a 5-bit binary comparator 9324 as shown in the schematic (fig. 3).

The five input bits of the Gray code G_0–G_4 are considered true when zero.

They are sent, after inversion, to a Gray-to-binary EXOR gate SN7486, following the code conversion logic:

$$B_i = G_{i+1} \oplus G_i,$$

$$B_n = G_n, \qquad i = 0, 1, \ldots, n-1.$$

The B are supplied as inputs B to the 9324 5-bit comparator that is enabled only when the centering comb fiducials are reached insuring the overlapping of the hv sliding contact on the hv static contact on the P.C. board, as explained before. The directional movement is controlled through two set–reset flip-flops formed by transistors T_2T_3 and T_4T_5 and relais R_2 and R_1 respectively. Set pulses are sent as "1" logical level (high) to the base of transistors T_3 and T_4; when excited, the relais R_2 and R_1 actuate a holding contact keeping the ON state of the flip-flop: reset pulses are sent as zero level to the base of transistors T_2 and T_5 releasing consequently the holding contacts. The bases of transistors T_2 and T_5 are biased through open-collector high voltage inverter (SN7406) whose input is logical "1" level.

The switching contacts of relais R_1 and R_2 realize the following functions:

R_1 CR_{11} normal free,
excited holds the coil of relais R_1 excited to ground,
CR_{12} normal supplies -5 V to the motor through CR_{22} to move it in the back direction,

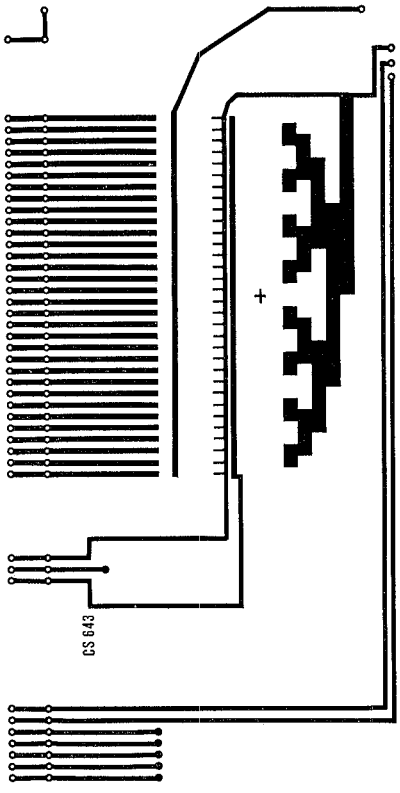

Fig. 1. Printed circuit board with hv comb and Gray code control contacts.

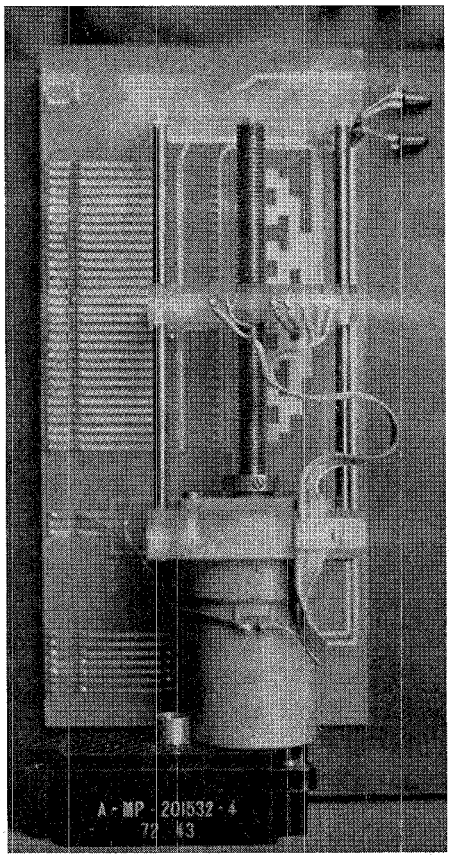

Fig. 2. Motor driving set mounted on the P.C. board of fig. 1,

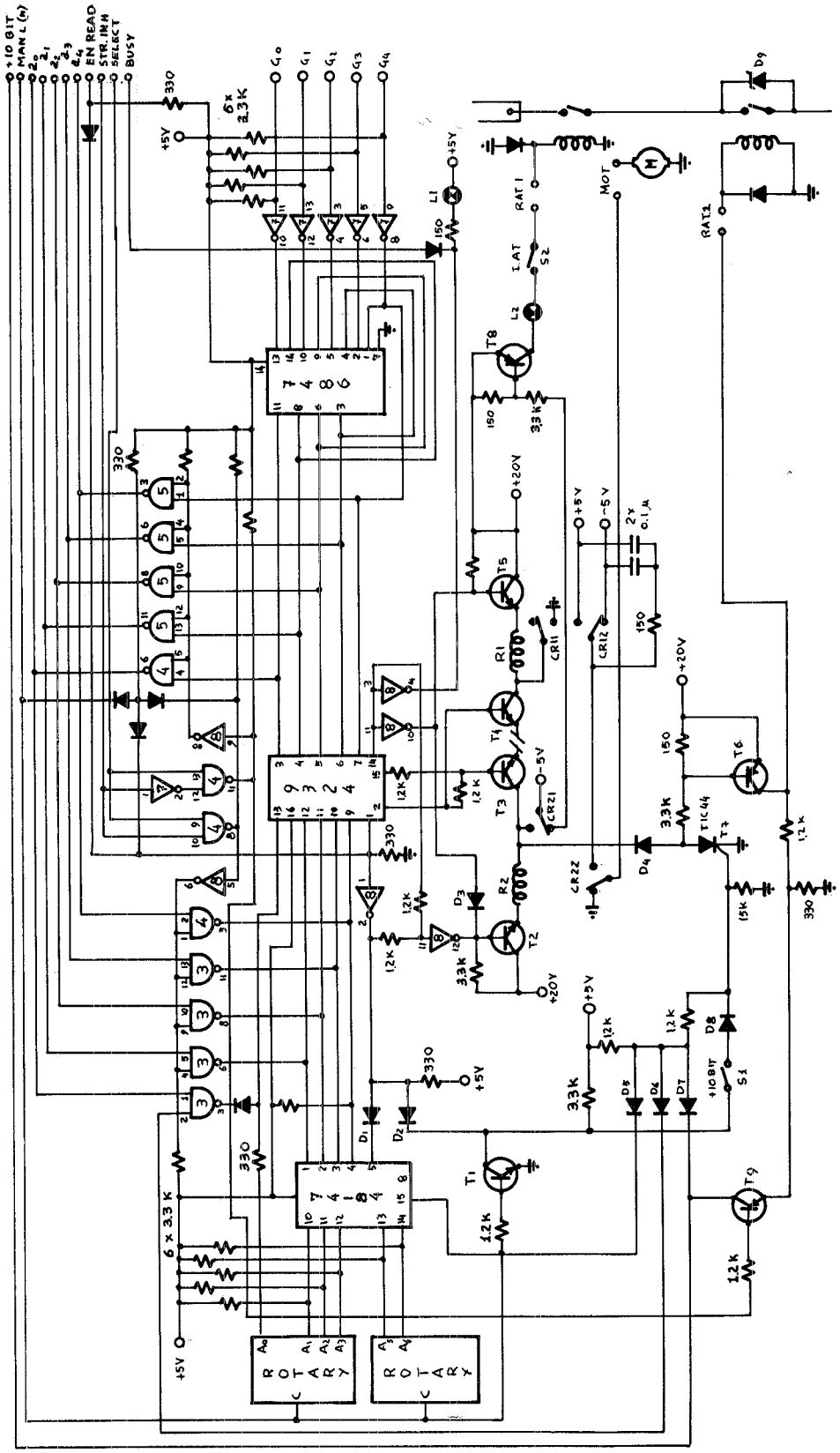

Fig. 3. Schematic of the control logic and interfacing with the device UNIBUS.

excited supplies +5 V to the motor through CR_{22} to move it in the forward direction;

R_2 CR_{21} normal applies −5 V to the base of T_8 exciting the hv relais $R_{at\,1}$ if S_2 hv is switched on from the front panel and connects the selected hv to the supply line of the P.M.,

excited holds the coil of relais R_3 excited to −5 V and releases SCR T_7 (TIC44) that, through transistor T_6 and hv relais $R_{at\,2}$, shorts the series 10 V zener D_9 on the hv supply line of the P.M.,

CR_{22} normal shorts the supply line of the motor to ground thus realizing its magnetic braking,

excited transmits the supply voltages +5 V or −5 V selected by the state of the relais R_1 (contact CR_{12}) to the motor actuating motion in the two directions.

When the 5-bit comparator 9324 discovers $A=B$ (selected position reached) its pin 14 is brought high, releasing, through gate 8 (11, 10), the relais R_1 and via an OR resistive function to the input of gate 8 (13, 12) the relais R_2. Thus after $A=B$ everything is at rest.

When the rotary request is such that $A>B$ or $A<B$ ($A\neq B$) the relais R_2 is esxcited and the motor is supplied. Only if $A<B$, also R_1 is excited and CR_{12} changes the motor supply to +5 V reversing its motion.

The 32 positions of the rotary switches are binary converted by the SN74184N through numbers 0–31. When the fifth bit (≥ 32), pin number 5, goes high (on 32–39 position requests from the rotary-switches) diode D_1 results in being inversely biased: the anode of diode D_1 and diode D_2 connected to the inverter T_1 of the MANUAL signal (MAN) become active when low, and the output of open-collector inverter 8 (1,2) of the enabling signal (EN9324) applied to the 9324 comparator (pin 1), are wire-ORed. At the output of gate 8(1,2) the following logical relation is performed:

$$\text{OUT}(8(1,2)) = \overline{\text{MAN}}\ (\geqslant 32)\ (\overline{\text{EN9324}}).$$

When such a relation is satisfied, the flip-flop relais are reset through gate 8(11, 12) whose output goes low driving directly the reset base of transistor T_2 and through the diode D_3 the reset base of transistor T_5. Thus the motor is stopped on the next position after the incorrect position request.

The EN9324 signal results as in the following:

1) When the whole apparatus is not under (manual or computer) control the 9324 must not take any decision, that is EN9324 must be high. The computer control is effective if the SELECT (SEL) signal, actuating one circuit on the strip bearing 8 different control circuits, is high, "and" the general signal of actuation STROBE IN (STR IN) is also high (see section 4).
2) If condition (1) is not verified the 9324 must take a decision only if the sliding contact for centering the hv contact (EN LETT signal) is active, that is low ($\overline{\text{EN LETT}}$ active).

From these considerations the following logical relation results (fig. 4):

$$\overline{\text{EN9324}} = \overline{\text{EN LETT}}\cdot\overline{\text{MAN}} + \text{SEL}(\text{STR IN}).$$

The choice of the value of the voltage step to 10 V or 20 V is obtained by short-circuiting a 10 V zener D_9 in series with the hv supplying line of the P.M.

The manual control is enabled through diode D_8 only when the collector of T_1 is high, that is the line-enabling manual operation (MAN) is low.

When TIC44 SCR (T_7) is fired closing switch S_1, T_6 saturates carrying current through the coil of relais $R_{at\,2}$ whose contact is normally open: the steps of the hv supply on the sliding contacts are kept unaltered (t.i. equal to 20 V): if S_1 remains open, the hv on the supply line is 10 V less than that on the sliding contact.

Any time that the relais R_2 is excited (i.e. the motor moves changing position) SCR T_7 is open through diode D_4 whose cathode applies −5 V to the anode of T_7.

The insertion of D_9 is controlled by the +10 BIT line that must go high to short diode D_9 (steps equal to 20 V). In fact the output of the enabling gate formed by diodes D_5, D_6, D_7, goes high firing T_7 if, respectively, MAN line is high and the channel is selected by the computer address (SELECT signal) and actuated through the STROBE IN signal.

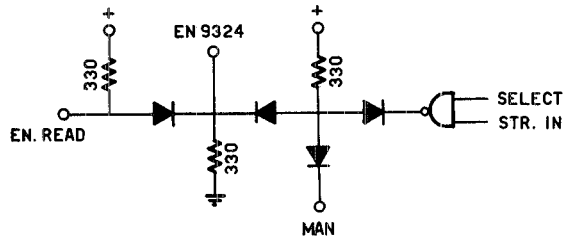

Fig. 4. Schematic of the logic concerning the comparator 9324 enabling (extracted from schematic of fig. 3).

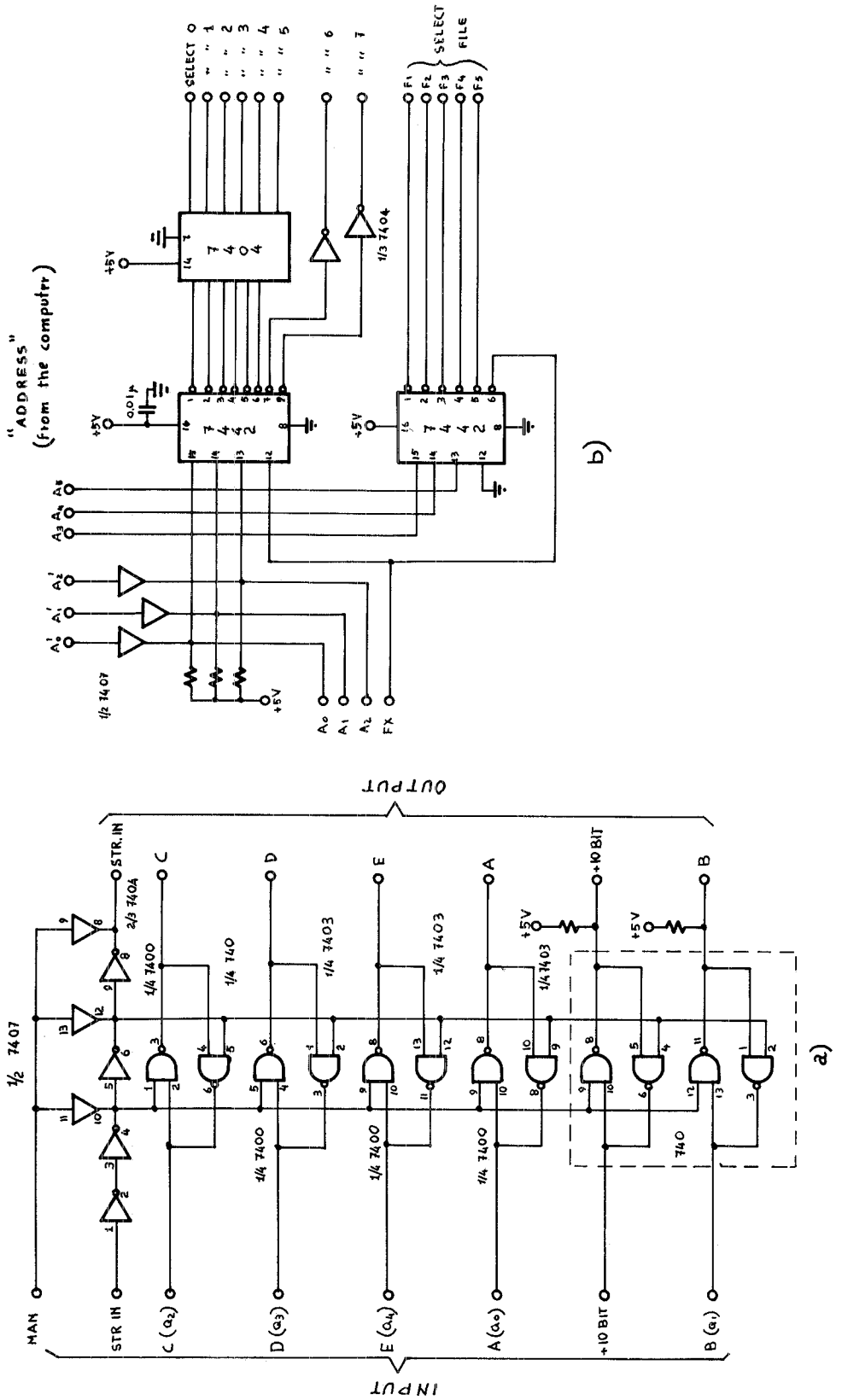

Fig. 5. Schematic of the buffering and addressing for eight channels.

TABLE 1

Summary of operations supervised by the two signals STR IN and SELECT.

STR IN	SELECT	Operation performed		
		read	write	other
0	0	NO	NO	to rest on the last position
0	1	YES	NO	to read binary the last position
1	0	NO	NO	to rest on the last required position
1	1	NO	YES	to set new inputs to the 9324 till a "0" level is set on the BUSY line when position is reached

When the 9324 comparator input bits A and B are identical (pin $A=B$ is high) the lamp L_1 is lighted on the panel indicating that the requested position is reached. Lamp L_2, when lighted, indicates that the switch S_2 has been closed, i.e. the hv supply line is "on".

4. Omnibus interconnecting wiring

The computer signals are transmitted to the single control circuit through an omnibus wiring including:

a) a_0 through a_4 lines: data lines for reading and writing the position of the sliding contact, i.e. for setting the value of the hv on a single P.M.,

b) +10 BIT data line: to establish the value of the step (20 V if "high", 10 V if "low"),

c) SELECT control line: to select the single control circuit within a strip (row), when the row itself is selected by appropriate address of the computer,

d) STR IN control: to give generally the command of actuating the request of "writing and go" if high or "reading" the position if low,

e) BUSY line: an answer line remaining high if the new position is not reached: it is permanently low when the device is at rest in the last required position. This line on each control circuit is "ORed" with the $n-1$ lines of the other $n-1$ devices (channels) enabling a channel at a time to be serviced under computer control.

The two control lines, SELECT and STR IN, supervise all the operations of information flow between the device and the computer. The logic decisions in which they are concerned are described in table 1.

The busy line gives an answer from the device considered as whole set, whether the computer is allowed or not to interact with the device, reading positions, changing the value of the voltage steps or requesting new positions.

As a consequence the "zeroing" edge of the BUSY line is normally used to set the flag of the device calling attention from the computer.

5. Buffering of unibus lines and selecting the channel

The unibus on each strip (row) of 8 channels is buffered by a "two ways" input–output card, from the device general bus interconnection. The schematic of the card is shown in fig. 5a in which buffering and gating of data lines (a_0–a_4, +10BIT) is shown.

Input–output gating is controlled by the STR IN signal. This allows the flowing of signals from input (computer) to output (the channel) when it is set to the high level ("1"); when it is "low" the flowing is reversed and the reading into the computer of the actual position of the sliding contact and the value of the single step is allowed.

When the device is not under computer control (MAN signal low) the MAN signal disables the STR IN line towards the device, via open-collector gate 7406.

The outputs of the transmitting gates from the computer are on the unibus of the strip bearing 8 channel circuits, each one with unterminated input (see fig. 4 for input a_0–a_4+10 BIT): the transmitting gate has then its pull-up stage (standard type 7400). However, the input of the buffer (from the computer) is expected to be terminated so that the transmitting gate to the computer is then an open-collector (standard type 7403).

The circuit schematics for address selection is shown in fig. 5b. Three bits of the computer output word are employed to choose the strip (8 channel circuits), and three more bits to select the channel within the strip. We have redundancy with respect to the 44 channels included in a single unit but decoding is directly obtained through two separate 7442 BCD-to-decimal decoders. Using only 8 outputs, the input of the de-

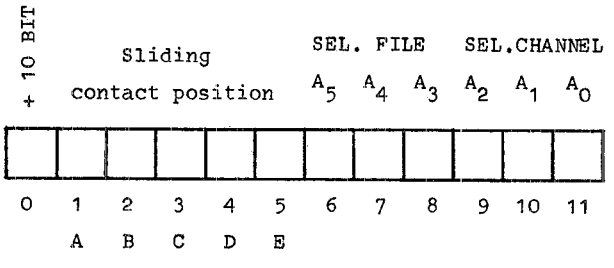

Fig. 6. Word bit organization for information exchange between the device and the computer.

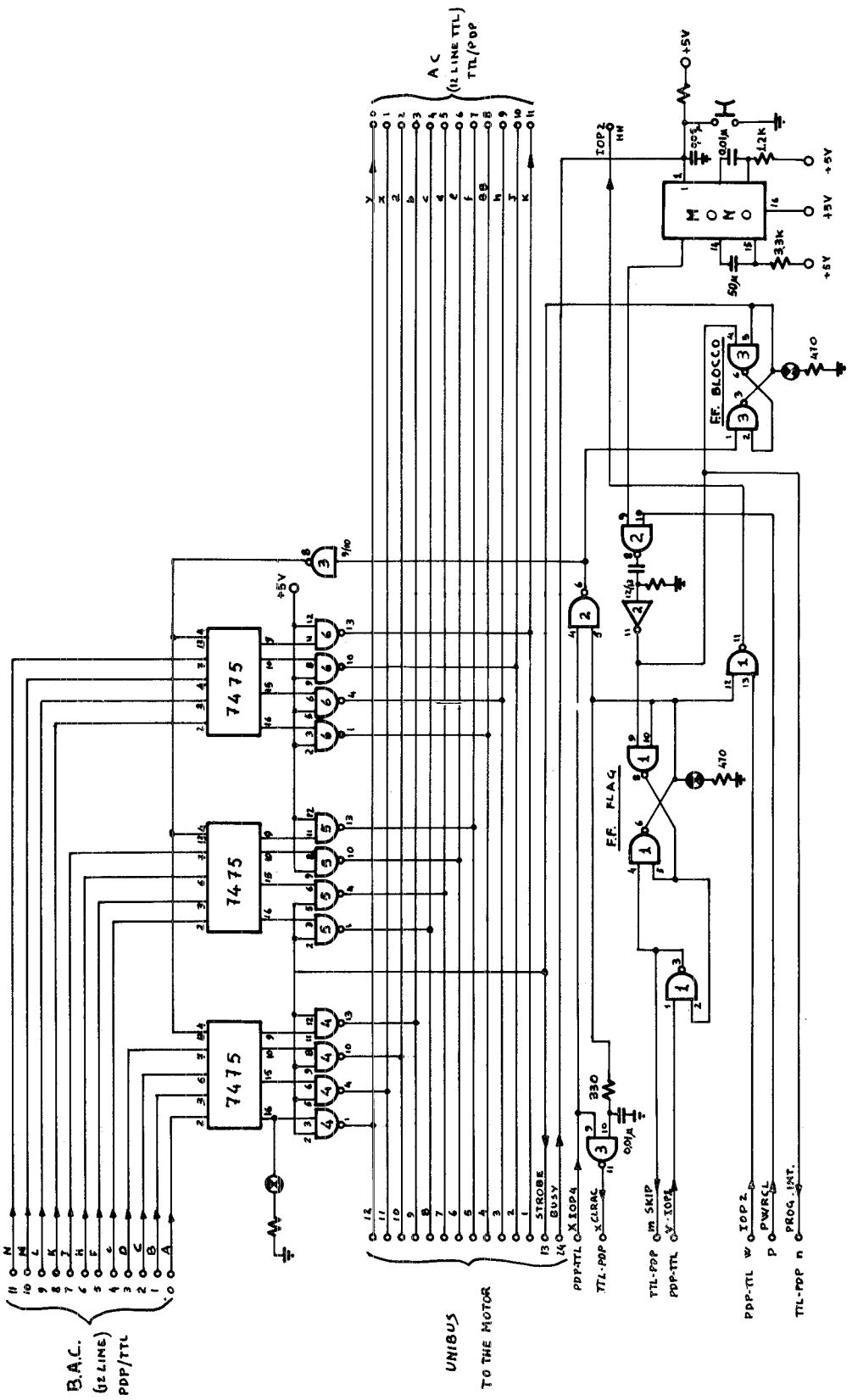

Fig. 7. Schematic of the interfacing between the device and a PDP8.

coder's M.S.B. is used as ENABLE input to select the channel within the strip.

The organization of word bits to exchange information between the device and the computer, is shown in fig. 6.

6. Reading the position and requiring a new one

Referring to table 1, when the SELECT signal is active (high) and STR IN is low, inverter 7(1,2), NAND gate 4(12:13, 11) together with the inverter 8(8, 9), realize the R signal to open the reading gate on the unibus, that is:

$$(\overline{\text{STR IN}})\cdot(\text{SELECT}) = \text{R}.$$

The output bits of the Gray-to-binary converter (input B to the 9324 comparator) are transferred as output data $a_0 a_1 a_2 a_3 a_4$ to the unibus data lines.

Transistor T_9, utilising $\overline{R}$ as a base signal ($\overline{R}=0$ for reading), transfers a high level on the +10 BIT data line if relais $R_{at\,2}$ is excited, i.e. the voltage step value is set to 20 V. However, if the value of the voltage step is 10 V (relais $R_{at\,2}$ released, contact open, D_9 inserted in series) a "0" level is transmitted to the +10 BIT unibus data line by transistor T_9.

When the STR IN and SEL signals are active together, the NAND gate 4(9:10, 8) and inverter 8(5, 6) produce the signal W as:

$$\text{W} = (\text{STR IN})\cdot(\text{SELECT}).$$

This signal opens the gates which send the signals on the data lines unibus to the input lines of the 9324 comparator compelling the motor to move towards other required positions.

When the device is under computer control, the MAN signal disables the ECD-to-binary converter whose outputs are open-collector, enabling the control from the writing gates. Notice that data must be present on the unibus for all the time required by the motor to reach the new position.

7. Interfacing with a PDP8

A schematic of the interfacing circuit is shown in fig. 7. Data words from the computer are buffered in a provisional register written by IOP4 pulse when F.F.FLAG is set. The flag setting is obtained from the zeroing edge of the BUSY line signal after an appropriate delay to bypass any mechanical backlash of relais and motor after the stop command.

The status of the flag is continuously checked by IOP1 which produces the flag resetting.

The same pulse from the monostable setting the flag resets the hold-up F.F. whose output gives the STR IN signal that is allowed high for the whole time the data are requested to be stable on the unibus. The setting of the data-hold F.F. is due to the same IOP4 pulse strobing data for the computer B.A.C. lines into the holding register.

The high level of the STR IN line strobes data from the provisional register to the unibus.

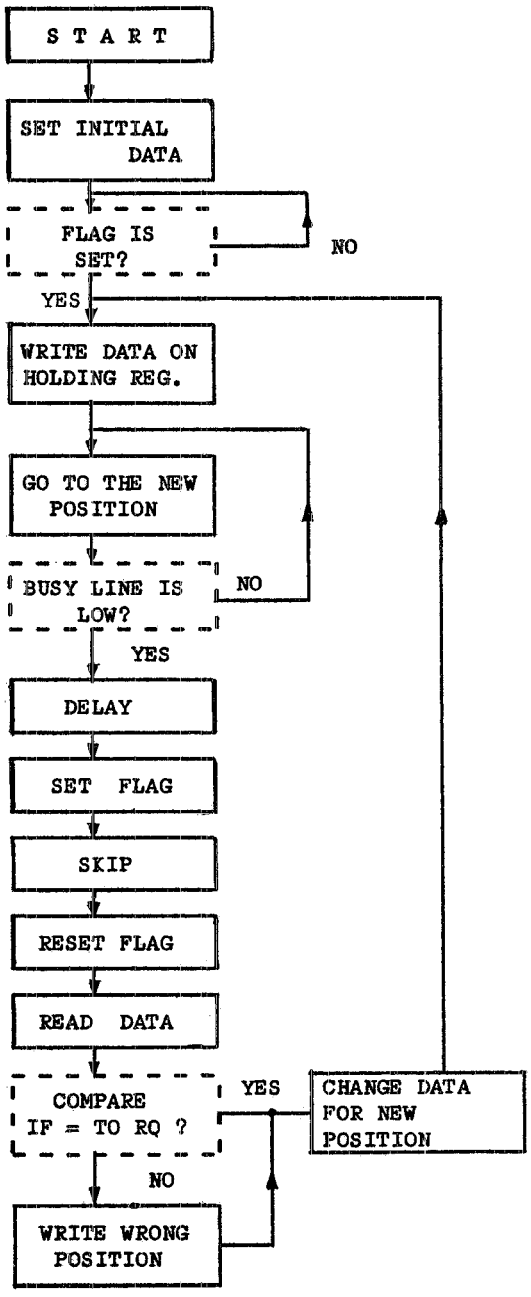

Fig. 8. Flow-graph of logic sequence of operations performed by interfacing circuitry.

Being programmed to request a position and then check, to read the same position before requesting a new one, the device has all the "address" bits in the computer word always stable on the unibus without gating.

A SKIP signal is generated (if the flag is set) at the moment the IOP1 pulse is checking its status, and is delivered by the computer before servicing the device.

A pulse to clear the accumulator is sent to the output of gate 3(9, 10) with a little delay after the IOP4 has been delivered writing the holding register.

The flow-graph of a logic sequence of operations that could be performed by the interfacing circuitry is shown in fig. 8. The circuit performing the operations of the flow-graph is shown in fig. 7.

8. Conclusions

To provide a motor-driven sliding contact to change the values of the hv to supply a P.M. particle detector seems to be economical and at the same time a simple way for computer control. In the near future devices could be realized to vary the hv supply without a mechanical sliding contact. One of these devices is under development in the L.N.F. (National Frascati Laboratories) and it seems to be sufficiently economic to be applied for a general solution of the problem. We need at the moment to ensure more reproducibility and reliability.

Nevertheless the two solutions need to be tested in actual experimental sets to get more experience about the use of such technological support in a high energy experimental apparatus.

The useful discussion with Prof. G. Barbiellini, about the design, the realization of the apparatus, and its use in high energy physics experiments, is greatly acknowledged.