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PROPOSAL FOR AUTOEQUALIZING SYSTEMS IN ANALOG TO DIGITAL CONVERSION

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I. - PULSE AMPLITUDE CODING. -

The purpose of this paper is to describe a method for A-D conversion with a good speed performance and intrinsic statistical equalization of the channel width[1]. The basic idea is to get a digital prevision of the final value of the amplitude to be measured before analyzing the pulse with conventional methods. Following this way, the measurement is performed only on the difference between the input and the analog conversion of the digital prevision (see fig. 1).

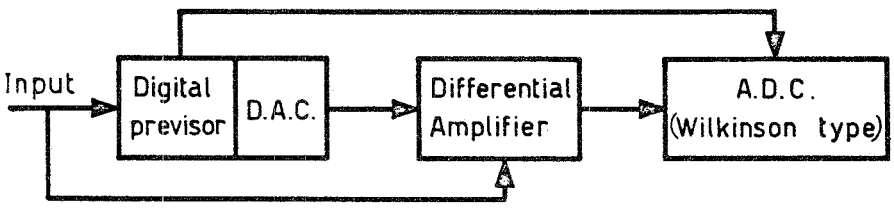

Fig. 1 - Block diagram of the converter system.

Two ways may be followed to carry out a prevision both taking an information from previously analyzed pulses or from the same incoming

pulse.

In the first case, the circuit that performs the prevision, the "previsor" would set the register of the ADC on the most probable amplitude on the basis of the previously analyzed amplitudes.

In the second case, one gets the information for the prevision from the leading edge of the incoming pulse or carrying out a parallel rough amplitude measurement. We point out that this rough analysis is a rough one in the sense that it has not to be precise.

I.1. - First method of analysis. -

First we take into consideration the simple case of a prevision performed on the basis of the previously analyzed pulse amplitude. For clarity sake, let us think of the incoming pulse amplitude to be little different to that registered for the previous event; in this case the "previsor" is the same ADC register that has not been reset after any cycle of analysis.

Now, let us briefly explain how the statistical equalization of the channel width is intrinsically performed (Autoequalization). In fact, the incoming amplitude is measured as a difference whose subtractor is the previously registered amplitude that generally is different from pulse to pulse as for the same input pulse amplitude.

The relative error of the channel width, W_k of the Digital to Analog Converter (DAC) in fig. 2 can be evaluated as follows:

$$W_k = C^{-1}\left[\sum_{i=0}^{k}(\varepsilon_{i+1}-\varepsilon_i)P_i + \sum_{i=k+1}^{C}(\varepsilon_{i+1}-\varepsilon_i)P_i\right] =$$

$$= C^{-1}\sum_{i=0}^{C}(\varepsilon_{i+1}-\varepsilon_i)P_i, \qquad (k = 1, 2 \ldots C),$$

where

P_i = the probability function that the event will be in the i^{th} channel;

C = the total number of channels;

ε_i = the relative error of the i^{th} level which defines the minimum boundary of the i^{th} channel;

$\varepsilon_{i+1} - \varepsilon_i$ = the relative error of the width of the i^{th} channel.

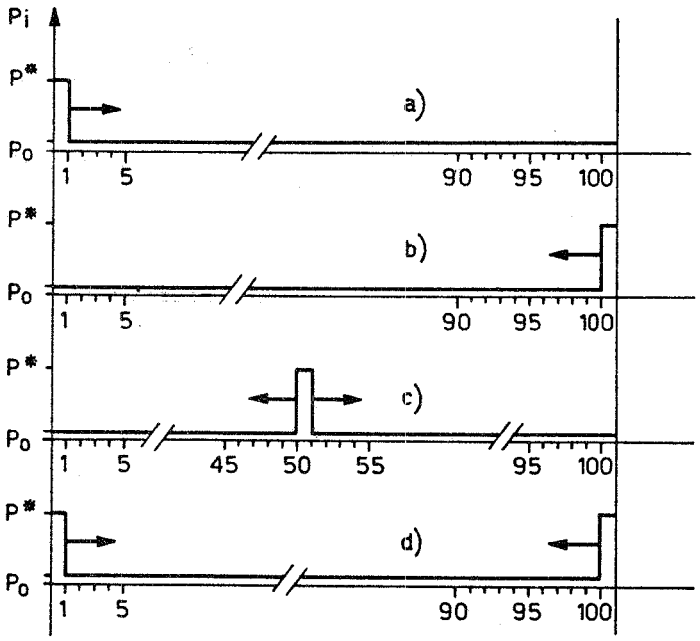

Fig. 2 - Probability functions P_i considered for conversion time valutation ($P^*/P_o = 10$).

Then, as W_k is independent from k, the differential linearity of the system is theoritically unaffected by DAC.

The channels of this system are equalized on different numbers of the Wilkinson ADC channels; in fact, the first and C^{th} channels interest all the Wilkinson ADC whereas, in the worst case, the $1/2\,C^{th}$ channel interest only 1/2 C channels of the Wilkinson ADC.

Let us now evaluate the time of analysis of the system. Given two consecutive independent pulses X and Y of amplitude i, k (i, k = 1, 2... C) whose probability is respectively P(i) and P(k). Let us consider the difference k-i = j, that has the following $P^*(j)$ probability function:

$$P^{*}(j) = \sum_{i,k=1}^{C} P(i) \cdot P(k),$$

or(o)

$$P^{*}(j) = \begin{cases} \sum_{s=1}^{C} P^{2}(s), & \text{for } j = 0, \\ \sum_{-s=1}^{C-j} P(s) \cdot P(s+j), & \text{for } j = 1, 2 \ldots C-1. \end{cases}$$

Being the Wilkinson ADC analysis time proportional to the number of the channel in which the event is registered, the expected value of the analysis time of our system is

$$t_1 = T \sum_{j=1}^{C-1} P^{*}(j) j.$$

The expectation value of the analysis time of a conventional Wilkinson ADC is

$$t_2 = T \sum_{j=1}^{C} P(j) j,$$

where T is the conversion time of one channel.

For a uniform probability P(i) function we obtain

$$t_1 = \frac{1}{3} T(C^2 - 1)/C \approx \frac{1}{3} TC,$$

$$t_2 = \frac{1}{2} T(C + 1) \approx \frac{1}{2} TC,$$

then the value of the ratio t_1/t_2 is $\approx 2/3$.

We see that the analysis time is reduced applying the method herein described.

(o) - To check the approximation of this formula for a finite number of pulses, we have applied a Monte Carlo method for a 100 channels and 2×10^6 total number of pulses. The approximation obtained is better than 10 %.

The t_1/t_2 ratio depends generally on the total channel number and on the shape of the probability P(i) function. The general case can be described referring to the results obtained considering the probability function configuration reported in fig. 2.

We have considered a 100 channel analyzer and a ratio between the peak and background probability equal to ten. The results shown in fig. 3 have been reported vs the number of the channels whose probability is ten times the background moving as the arrows of fig. 2.

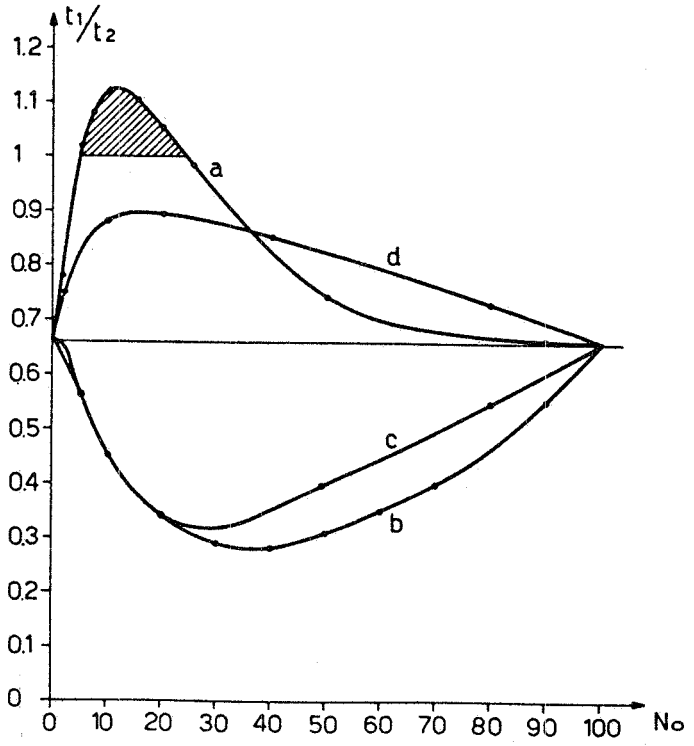

Fig. 3 - Time conversion ratio vs N_o = total number of the channels whose probability is P^*.

We note from fig. 3 that we have generally a reduction of analysis time except in case (a) for a little channel range (5 ÷ 25) of the peak width. Furthermore, the value of the ratio is not higher than 1.12 and we can report operatively this situation to case (b) by a simple complementation of the j-difference value.

The basic scheme of the system that is in progress, is shown in

fig. 4.

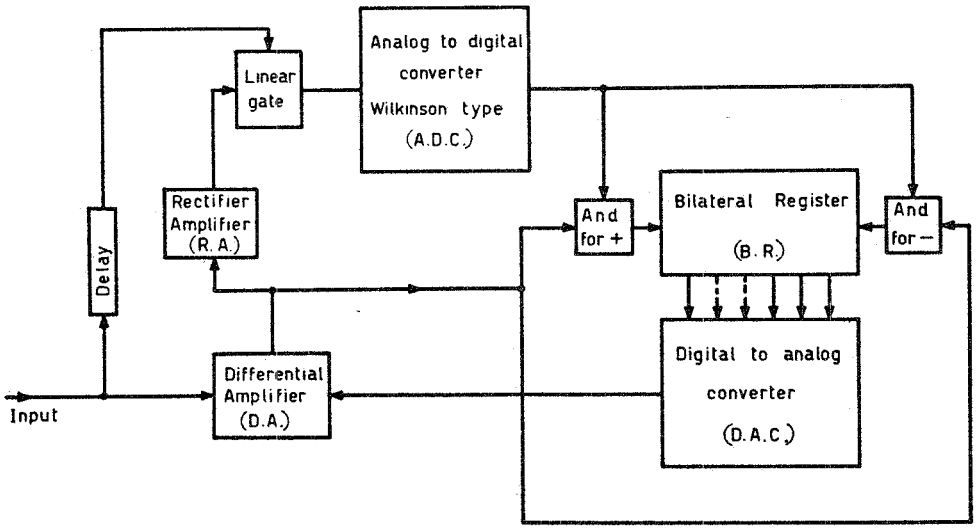

Fig. 4 - Block diagram of the first conversion system.

The BR (bilateral register) is never reset so that one input of the AD differential amplifier is always fed by the digital to analog conversion of the last registered pulse amplitude. The absolute value of the difference between the previously measured amplitude and that of the incoming pulse is analyzed by the ADC, while the difference sign controls the gates of the BR.

The differential linearity of the system depends on the Wilkinson ADC and on DAC of the "previsor" but the intrinsic capability of the autoequalization reduces the problem also in the actual realization when a finite number of pulses is coded.

I. 2. – Second method of analysis. -

Let us now consider the case of the prevision performed with a parallel analysis on the incoming pulse. The block diagram of a C(1024) channels converter is shown in fig. 5.

The ADC 1 is a parallel converter (multilevel converter) providing

$C_1(32)$ levels: at the output the rough digital conversion is transferred on the more significant bits (= $\log_2 C_1 = 5$) of the register. The less significant bits are set at random, for example not resetting those after any cycle of analysis.

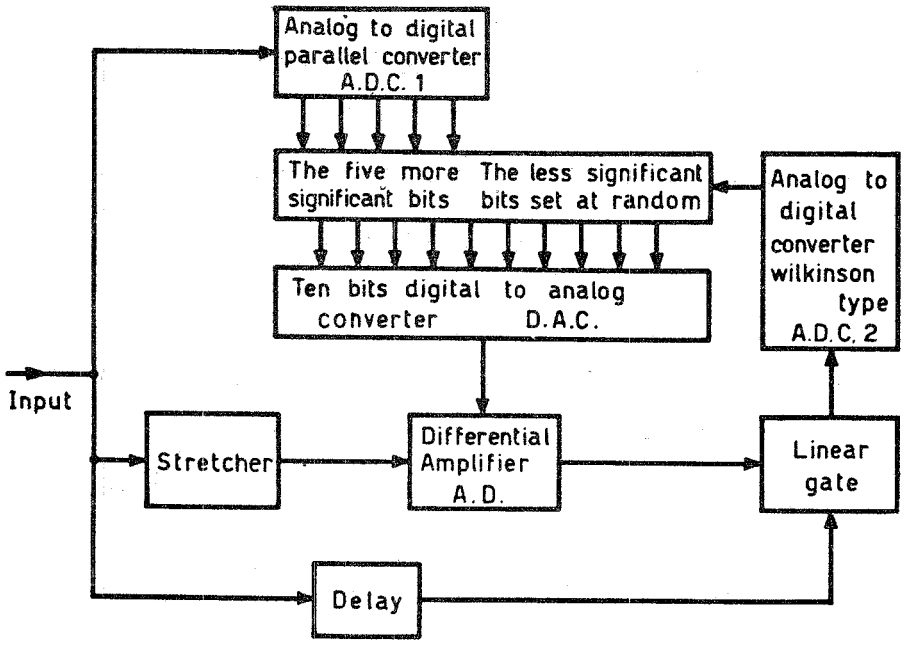

Fig. 5 - Block diagram of the second conversion system.

The ADC 2 Wilkinson converter analyses the difference value between the digital to analog conversion of the register and the input pulse amplitude.

The total number of ADC 2 channels must be theoretically $C_2 = C/C_1(32)$, but, as the precision and the stability of ADC 1 is poor, this number must be light increased and it is obviously expressed by

$$C_2' = C_2(1 + x),$$

where x is the differential linearity of ADC 1. Let us now remember that the register of the less significant bits is set at random; as a

consequence the output pulse from the differential amplifier may be positive or negative. To avoid the bidirectional register, as done in the block diagram in fig. 5, we must shift the ADC 1 levels over a quantity equal to one channel width. The ADC 2 must then possess a channel number :

$$C_2'' = C_2(2 + x),$$

The choice of C_1 is suggested by the following considerations :

a) The total number of channels $C = C_1 C_2$;

b) The total mean time of conversion given by

$$\tau_c = \tau_1 + \tau_2 + \tau_3 ,$$

where

τ_1 = the ADC 1 conversion time (independent on C_1 number);

τ_2 = DAC conversion time;

$\tau_3 = \frac{1}{2} T \cdot C_2$ is the expected conversion time of the Wilkinson converter fed by a white amplitude distribution;

c) Practical limits in the actual realization of the multilevel converter ADC 1;

d) The channel number to which the equalization must be extended.

The channel width autoequalization is effective on C_2 channels as regarding the differential linearity of the DAC, but for the Wilkinson ADC 2 the autoequalization is effective in the worst case on $\frac{1}{2}C_2$ channels. When the autoequalization is effective, τ_3 is further reduced by a factor 2/3.

Finally we give a numerical evaluation of τ_c for

$$C = 1024 ; \quad C_1 = 32 ; \quad x = 0.25 ; \quad C_2'' = 72 .$$

If we suppose to have

$$\tau_1 = 1\,\mu\text{sec} ; \quad \tau_2 = 2\,\mu\text{sec} ; \quad T = 0.05\,\mu\text{sec/channel},$$

we obtain

$$\tau_c = \tau_1 + \tau_2 + \frac{2}{3}\left(\frac{1}{2} TC_2''\right) = 4.2\ \mu\text{sec}.$$

We can see that the expected performance of the analysis time is a very good one.

I. 3. - Conclusions. -

The interest to increase the speed of analog to digital conversion must be centered on the extensions of the channel number for a high resolution in multiparametrical analysis problems, with a constraint of the dead time of the system. This point of view justifies also the importance we gave to an intrinsic autoequalizing system utilizing a Wilkinson converter.

In our laboratory a work is in progress to check the actual performances of the two proposed systems. Moreover, we have started with the synthesis for the optimum "previsor" to perform the minimum expected time of analysis of the first system we have described in this paper.

II. - TIME TO PULSE HEIGHT CONVERSION. -

The main problem in time to pulse height converters (TPHC), like in all systems which operate lineraly on a signal distribution, arises from the request of good integral and differential linearity performances. These are improved by a very careful circuitry, but a substantial progress with statistical equalization methods is possible[1, 2, 3]. We refer to our equalization method, previously used in analog to digital converters[4], in order to improve their differential linearity performances. We will deal with two of possible realizations of this method; the first allows the improvement of the differential linearity; the second

too allows a reduction of the time of analysis associated with the multichannel pulse height analyzer.

Method description: The basic idea is not to convert directly the time interval T (defined by the START and STOP pulses), but to obtain its conversion by the algebraic sum of the two levels relative to the conversion of two uncorrelated time intervals T_1 and T_2. These are generally different, also for time intervals that will be classified in the same channel; in this way we obtain a statistical equalization of the channel width.

Let us see now, how the two time intervals may be generated.

T_1 is bounded by the START pulse and by an external random stop pulse (RSP). The second interval, T_2, must be realized in two ways according to the arrival order of the RSP and STOP pulse: if the RSP is coming before the STOP pulse T_2 is bounded by the RSP and STOP; in this case T is the sum $T_1 + T_2$ (fig. 6a). On the contrary the boundaries are inverted and now T is equal to $T_1 - T_2$ (fig. 6b).

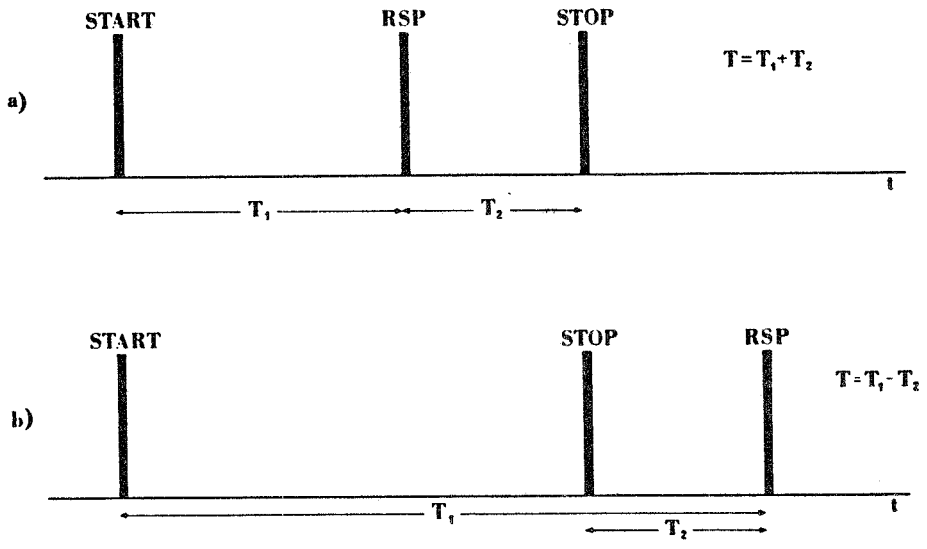

Fig. 6 - The two situations for the T_1 and T_2 pulses.

Some schemes of method realizations: Many circuits may be suggested to perform the measurement with statistical equalization as described before.

In fig. 7 we show a block diagram of the first suggested system. The RSP pulse is obtained by a time interval random generator. The T_1 interval is converted by the C_1 converter. Let us suppose that, at the beginning, the logic gates G_1 and G_2 are opened while G_3 and G_4 are

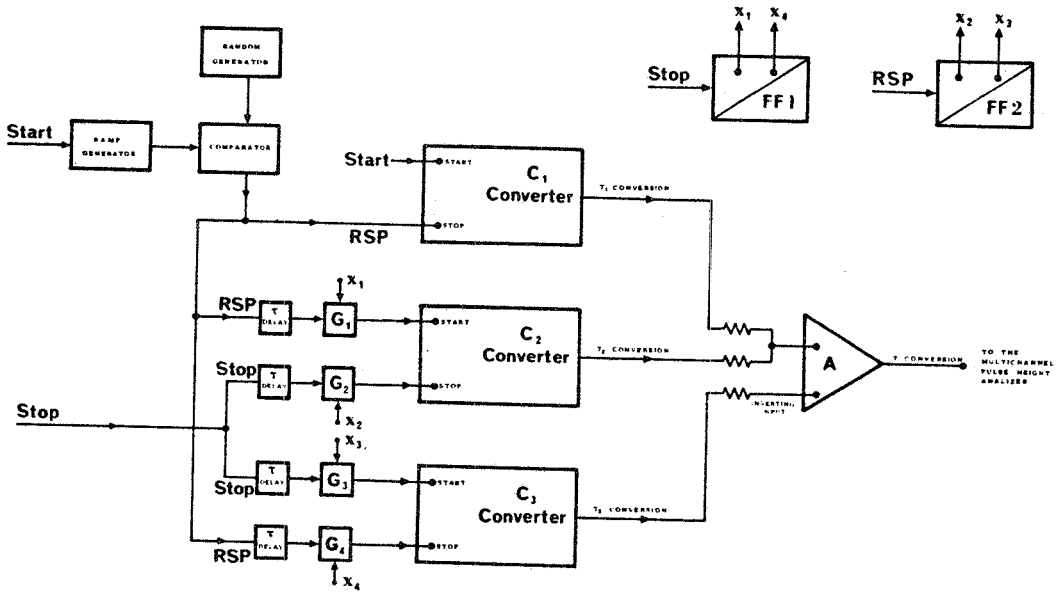

Fig. 7 - Block diagram of the first system.

closed by means of the FF1 and FF2 flip-flop triggered by the STOP and RSP pulses.

When RSP is coming before the STOP the time to height conversion of T_2 is carried out by the C_2 converter because G_3 is now closed and G_2 opened by the FF2 commutation; then the next pulse (the STOP) will feed C_2. In the second case (the STOP coming before the RSP) the T_2 conversion is carried out by the C_3 converter.

The C_1, C_2 and C_3 outputs are algebraically added by the adder A whose output is then the T conversion.

The minimum time interval that can be converted is equal to the

switching time T_s of FF1 and FF2; in order to reduce that interval four equal delays τ are introduced. If the STOP and RSP widths are greater than $T_s - \tau$ and $\tau < T_s$, the time resolution is now $T_s - \tau$.

The second scheme we propose is shown in fig. 8. The RSP pulse is obtained by the digital to analog conversion (DAC) of the bidirectional

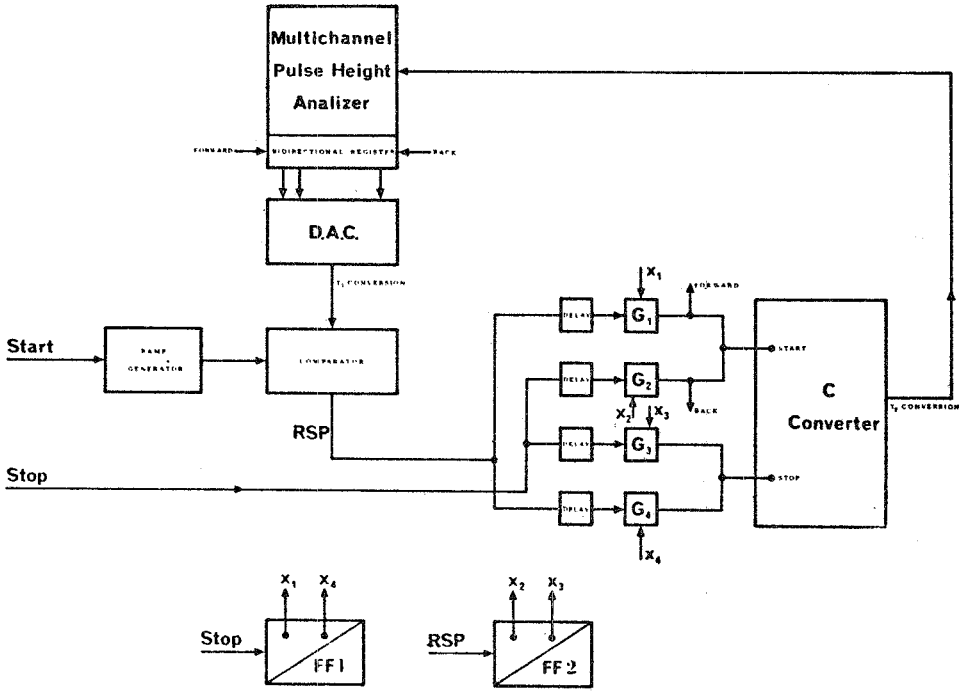

Fig. 8 - Block diagram of the second system.

register of the multichannel analyzer which holds the measure of the previously analyzed time interval T. This is to be considered as the T_1 measure.

At the beginning G_1 and G_2 are opened and G_3 and G_4 closed. By means of the logic already explained in the previous scheme we obtain, from C, the T_2 conversion independently from the arrival order.

The C output feeds the multichannel analyser and its analog to digital conversion is added or subtracted to the bidirectional register content according to the pulse to the C converter "start" input comes from the gate G_1 or G_2.

In this case we generally perform, besides the statistical equalization of the T conversion, a reduction of the analysis time if one uses a Wilkinson type analog to digital converter. For instance, if the time interval spectrum is uniform, we have a reduction of the analysis time equal[2] to 1/3.

We can note that in both schemes the statistical equalization leads to a more complex circuitry and it requires a more flexible instrumentation as, for example, a bidirectional register in the multichannel analyser. This fact is not a heavy problem owing to the present tendency towards more flexible systems.

Moreover, optimized systems can be studied following the method proposed. For example, in the scheme of fig. 7 the C_3 converter can be substituted by a logic able to choose the inverting or non-inverting input of the final adder. Furthermore, the scheme of fig. 8 can be rearranged substituting the DAC with an analog memory.

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