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R. Visentin : A SHORT DEAD TIME GATED-INTEGRATOR

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A SHORT DEAD TIME GATED-INTEGRATOR

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The circuit here described, is a linear gate. It was derived from the circuit published in Nucl. Instr. and Meth. **64** (1968) 21 *.

The actual circuit (fig. 1) is completely dc coupled and works with positive pulses of any shape and amplitude from 0.1 mA to about 100 mA. The differential amplifier T_xT_y is sensitive to the potential differences on R_x or C_x, which are zero when D_x is turned off (gate shut). T_xT_y gives at the output two equal amplitude pulses of opposite polarity. These pulses are a linear replica of the input pulse (gate on) on the collector of T_1, when R_x is the load. When C_x is the load on the collector of T_1, the output voltage pulses are the integral of the input current pulses on T_1. A negative pulse on T_2 opens the gate for a length Δt; the current $I_1+I_2+I_p$ turns off D_1 and the current from R_y flows through D_2 in D_x, which is turned on. In this condition the current pulse at the input of T_1

* In this paper the label near each curve of fig. 5b has to be changed from picocoulomb to nanocoulomb

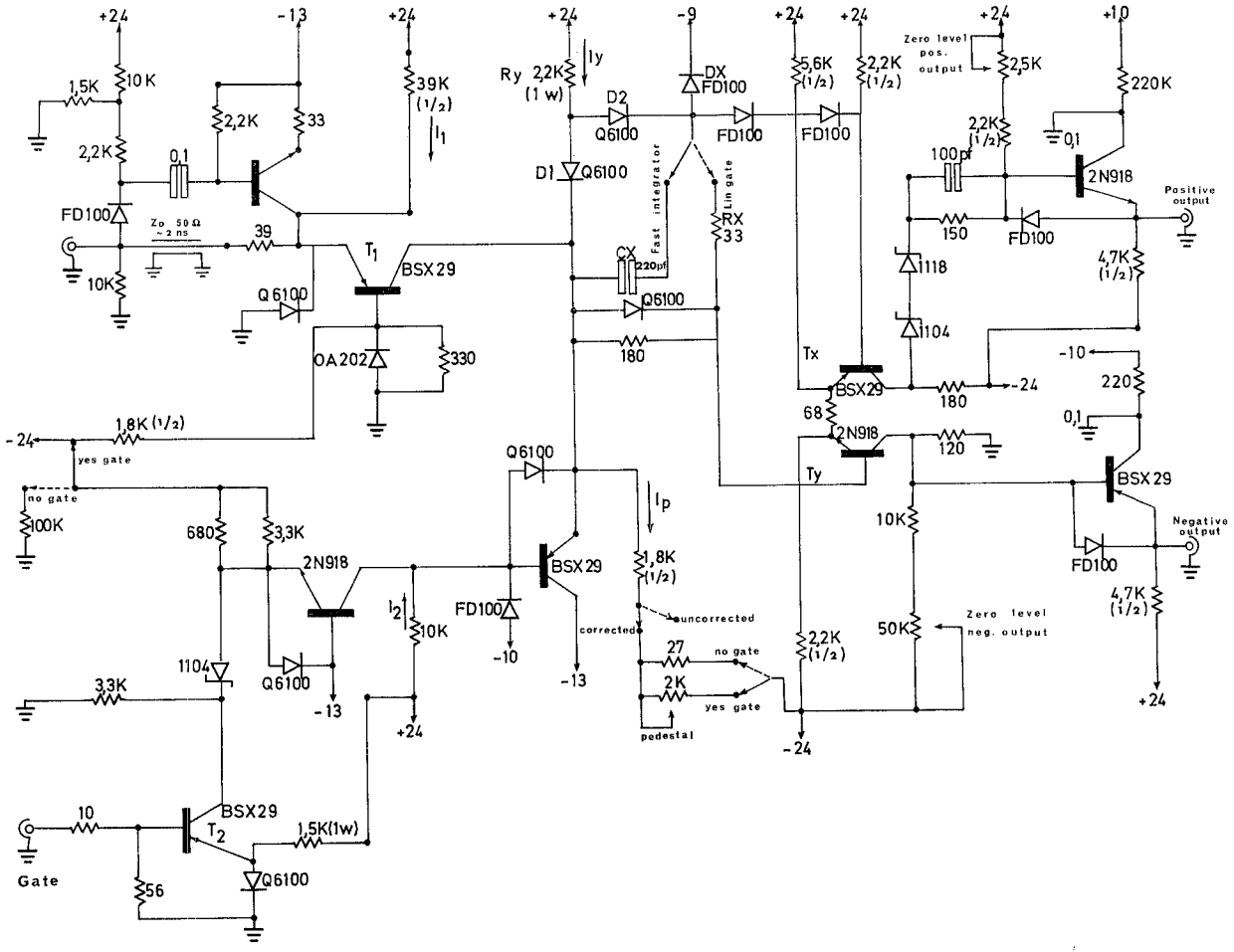

Fig. 1. Scheme of the short dead time gated-integrator.

charges C_x, or gives a p. d. through R_x. When the gate is shut, D_1 conducts, D_x is turned off, and C_x is discharged in $\approx$ 20 ns. Thus the length of the output pulse is practically always equal to Δt. This circuit, used as fast gated integrator, has been tested at frequencies up to 12 Mc/sec in the range of input currents cited above. When used as a linear gate, it operates at higher frequencies up to 20–25 Mc/sec.

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