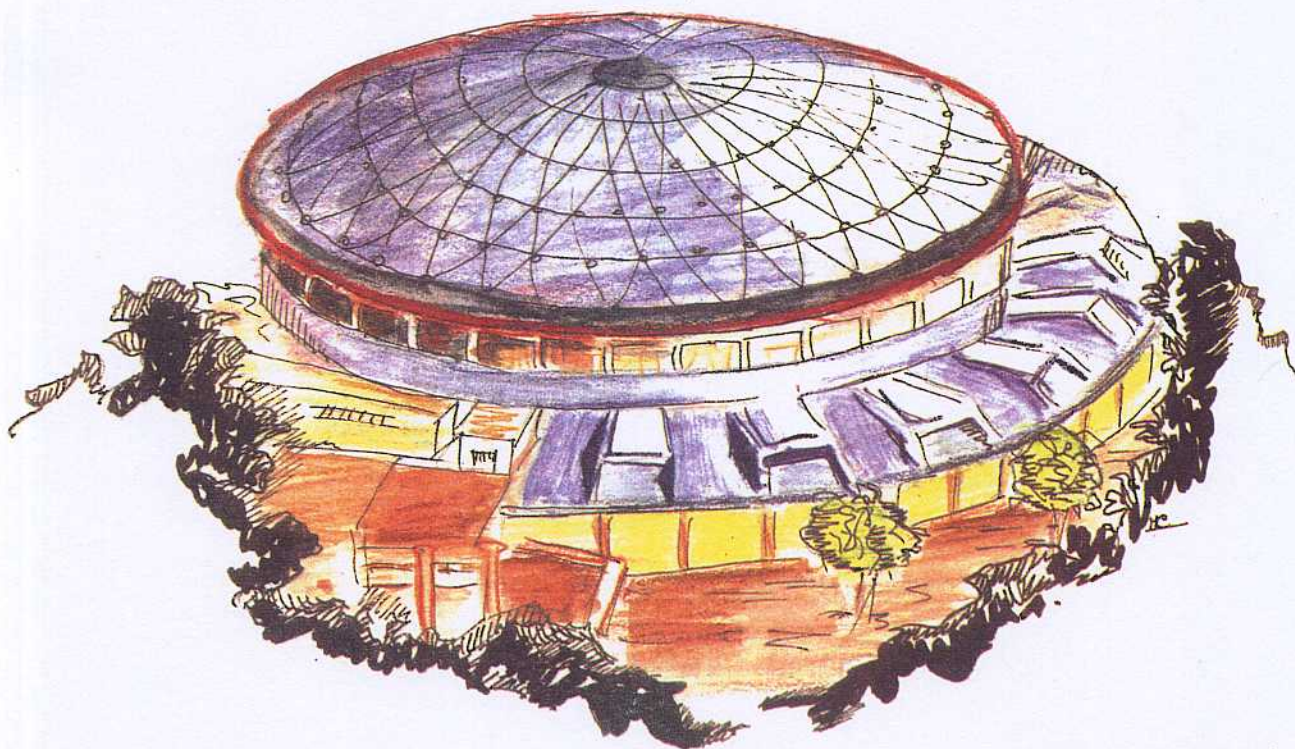


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**MACTRA: AN INTERFACE BETWEEN A MACINTOSH II AND A
TRANSPUTER LINK**



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**MACTRA: AN INTERFACE BETWEEN A MACINTOSH II
AND A TRANSPUTER LINK**

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ABSTRACT

MACTRA is a NuBus board that allows to interface a Macintosh with a Transputer system through a standard transputer link. The board has been designed to transfer graphic data at a high rate to the Macintosh. A transfer speed of 600 kBytes/s has been achieved from the link to the Mac. No effort has been done to optimize the speed in the opposite direction, because the system has been designed to perform as a graphical output device.

1. - INTRODUCTION

The Macintosh computer is ideally suited to be a color graphic output device. If an application is written according to the Apple guidelines one can immediately take advantage of several operating system facilities, like multiple screens, variable color depths, palette handling, etc.

We have built a Nubus interface to a transputer link, with the idea of downloading from a separate host calculated graphic data.

2 - SYSTEM DESCRIPTION

The system has been kept as simple as possible to maximize speed. Fig. 1 shows a block diagram of the interface.

The operation is as follows: the transputer link is connected to an INMOS IMS C011 Link Adapter.

When the Link Adapter receives data from the link it signals their presence to the control logic. The interface automatically transfers the data to a set of two 2048 byte FIFO's. Data are

written in series, alternating bytes between them, and read in parallel from the Macintosh through the NuBus interface. When the FIFOs contains more than 1024 bytes they generate a Half Full signal. This signal is used to notify the Macintosh that it can read 1024 16 bit words without having to check individually for their existence.

Data sent from the Macintosh to the transputer link are directly routed to the Link Adapter, which generates a DTACK (Data Transfer Acknowledge) toward the Nubus Interface. This arrangement is much slower than the one in the opposite direction, but in our case only a very small amount of commands was to be sent to the Link. It would be easy to duplicate the FIFO arrangement in the other direction, if needed. Care has to be taken while using the FIFO at the same time for reading and writing from two asynchronous hosts, since the two operations cannot be performed at the same time. We used a first come, first serve arrangement.

The board has been tested with the link adapter IMS C011 operating at 10Mbit/s. It is possible to operate at a speed of 20 Mbit/s for very short links.

The tests have achieved a speed of 600 kBytes/s. This corresponds to a refresh speed of 2 Hz on a standard 13" Macintosh monitor (640*480 pixel with 256 colors). An improvement of a factor of two could be gained using a 32 bit Nubus interface. A large additional factor can be achieved by the use of image compression techniques.

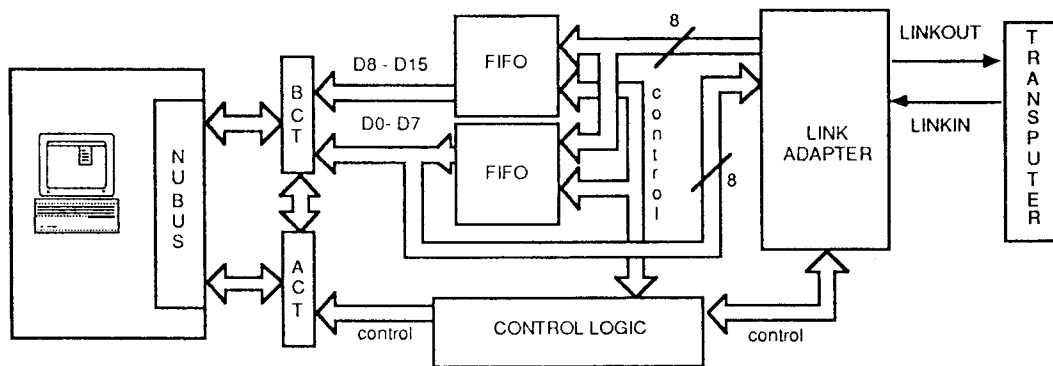


FIG. 1 - MACTRA block diagram.

2 - HARDWARE

The interface prototype was built using a semicustom board, MCP (Macintosh Coprocessor Platform) from Apple Computer. This board contains a Nubus interface built around two Texas Instruments integrated circuits, SN74ACT2441 and SN74BCT2425. The board also contains a 68000 CPU which was disabled for our prototype.

The FIFO was a cascadeable 2048x9 (CYPRESS CYC429), with a read/write speed of 25 MHz.

The control logic was realized with a sequential logic circuit. We used standard TTL flip-flops and a PAL MA1628.

3 - SOFTWARE

A set of primitives has been implemented in 68030 Assembler language in an MPW environment. The primitives, structured as subroutines and recallable by any other language, include:

MACTRA INIT, to initialize the board.

MACTRA READ ONE, to read one byte from the FIFO.

MACTRA READ BUFFER, to read 1024 bytes from the FIFO.

MACTRA WRITE ONE, to write one byte to the Link Adapter.

A test program was used to transfer a full screen image to the MAC using the MACTRA READ BUFFER routine and testing the FIFO Half Full bit.