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F. Celani: HARDWARE PROCESSOR, SPECIAL PURPOSE,
FOR CAMAC SYSTEM. -

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SUMMARY...

A Camac system in order to read, elaborate, m.emorize, visua
lize the data on film by:using displays, takes the place of Crate Control
ler. Branch Driver and Computer.   -

1. -INTRODUCTION.-

We describe the technical characteristics of an experimental
apparatus" which has been realized at the Laboratori Nazionali di Fra
seati and used by the MEA group in the counting room of Adone. The-
major characteristics of this apparatus allows to realize a system of
acquisition, elaboration, memory, reinput and permanent memory on
film of data.. In our particulary experiment the apparatus takes com-
pletely the place of both the Crate Controller (and Branch Driver) and
the Computer. Essentially the apparatus consists of a "IControl block"
which gives: the suitable commands to acquire and to reinput data, an
Elaboration block in order to elaborate the acquired data, a "Memory
block" (with registers) to memorize temporarily the elaborated data
before to reinput them on Writing lines (W) to load the Output Registers.

2. - LOGICAL SEQUENCE OF THE OPERATIONS DONE.-

TheCamac configuration with which the system exchanges informations consists of:

a) 4 Pattern Units,
b) 4 ADC,
c) 8 Output Registers (OR),

The logical sequence of operations performed by the system is:

a) Send the commands of Reading in order to acquire the data from Patterns and ADC ;
b) Elaboration and memorization of acquired data;
c) Send` commands of Writing in order to input in the OR tb.e data pre viously elaborated and loaded;
d) Synchronous lighting of all the Displays (done with Nixies) controlled by OR when the transf.er of data has been finished on these OR;
e) Permanent memory on film of the configurations of the displays.

3. - BLOCK DIAGRAM.-

We describe here the block diagram for the controller. The signal of "EVENTO" (the only signal needed to initialize the appara‥tus), which is delayed of 130 μs in order to prevent the upsets caus ed by "discharge" of the Spark Chambers in the operative room of‥ Adone. After this time a One-Shot clears and presets the apparatus.

The end of the previous signal controls a Flip-Flop whose output "set free" a "Gated Clock", which together with the circuit "SHA PER". gets the timing in accordarlce with the CAMAC requests.

A Synchronous Counter to 16 counts the pulses of the gated clock and with his 4 outputs A, B, C, D controlls the DEMULTIPLE‥XER *0/16* outputs). These 16 outputs of the demultiplexer, grouped 4 by 4. gating proper Flip-Flop and Gates, cause the Function of Read or Write. the Strobes SI and S2, the Sub-Address A1 and A2 (in order to select the 2nd section of each OR) and contributes to the Number of Station in order to select the module with which one wants to dialogue. The selection of the module is performed with the assistance both of a "to 4" counter (triggered by the output ripple clock of synchronous counter to 16) and of a decoder block of the number counted by the asynchronous to 4 counter. As soon as writing is accomplished on the last of OR, a GATE circuit acknowledges this situa tion and stops the system.

In respect of the Elaboration, the data coming from Patterns are inverted before the reinput in the OR, while the data coming fronl ADC, first are inverted and next are converted from Binary to BCD code.

The Record of the data has been done using many DFF organi-'zed in a 16 bits register (the greatest capacity of the Patterns). The CP for the registers coincides with the S1. strobe that occurs during the reading, specified in the diagram by 81 R.

4. - FURTHER DEVELOPMENTS. -

The system has been designed to be very flexible and extendible. In the block diagram (Fig. 1) the elemnts necessary to adjust the system to the request of the MEA Group, respectively to input and out put, have "been showed with the representation _ -   and · · · · ·· In order to extend the number of module with which exchange informa tion one can :

a) To alter the reset of asynchronous to 4 counter. For every unitari-an increase of the previous reset it is possible to dialogue with 2 m'odules in a reading mode and 2 mode in a writing, mode.

b) To use the next outputs of the circuit "Selection Number Station: N".

In order to change the Elaboration it is necessary to replace the elaboration module (the code converter Binary ⟶ BCD). For this purpose we have done the priod of the Strobe (decided from "SHAPER" circuit) with 600 ns followed by 600 ns of "dead time".

In order to change the Functions it is necessary to add other proper FF and Gates to the first outputs of every group of 4 outputs of the demultiplexer 1/16 outputs.

CAMAC DATAWAY

F16 1"8 F4 F2 F1   A8 A4 A2 A1

S1 52 C Z 1

NORMAL OR CONTROL STATION

CAMAC DATAWAY

READ LINES 16 BITS

NORMAL STATION

13 LINES

16 LINES

CAMAC DATAWAY

N

CONTROL

STATION

12

LINES

Functiones: FCT2/FCT16

PATTERN-A.D.C./OUT.REG.

SAD: A8, A4, A2, A1

S1, S2, C, Z, N

S1R
S1

LATCHES 16 BITS
Decoder BIN → BCD
8 → 10 BITS
From Read Lines
of A.D.C.

16
Lines

DATAWAY
WRITE
LINES
16 BITS
NORMAL.
STATION

16 LINES

1

16

SHAPER

Enable

DEMULTIPLEXER
1 of 16 OUTPUTS

Clear

Input

A B C D

A B C D

DELAY
130 /us

EV:

One-Shot
for
Clear and
Set

Set

F.F. for
Init/End
Cycle

Gated
ClOCk.

Syn.
Counter
to 16

Asyn.
counter
to 4

Selection
Number
Station:N

GATE

Clear of   Initialize of Cycle.

Reset

Load
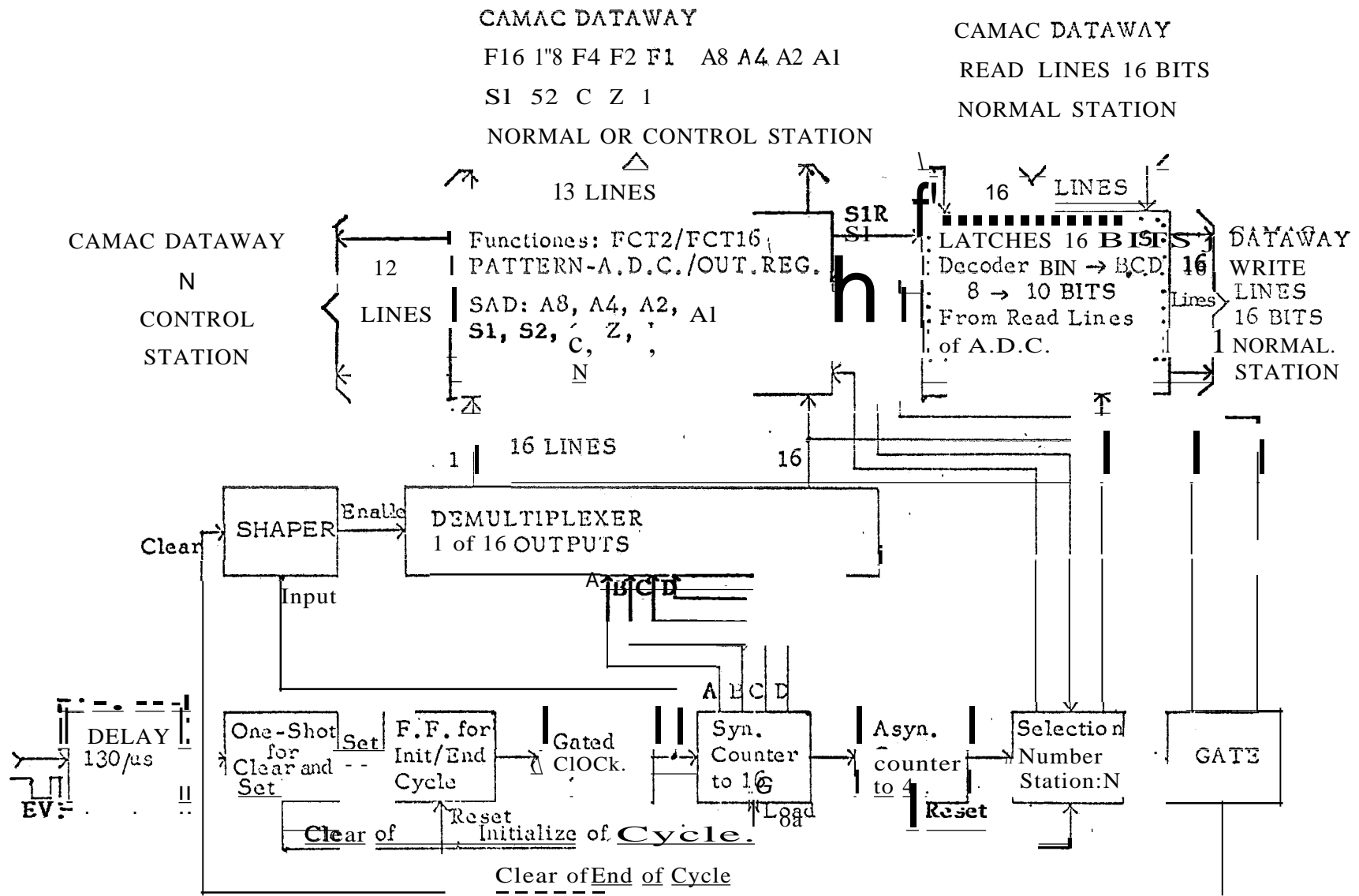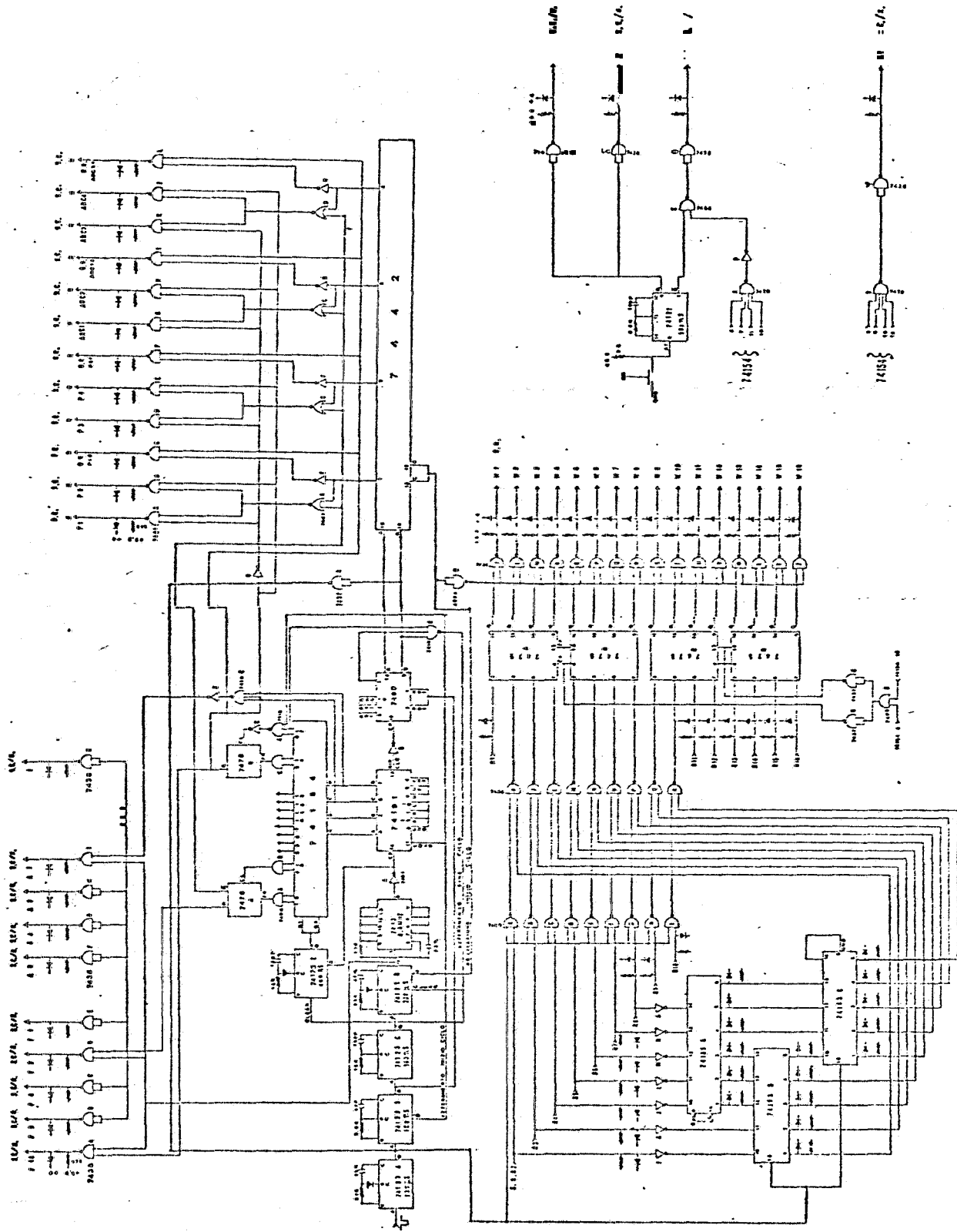
Reset

Clear of End of Cycle

FIG. 1 - Block diagram.

FIG. 2 - The complete schematic of the special controller.