

Laboratori Nazionali di Frascati

LNF-69/20

C. Prezzi and F. Soso : AN INTEGRATED FAST CORRELATION UNIT
FOR $n = 4$ BINARY VARIABLES

Estratto da : Nuclear Instr. and Meth. 68, 45 (1969)

AN INTEGRATED FAST CORRELATION UNIT FOR $n = 4$ BINARY VARIABLES

C. PREZZI and F. SOSO

Laboratori Nazionali di Frascati del CNEN, Frascati, Italy

Received 8 October 1968

Correlation units are intended as flexible building blocks of decision electronics in multiscaler experiments. The design and performance of a 4-variable module are reported.

1. Introduction

The need for new types of flexible and computer programmable logical electronic modules, for fully automated experiments, happily meets with the excellent characteristics of integrated circuits.

Conventional coincidences, fan-in, fan-out modules etc., can be built by integrated circuits, adding, if necessary, non-integrated circuitry to improve the overall performance*.

Also the whole experimental logical diagram can be

* For instance the Miniature Logic System of Elliot Process Automation Ltd.

built with integrated circuits, on large printed boards, with such mounting and wiring as to allow for the necessary changes.

An intermediate approach is to build some modules, whose logical function is complex enough to take advantage of integrated circuits and to obtain all logical diagrams by assembling few equal modules; yet the modules should be simple enough to be of a general type, independently of the particular application.

One such module has been studied and called Correlation Unit¹). It can give any logical function of n binary variables, in a time not longer than that requi-

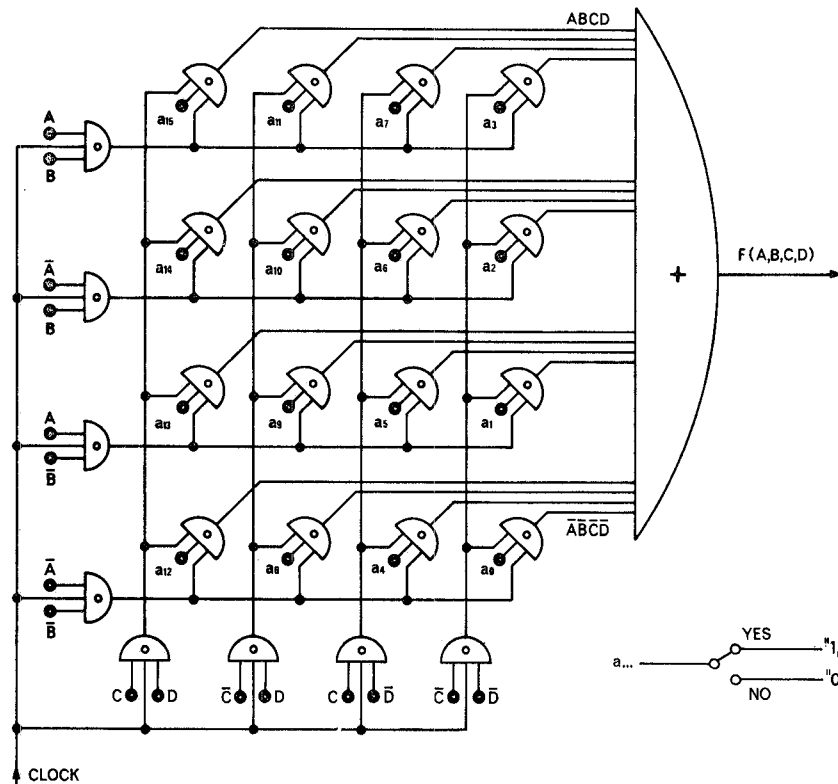


Fig. 1. Block diagram to obtain Boolean functions of 4 variables A, B, C, D . The remotely controlled a_i coefficients determine the function $F(A, B, C, D)$. The $a_i N_i$ terms are obtained from AND-gates, and then added in the OR-gate. The clock signal is a pulse synchronous with beam bursts (e.g. in storage rings), or can be obtained from a coincidence between low threshold discriminators.

red for usual coincidence-anticoincidence operation.

The output function can be easily changed by switches or external voltage levels from one function to another of the same variables. No change in signal width or delay is required.

2. Logical organization of a correlation unit

Let x_1, \dots, x_n be Boolean variables, e.g. discriminated signals from n counters. Any one of the 2^k , with $k=2^n$, Boolean functions $F(x_1, \dots, x_n)$ can be written

$$F(x_1, \dots, x_n) = \sum_{i=1}^k a_i N_i(x_1, \dots, x_n), \tag{1}$$

where the a_i 's are binary numbers and $N_i(x_1, \dots, x_n)$ are the normal products or minterms of x_1, \dots, x_n .

We define a program

$$\phi = (a_1, \dots, a_k), \tag{2}$$

as the set of k bits that completely specify $F(x_1, \dots, x_n)$. A correlation unit for the variables x_1, \dots, x_n must give a particular $F(x_1, \dots, x_n)$ by easily choosing one of the 2^k programs ϕ .

The block diagram of the correlation unit is somewhat simplified if $F(x_1, \dots, x_n)$ is written as

$$F(x_1, \dots, x_n) = \sum_{r,s} a_{rs} N_r(x_1, \dots, x_m) N_s(x_{m+1}, \dots, x_n), \tag{3}$$

where the a_{rs} are binary numbers and N_r and N_s are the minterms of the variables (x_1, \dots, x_m) and (x_{m+1}, \dots, x_n) respectively.

The diagram for $n = 4$ variables and $m = 2$ is shown in fig. 1.

3. Choice of the integrated circuits

The features of the AND, OR-gates to be used should be:

- Low switching and delay times. Therefore non saturated or current-mode logic should be preferred.
- High noise immunity, to neutralize crosstalk between signal paths.
- Logic levels like the usual levels of fast logic signals.

These requirements are well met by the Emitter Coupled Logic integrated circuit (Motorola MECL II, ARCA ECCSL, etc.).

The basic gate circuit (fig. 2) is similar to many tube or transistor coincidences with a current source shared by active elements.

The logical swing (0.7 V) is the one of NIM standard, with some level shift (-0.8 V) required.

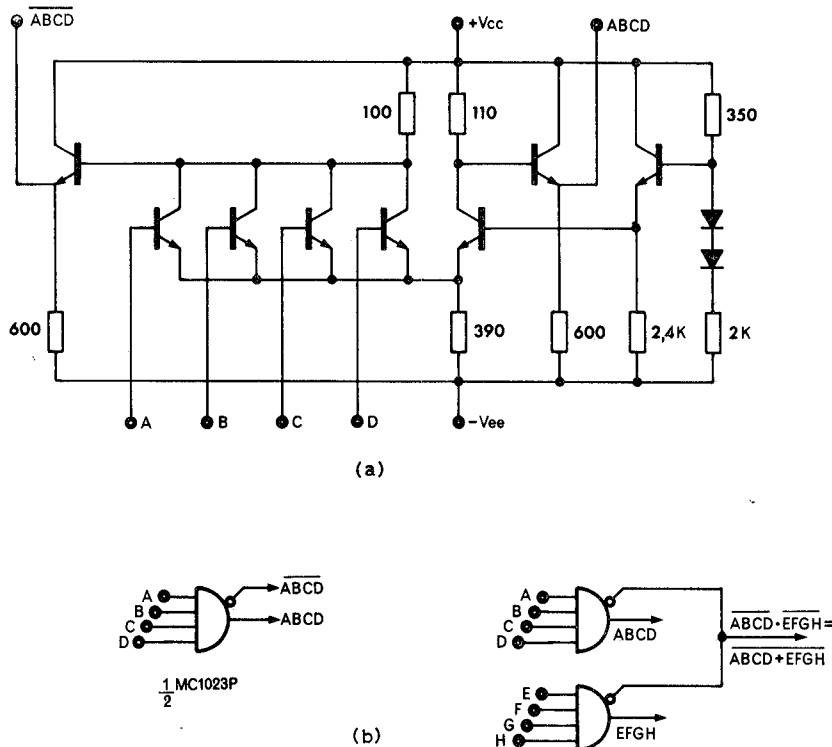


Fig. 2. a. The basic current-mode gate provides simultaneous AND-NAND output functions ("1" logic level negative). The threshold point is fixed by an internal bias reference. b. Logic symbol of the AND-NAND gate, and tied connection of two gates.

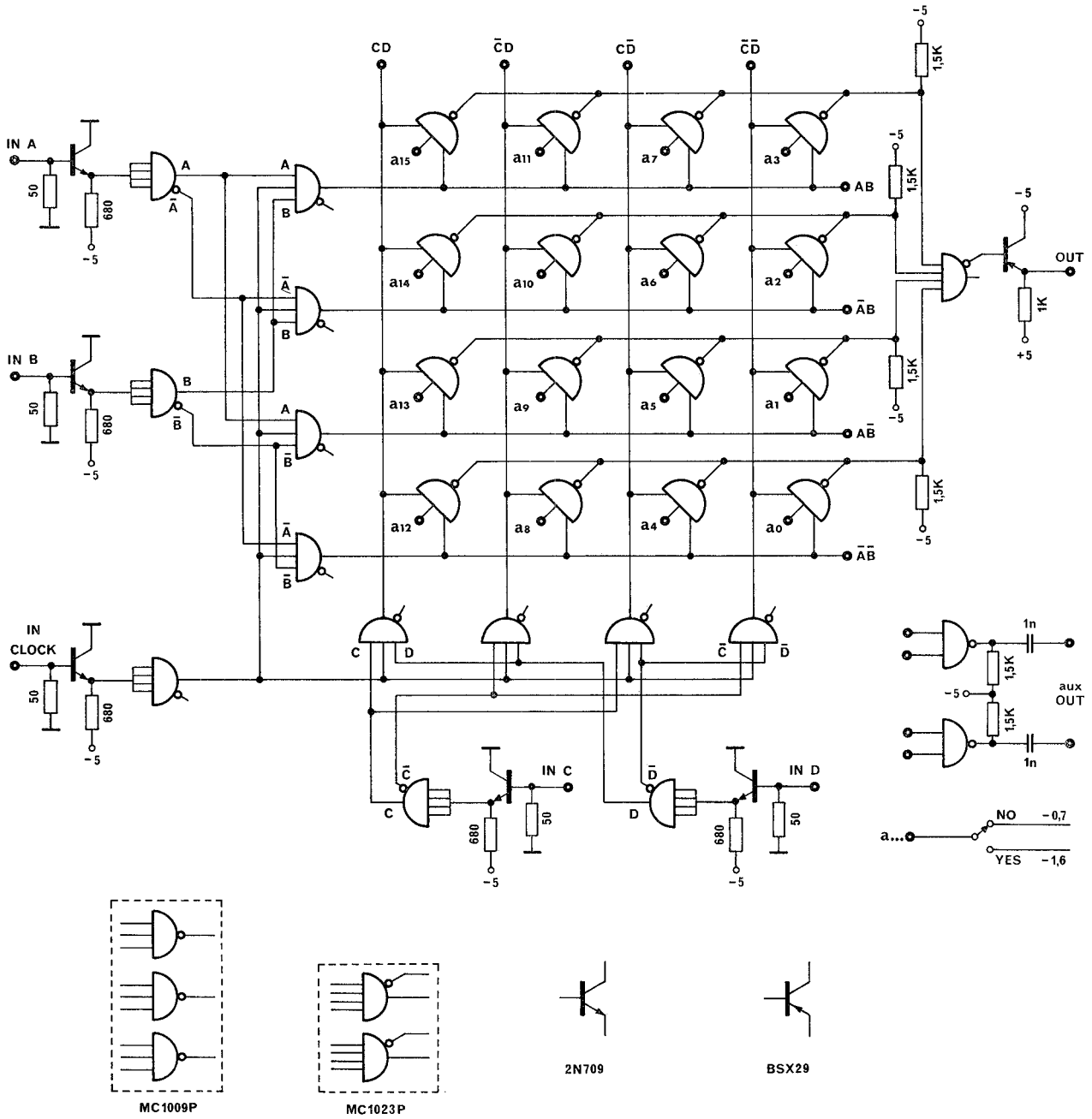


Fig. 3. Practical diagram of the correlation unit.

4. Practical correlation unit

Once the integrated circuits have been chosen, the diagram of a 4-variable unit (fig. 3) is straightforward.

Transistor emitter followers provide the input and output level shift, so that the whole circuit is dc coupled. Tied connections are used whenever possible. The a_i 's are switch-selected voltage levels.

Apart from some care in the printed card layout, no component selection or initial adjustment are necessary.

The behaviour of the correlation unit is shown in fig. 4. A clock signal at $f_0 = 50$ Mc and A, B, C, D waveforms at $\frac{1}{2}f_0, \frac{1}{4}f_0, \frac{1}{8}f_0, \frac{1}{16}f_0$ respectively are sent to the unit.

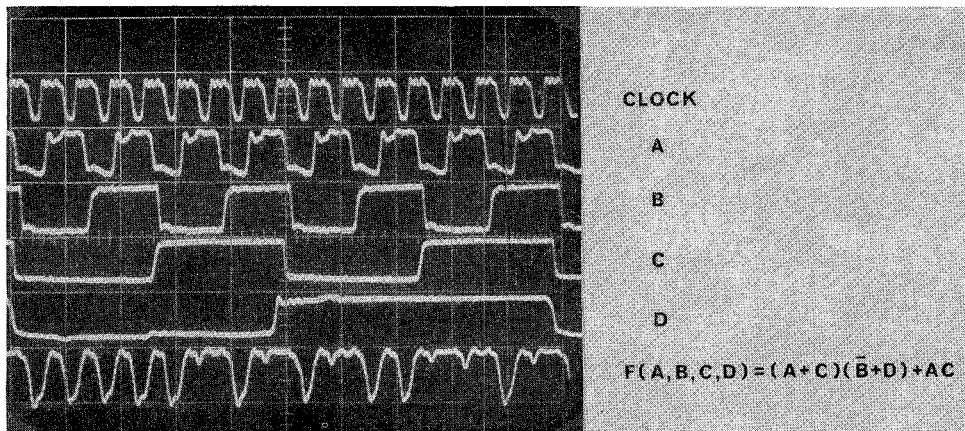
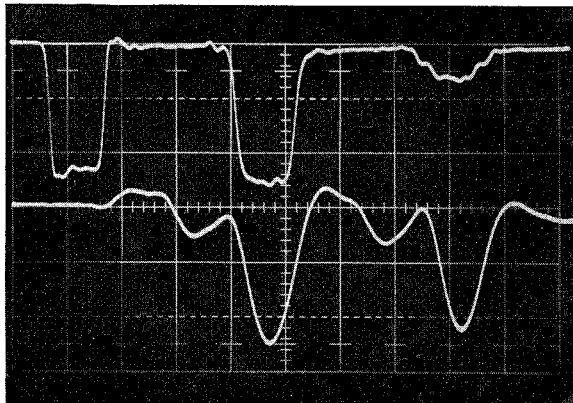


Fig. 4. Output pattern $F(A,B,C,D)$ of the correlation unit when the a_i coefficients are set for the function $F = (A + C)(\bar{B} + D) + AC$. Clock repetition frequency is 50 Mc/sec.



The a_i coefficients are set for the function $F(A,B,C,D) = (A + C)(\bar{B} + D) + AC$, which is in fact the pattern of output clock pulses.

The minimum clock width (5 nsec fwhm) and the output rise, fall and delay times are shown in fig. 5. The double pulse shows minimum clock spacing.

The resolution curves when the correlation unit is

Fig. 5. Clock signal at the input (upper trace) and output (lower trace) of the correlation unit. Vert. : 0.3 V/cm; time scale 5 nsec/cm.

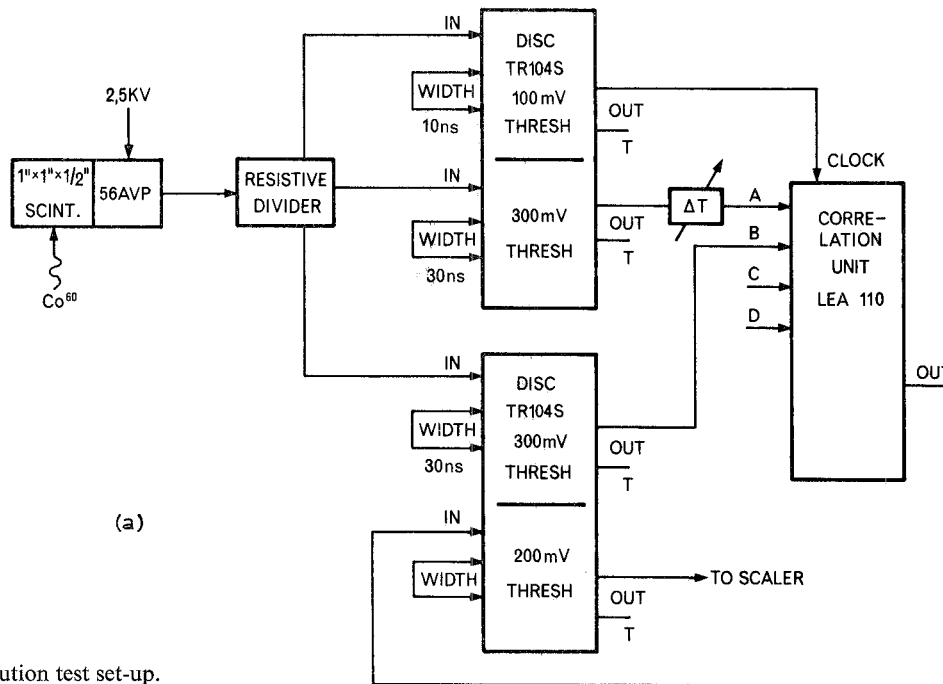


Fig. 6. a. Resolution test set-up.

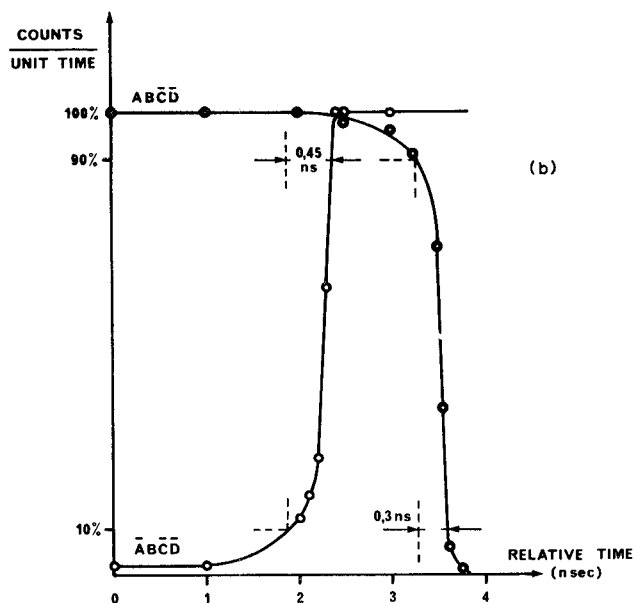


Fig. 6. b. Plot of normalized counting rate vs relative delay.

used as a coincidence or anticoincidence between photomultiplier signals are shown in fig. 6.

5. Conclusion

Having built a medium complexity fast logic module, using suitable integrated circuits, the integrated circuits and the module itself have shown very satisfactory performance.

From a practical point of view the module is neither more costly nor more bulky than a conventional module.

It requires no alignment and is presumably very reliable.

Using the same integrated circuit and techniques, other logic units can be designed.

Thanks are due to Mr. A. Albanesi and Mr. V. Lauta for the careful design of the prototypes.

Reference

¹⁾ E. Schiavuta and F. Soso, Nucl. Instr. and Meth. **60** (1968) 36.

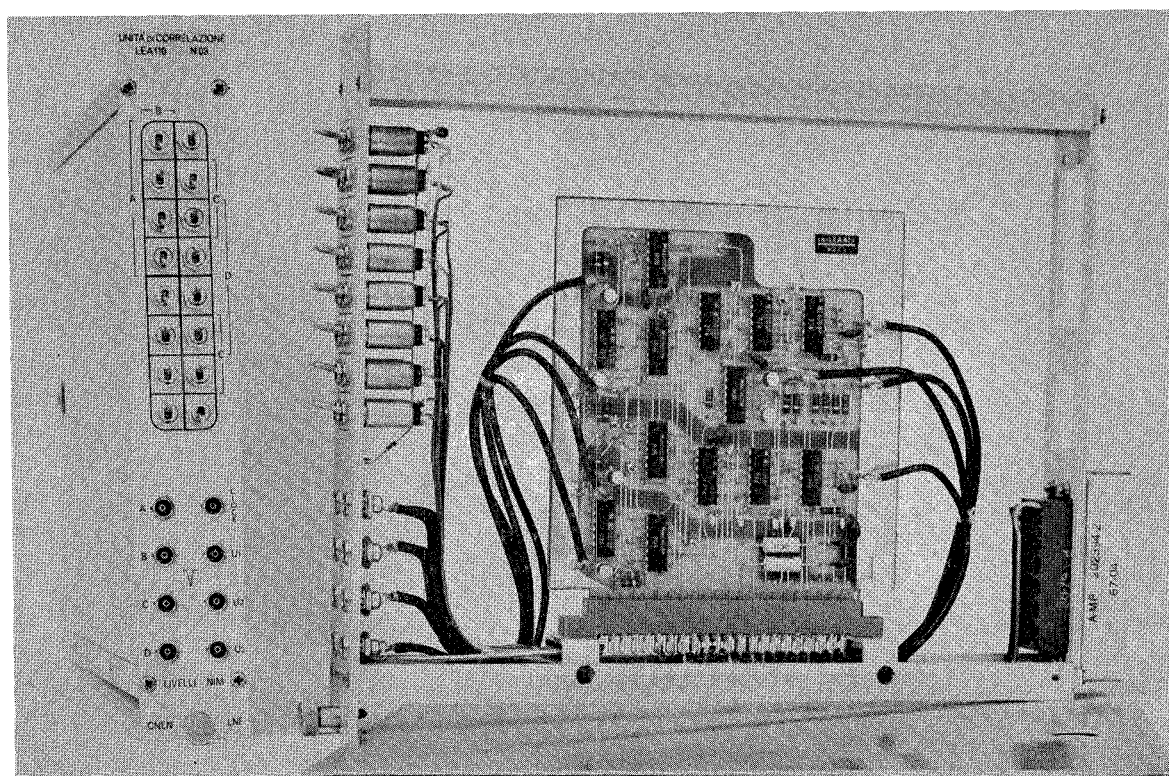


Fig. 7. Front and side view of a correlation unit, NIM module. The a_i switches are arranged in a Veitch diagram, to choose selection of different output functions.