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A GATED LINEAR CHAIN

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The linear chain described here has been studied to process positive current pulses.

The chain can be used as a fast linear gate, when timing and shape information of the pulses have to be preserved, allowing further processing at high repetition rates (up to 20 Mc/sec), or it can be used as a gated integrator with a short dead time.

The gate, which is essentially a current transducer, exhibits a linear response with pulses whose amplitude is ranging from ≈ 0 to about 6 V, with a linearity better than 1%. The pedestal amplitude can be minimized to less than 0.5 mA without affecting the opening and closing times of the gate (≈ 6 ns for 90% transmission of total charge). The signal feed-through is less than 20 mV at an input signal of ≈ 14 V (rise time less than 1 ns).

1. Description of the circuit

A simplified scheme of the gate circuit is given in fig. 1: in the quiescent state the current i_1 flows from the collector of the C.B. T_1 into the emitter of T_2, whose base is clamped to a fixed voltage by the conducting diode D_1. Diodes D_3, D_p are, together with D_1, in the "on" condition, D_2 and D_4 in the "off" one (D_4 is reverse biased with a p.d. $\simeq -2$ V). In these conditions a positive current input signal is transferred through T_1 in the low input impedance of T_2 and no signal appears in the output circuit.

A positive gate signal (length Δt) switches off the emitter current of T_3. Consequently D_1, D_3, D_p and T_2 are turned off, D_2 and D_4 are turned on. Then the current $I_t = i_1 + i_2 - i_4 - i_p$ is switched in the output circuit (through D_4). It gives the pedestal signal and can be minimized by regulating the current i_p. A positive input signal, applied during the time interval Δt, is transferred by the C.B. T_1 to the load, T_2 being now seen as a high impedance (its base emitter junction is short circuited by the conducting diode D_2 at all output voltage levels).

The C.C. transistor T_2, used as gating element, allows a wide input current to be gated by a small current

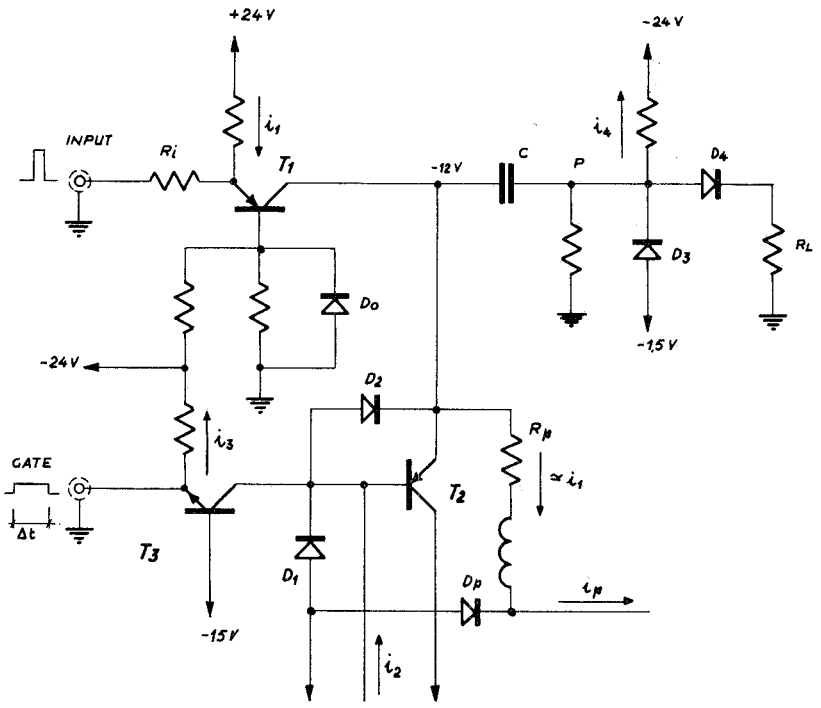


Fig. 1. Simplified scheme of the gate circuit.

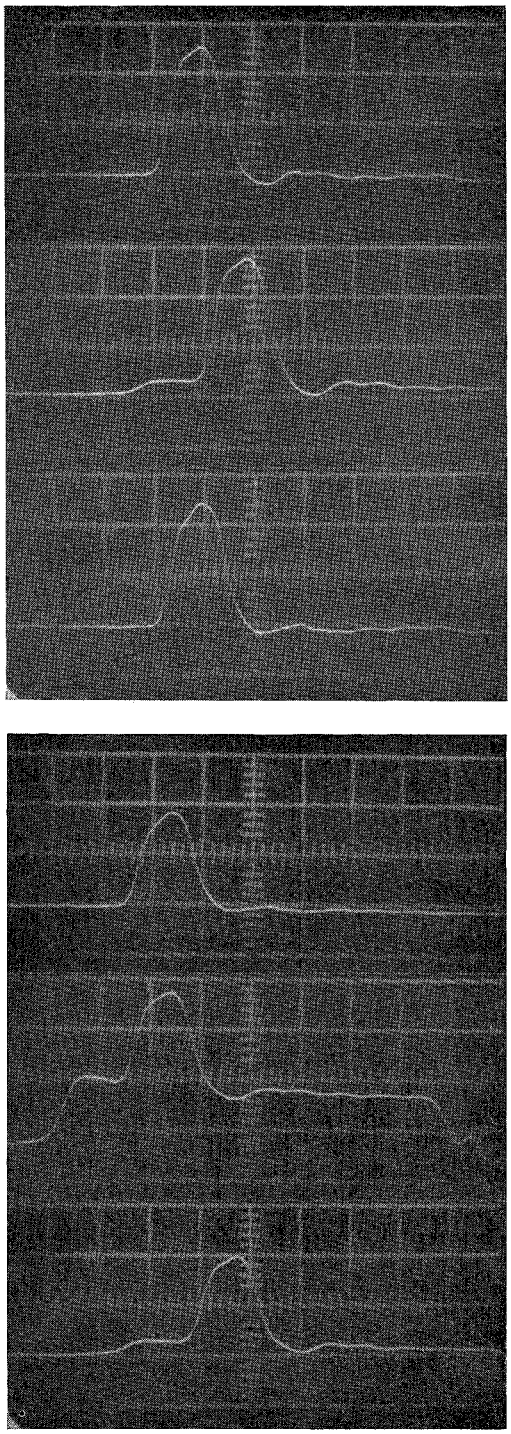


Fig. 2. Response to a 10 ns positive pulse. a. Input; b. Output (uncorrected pedestal); c. Output (corrected pedestal). Scale (a,b,c) hor.: 10 ns/cm; vert.: 1 V/cm. Scale (d,e,f) hor.: 10 ns/cm; vert.: 200 mV/cm.

signal applied to the gate input, as well as the transition off-on to be very fast; this transition is essentially limited by the short storage time of diodes D_1, D_3 and of the emitter-base junction of T_2 and by stray capacities. Diode D_3 and the low input impedance of T_2 allow a fast recovery time (discharge of C) in the "on-off" transition, and, consequently, a good performance at relatively high repetition rates ($\simeq 20$ Mc/sec).

Thus the C.B. T_1 is used as a linear current transducer from the input impedance R_i to a resistive or capacitive load, allowing the processing of very low input current signals too (fig. 2).

The actual complete scheme of the circuit is shown in fig. 3: in the input circuit there is a fast limiter (D_5, T_5), it limits the max. input amplitude to about 6 V. The short delay line ($z = 50\ \Omega$, $\Delta\tau \simeq 2$ ns) has been used to compensate for the delay introduced by D_5 and T_5.

The tunnel diode T_D and transistors T_3, T_4 form a low threshold (≈ 8 mA) monostable univibrator, which gives the gate length, when internal mode of operation has been chosen.

The programming for different gate lengths is available by varying C'. T_6 allows a dc connection to the input gating circuit.

The pedestal amplitude stability is assured when the ± 24 V are well stabilized. The diode D_0 (fig. 1) provides a temperature compensation as well as the zero dc level on the input circuit.

At high repetition rates, the pedestal amplitude stability can be improved by using two C.B. transistors to inject the currents i_2 and i_p.

2. The gated integrator

When the resistive load on the collector of T_1 is replaced by a capacity C'' the circuit becomes a gated integrator. The value of C'' fixes the max. input charge ($V_{C''\,max} \approx 5$ V) and the sensitivity of the integrator (the ratio V_{out}/Q_{in}, Q charge).

A dc coupling to the output of the integrator has been obtained by using transistors T_8, T_9, T_{10}. They guarantee a flat top of the integrated pulse (high input impedance) and a low output impedance. The dc coupling assures no level shifting at max. frequency of the integrator (≈ 1 Mc/sec in fig. 4).

A fast recovery time of C'', discharged by the current from T_{11}, has been obtained by using transistor T_7 together with the diodes D_6, D_7. T_7 gives also a replica of the gated pulse without affecting the integration of the current*.

Fig. 5a shows the output from the integrator, as plotted against the delay time Δt between the input

* This scheme has been previously used by G. White[3]).

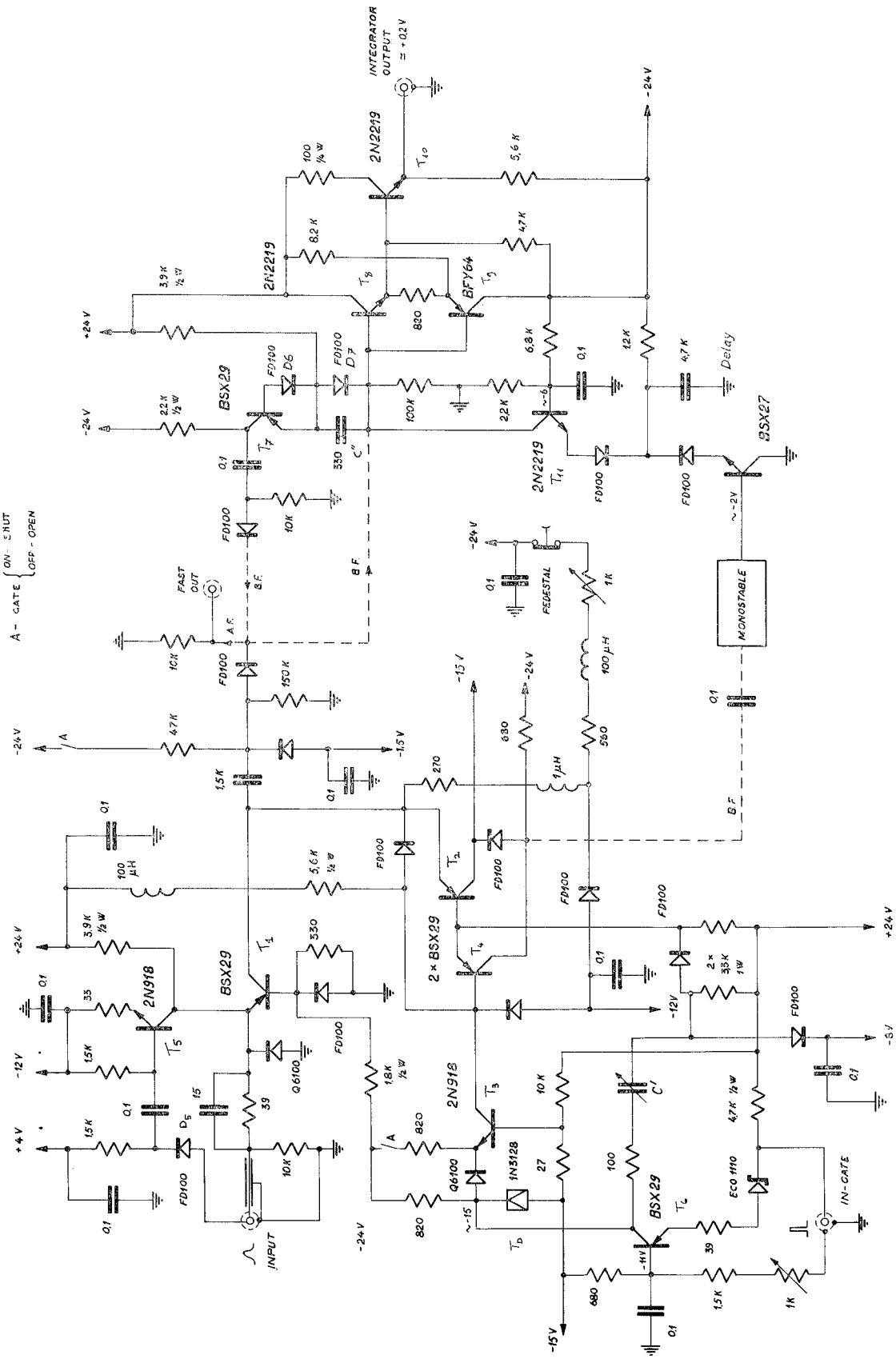


Fig. 3. The complete scheme (gate + internal gate generator + integrator). The dashed lines show the possible configurations: the fast gate and the gated integrator.

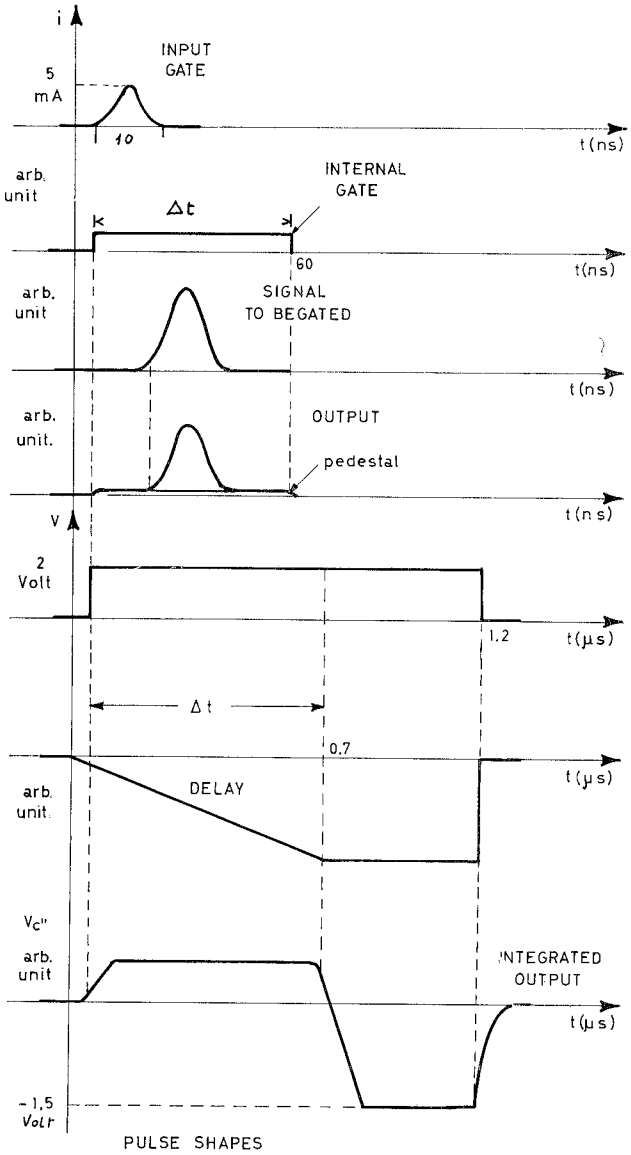


Fig. 4. Pulse shapes in the main points of the circuit.

signal to the gate stretcher and the signal which has to be gated.

Fig. 5b shows the overall response of the Gate + Integrator of fig. 3 as plotted against the amplitude of the gated pulses (the curves have been obtained by using rectangular positive pulses $10 \div 25$ ns wide).

3. Conclusions

The circuit of fig. 2 has been designed and used to work with the positive fast pulses from dynodes of a 56 AVP photomultiplier.

As an example in fig. 5b are shown the measured amplitude spectra of a large scintillation counter (1×1 m^2 plastic scintillator NE 102A, 2 cm thick). They have been obtained by testing this counter with 450 MeV electrons (from the pair spectrometer of the Frascati electronsynchrotron). The three spectra correspond to different thickness of lead, put in front of the counter.

They are the result of some measurements on the possibility of π-e selection with amplitude analysis in the $e^+e^- \rightarrow \pi^+\pi^-$ experiment, which will be performed at Adone[8]).

On this respect it is particularly interesting to derive from the circuit of fig. 1 a fast integrator.

This could be necessary because the pulses from a large scintillation counter are obtained by mixing the output of several photomultipliers which see the scintillator.

The pulses have an irregular shape due essentially to the finite transit time of the light in the scintillator. So an amplitude analysis is better performed on the total charge of the mixed pulses, and a good electronic π-e rejection can be obtained with a fast charge analysis.

This can be performed by feeding a fast discriminator with the voltage pulse amplitude v_C (capacity C in fig. 1), induced by the input current signal. The length of v_C can be programmed and is equal to the gate length.

The author is now interested on this line of work.

The circuit described here doesn't need particularly selected active or passive components. It can be easily designed to work with negative input pulses by replacing each transistor with its complementary, as well as by reversing all diodes and voltages. This can be very

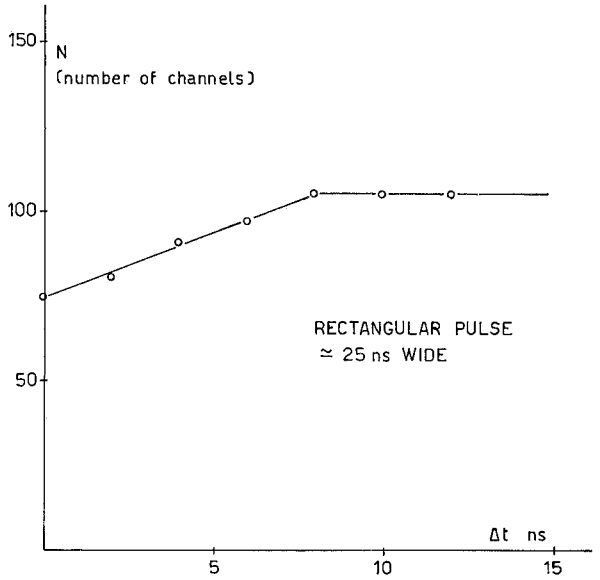
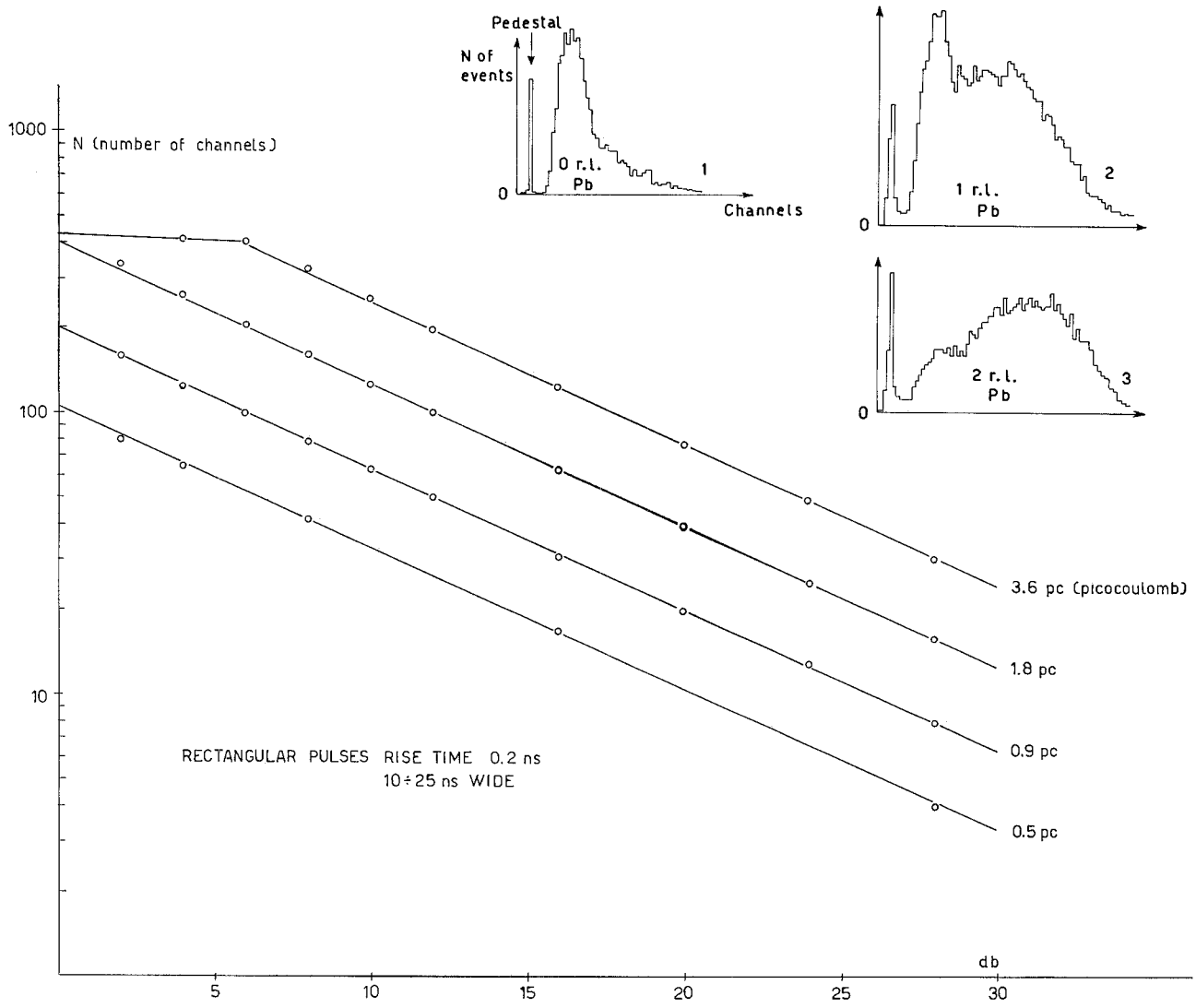


Fig. 5a. The integrator output as a function of the delay between the pulse to be analyzed and the input pulse to the gate stretcher.



5b. The response of the chain (gate + integrator) to rectangular current pulses. Abscissa: attenuation (dB) of the main pulse whose total charge is labeled near each line.
The integrator output voltage pulse has been analyzed, without any amplification, by using a Laben analyzer 1024. The three spectra refer to 0, 1, 2 rad length of lead respectively.

useful when negative pulses with very slow rise time (i.e. from NaI crystal scintillators) have to be processed.

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