Laboratori Nazionali di Frascati

LNF-68/4

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Estratto da : Nuclear Instr. and Meth. 59, 163 (1968)

NUCLEAR INSTRUMENTS AND METHODS 59 (1968) 163–166; © NORTH-HOLLAND PUBLISHING CO.

AUTOEQUALIZING METHOD TO INCREASE THE SPEED OF ANALOG TO DIGITAL CONVERSION*

N. ABBATTISTA, M. COLI and V. L. PLANTAMURA

Istituto di Fisica dell'Universita, Bari, Italy
Laboratori Nazionali del CNEN, Frascati, Italy

Received 11 September 1967

We propose and analyze two methods for analog to digital conversion based on the digital "prevision" of the incoming pulse amplitude in order to obtain a good speed performance (with a 1024 channel converter the expected conversion time is ≈4.2 μsec). Moreover it is possible to obtain a very good differential linearity by the intrinsic capability of two methods to perform a statistical equalization of the channel width.

1. Introduction

The purpose of this paper is to describe a method for A-D conversion with a good speed performance and intrinsic statistical equalization of the channel width[1]). The basic idea is to get a digital prevision of the final value of the amplitude to be measured before analyzing the pulse with conventional methods. Following this way, the measurement is performed only on the difference between the input and the analog conversion of the digital prevision (fig. 1).

Two ways may be followed to carry out a prevision both taking an information from previously analyzed pulses or from the same incoming pulse.

In the first case, the circuit that performs the prevision, the "previsor" would set the register of the ADC on the most probable amplitude on the basis of the previously analyzed amplitudes.

In the second case, one gets the information for the prevision from the leading edge of the incoming pulse or carrying out a parallel rough amplitude measurement. We point out that this rough analysis is a rough one in the sense that it has not to be precise.

2. First method of analysis

First we take into consideration the simple case of a prevision performed on the basis of the previously analyzed pulse amplitude. For clarity sake, let us think of the incoming pulse amplitude to be little different to that registered for the previous event; in this case the "previsor" is the same ADC register that has not been reset after any cycle of analysis.

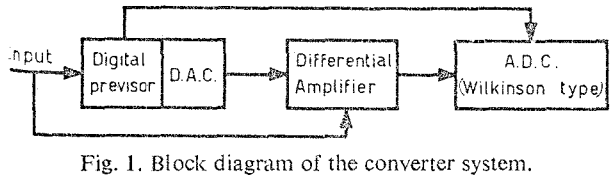


Fig. 1. Block diagram of the converter system.

Now, let us briefly explain how the statistical equalization of the channel width is intrinsically performed (Autoequalization). In fact, the incoming amplitude is measured as a difference whose subtractor is the previously registered amplitude that generally is different from pulse to pulse as for the same input pulse amplitude.

The relative error of the channel width, W_k of the Digital to Analog Converter (DAC) in fig. 2 can be evaluated as follows:

$$W_k = C^{-1}\sum_{i=0}^{k}(\varepsilon_{i+1}-\varepsilon_i)P_i+\sum_{i=k}^{C}(\varepsilon_{i+1}-\varepsilon_i)P_i =$$

$$= C^{-1}\sum_{i=0}^{C}(\varepsilon_{i+1}-\varepsilon_i)P_i, \qquad (k=1,2\ldots C),$$

where

P_i = the probability function that the event will be in the i^{th} channel;
C = the total number of channels;
ε_i = the relative error of the i^{th} level which defines the minimum boundary of the i^{th} channel;
$\varepsilon_{i+1}-\varepsilon_i$ = the relative error of the width of the i^{th} channel.

Then, as W_k is independent from k, the differential linearity of the system is theoretically unaffected by DAC.

The channels of this sytem are equalized on different numbers of the Wilkinson ADC channels; in fact, the first and C^{th} channels interest all the Wilkinson ADC whereas, in the worst case, the $\frac{1}{2}C^{\text{th}}$ channel interest only $\frac{1}{2}C$ channels of the Wilkinson ADC.

Let us now evaluate the time of analysis of the system. Given two consecutive independent pulses X and Y of

* Work supported by CNR – (Patent no. 38649-A/67; August 1967).

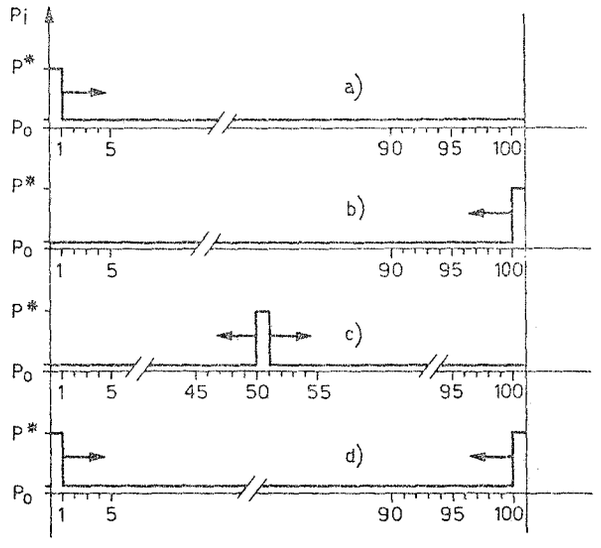


Fig. 2. Probability functions P_i considered for conversion time valuation ($P^*/P_0 = 10$).

amplitude i, k ($i,k = 1,2 \ldots C$) whose probability is respectively $P(i)$ and $P(k)$. Let us consider the difference $|k-i| = j$, that has the following $P^*(j)$ probability function:

$$P^*(j) = \sum_{i,k=1}^{C} P(i) \cdot P(k),$$

or†

$$P^*(j) = \begin{cases} \sum_{s=1}^{C} P^2(s), & \text{for } j = 0, \\ 2 \sum_{-s=1}^{C-j} P(s) \cdot P(s+j), & \text{for } j = 1,2 \ldots C-1. \end{cases}$$

Being the Wilkinson ADC analysis time proportional to the number of the channel in which the event is registered, the expected value of the analysis time of our system is

$$t_1 = T \sum_{j=1}^{C-1} P^*(j) j.$$

The expectation value of the analysis time of a conventional Wilkinson ADC is

$$t_2 = T \sum_{j=1}^{C} P(j) j,$$

where T is the conversion time of one channel.

† To check the approximation of this formula for a finite number of pulses, we have applied a Monte Carlo method for a 100 channels and 2×10^6 total number of pulses. The approximation obtained is better than 10%.

For a uniform probability $P(i)$ function we obtain

$$t_1 = \tfrac{1}{3} T(C^2-1)/C \approx \tfrac{1}{3} TC,$$
$$t_2 = \tfrac{1}{2} T(C+1) \approx \tfrac{1}{2} TC,$$

then the value of the ratio t_1/t_2 is $\approx \frac{2}{3}$.

We see that the analysis time is reduced applying the method herein described.

The t_1/t_2 ratio depends generally on the total channel number and on the shape of the probability P function. The general case can be described referring to the results obtained considering the probability function configuration reported in fig. 2.

We have considered a 100 channel analyzer and a ratio between the peak and background probability equal to ten. The results shown in fig. 3 have been reported vs the number of the channels whose probability is ten times the background moving as the arrows of fig. 2.

We note from fig. 3 that we have generally a reduction of analysis time except in case (a) for a little channel range ($5 \div 25$) of the peak width. Furthermore the value of the ratio is not higher than 1.12 and we can report operatively this situation to case (b) by a simple complementation of the j-difference value.

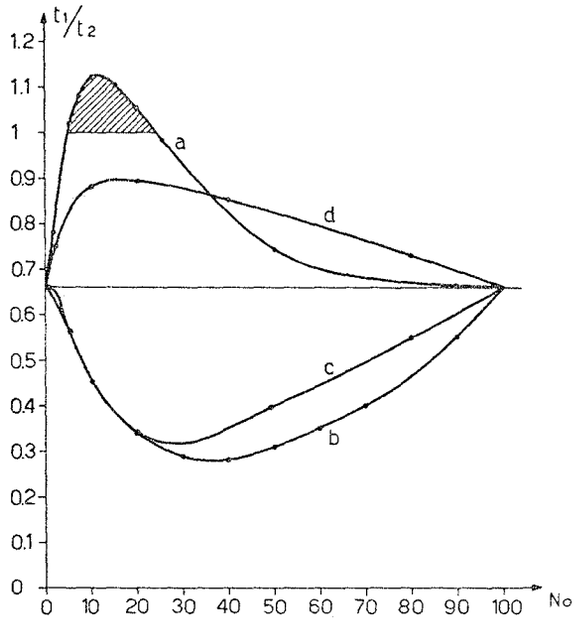


Fig. 3. Time conversion ratio vs N_0 = total number of the channels whose probability is P^*.

The basic scheme of the system that is in progress is shown in fig. 4.

The BR (bilateral register) is never reset so that one input of the AD differential amplifier is always fed by

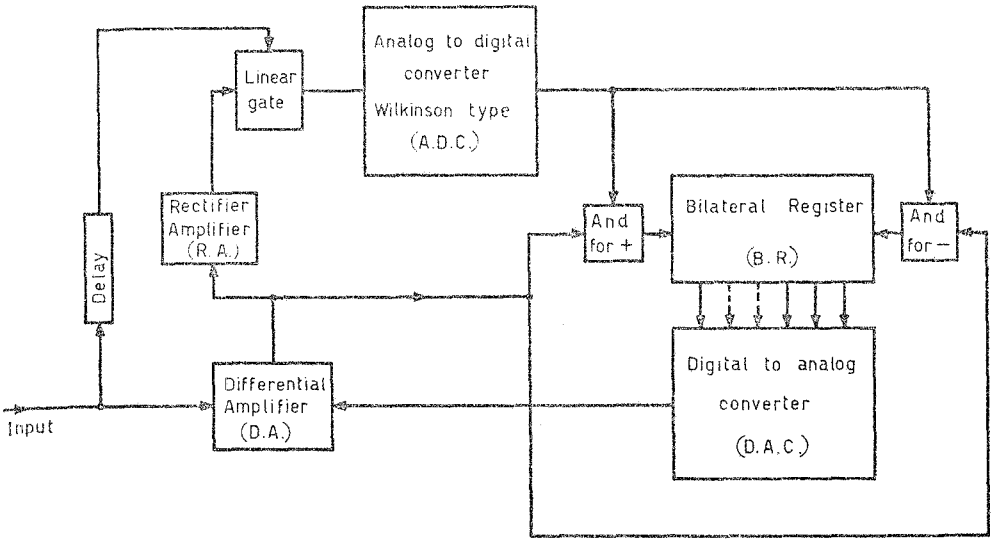


Fig. 4. Block diagram of the first conversion system.

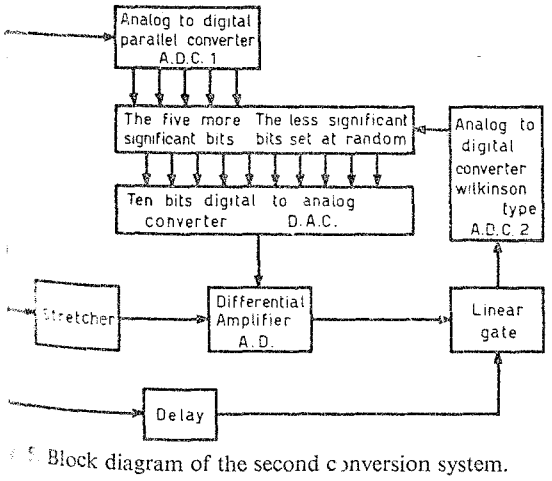
...tal to analog conversion of the last registered ...plitude. The absolute value of the difference ... the previously measured amplitude and that of ...ming pulse is analyzed by the ADC, while the ... sign controls the gates of the BR.

...fferential linearity of the system depends on the ... ADC and on DAC of the "previsor" but the ... capability of the autoequalization reduces the ... also in the actual realization when a finite ... of pulses is coded.

...nd method of analysis

... now consider the case of the prevision per... with a parallel analysis on the incoming pulse. ...k diagram of a $C(1024)$ channels converter is ... fig. 5.

...DC 1 is a parallel converter (multilevel con-



... Block diagram of the second c...nversion system.

verter) providing $C_1(32)$ levels: at the output the rough digital conversion is transferred on the more significant bits ($= \log_2 C_1 = 5$) of the register. The less significant bits are set at random, for example not resetting those after any cycle of analysis.

The ADC 2 Wilkinson converter analyses the difference value between the digital to analog conversion of the register and the input pulse amplitude.

The total number of ADC 2 channels must be theoretically $C_2 = C/C_1$ (32) but, as the precision and the stability of ADC 1 is poor, this number must be light increased and it is obviously expressed by

$$C_2' = C_2(1+x),$$

where x is the differential linearity of ADC 1. Let us now remember that the register of the less significant bits is set at random; as a consequence the output pulse from the differential amplifier may be positive or negative. To avoid the bidirectional register, as done in the block diagram in fig. 5, we must shift the ADC 1 levels over a quantity equal to one channel width. The ADC 2 must then possess a channel number:

$$C_2'' = C_2(2+x),$$

The choice of C_1 is suggested by the following considerations:

a. the total number of channels $C = C_1 C_2$;

b. the total mean time of conversion given by

$$\tau_c = \tau_1 + \tau_2 + \tau_3,$$

where

τ_1 = the ADC 1 conversion time (independent on C_1 number);

τ_2 = DAC conversion time;
$\tau_3 = \frac{1}{2}T/C_2$ is the expected conversion time of the Wilkinson converter fed by a white amplitude distribution;

c. practical limits in the actual realization of the multilevel converter ADC 1;

d. the channel number to which the equalization must be extended.

The channel width autoequalization is effective on C_2 channels as regarding the differential linearity of the DAC, but for the Wilkinson ADC 2 the autoequalization is effective in the worst case on $\frac{1}{2}C_2$ channels. When the autoequalization is effective, τ_3 is further reduced by a factor $\frac{2}{3}$.

Finally we give a numerical evaluation of τ_c for

$$C = 1024;\ C_1 = 32;\ x = 0.25;\ C_2'' = 72.$$

If we suppose to have

$$\tau_1 = 1\ \mu\text{sec};\ \tau_2 = 2\ \mu\text{sec};\ T = 0.05\ \mu\text{sec/channel},$$

we obtain

$$\tau_c = \tau_1 + \tau_2 + \tfrac{2}{3}\left(\tfrac{1}{2}TC_2''\right) = 4.2\ \mu\text{sec}.$$

We can see that the expected performance of the analysis time is a very good one.

4. Conclusions

The interest to increase the speed of analog to digital conversion must be centered on the extensions of the channel number for a high resolution in multiparametrical analysis problems, with a constraint of the dead time of the system. This point of view justifies also the importance we gave to an intrinsic autoequalizing system utilizing a Wilkinson converter.

In our laboratory a work is in progress to check the actual performances of the two proposed systems. Moreover, we have started with the synthesis for the optimum "previsor" to perform the minimum expected time of analysis of the first system we have described in this paper.

Reference

[1]) C. Cottini, E. Gatti and V. Svelto, Nucl. Instr. and Meth. 24 (1963) 241.