

LNF-05/16 (IR)
30 Settembre 2005

**A 32 CHANNELS CHARGE INTEGRATING ADC BASED ON
DIGITAL SIGNAL INTEGRATION**

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Abstract

A digital charge integrator with programmable gate width and range has been designed for use in the KLOE drift chamber front-end chain. The system has a resolution of 9 bits ranging from 600 fC/count up to ≈ 76 pC and integration time ranging from 100 ns to about 13 μ sec. Thirty two channels have been packaged in a single VME 9U board.

1 INTRODUCTION

This paper describes a digital integration technique used for charge measurement in the drift chamber of the KLOE experiment [1]. The integrator input signal is generated by the KLOE drift chamber front end electronics and it is the sum of twelve contiguous sense wires signals belonging to the same chamber layer as shown in fig 1.

The integrator is a 9U VME board that can host up to eight mezzanine cards. Each mezzanine card processes four channels in parallel giving a total amount of 32 channels per board (2).

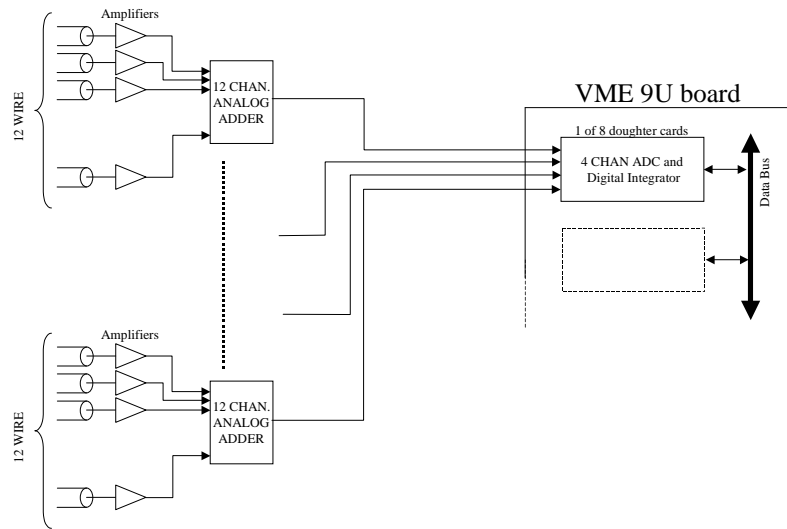


Figure 1: Simplified scheme of the front-end electronics for a set of drift chamber wires.

2 FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the VME 9U main board and mezzanine cards. The board processes 32 drift chamber front end signals. Each integrator channel has its own ADC (Analog to Digital Converter) and DI (Digital Integrator).

The basic operations performed for each channel are:

1. continuous analog shaping of input signal;
2. continuous digitization of the shaped signals at 20 MHz sample rate with eight bits dynamic range;
3. numerical integration of the samples coming from the ADC within a programmable time gate for each valid trigger;

4. range scaling, zero suppression and FIFO data storing of the DI output for each valid trigger;

All channels on the board works in parallel. The FIFO data of the 32 channels are sent to DAQ system by means of a custom interface.

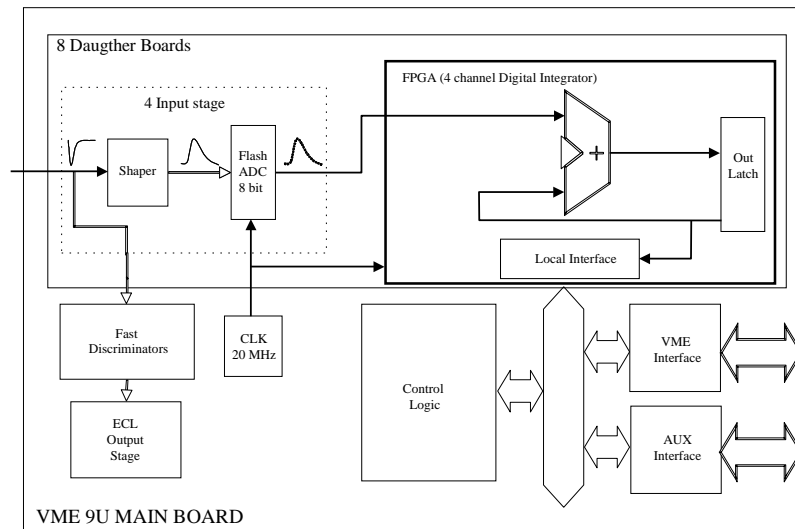


Figure 2: Simplified scheme of the main board and the daughter cards.

3 INPUT SIGNAL SPECIFICATION

Signals coming from the on-chamber electronics arrive to the digital integrator inputs at no fixed time with respect to the trigger signal. Besides the input signal can precede the trigger signal up to 200 ns because of KLOE trigger generation time and cable delay. The time structure of a signal generated by a minimum ionization particle crossing a drift chamber cell is shown in figure 3 (a).

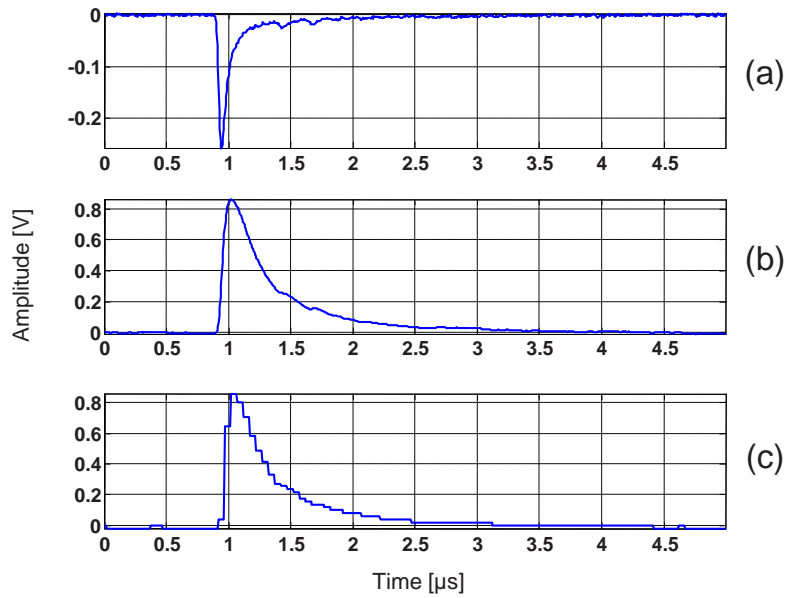


Figure 3: (a) Signal generated by a minimum ionization particle crossing a cell. (b) Output of the antialiasing filter. (c) Output of the analog to digital converter.

4 SHAPER AND ADC

As shown in the previous section the shaper and the ADC of each channel, constitutes the analog part of the board. The shaper acts, on the input signal, as an antialiasing filter, attenuating all the frequencies above half of the sample frequency f_c . A simplified scheme of the shaper is shown in figure 4.

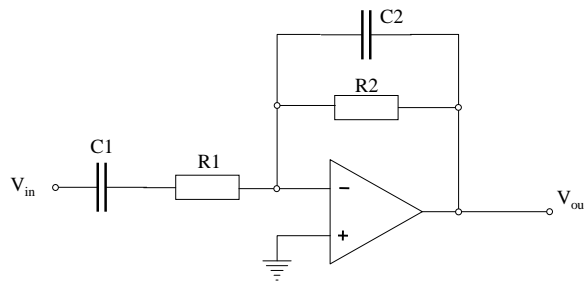


Figure 4: Scheme of the shaper input filter.

Figure 3 (b) shows the output of the filter. A typical ADC output sampled signal is shown in figure 3 (c). Besides the effect on the bandwidth also the polarity of the signal

has been changed as the ADC can manage only positive signals. The transfer function of the filter shown in figure 4, is

$$H(S) = -\frac{SC_1R_2}{(1 + SC_2R_2)(1 + SC_1R_1)} \quad (1)$$

with $R_1 = 1k\Omega$, $C_1 = 10\mu F$, $R_2 = 10k\Omega$ and $C_2 = 15pF$.

Equation 1 represents a second order filter with one zero in the origin of the complex domain and two poles p_1 and p_2 placed respectively at the frequency $f_1 = 1/(2\pi C_1R_1) \simeq 16$ Hz, $f_2 = 1/(2\pi C_2R_2) \simeq 1$ MHz respectively. Modulus and phase of the transfer function are shown in figure 5.

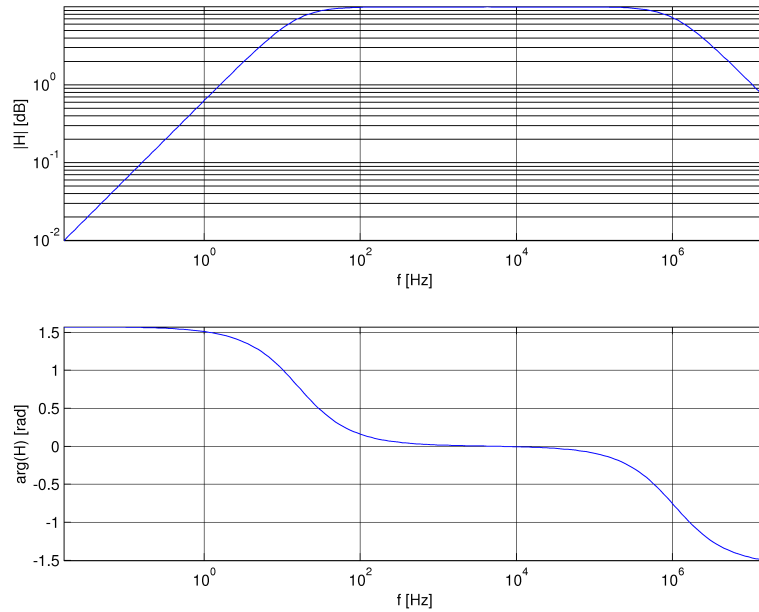


Figure 5: Transfer function of the antialias filter: modulus and phase.

The conversion stage has been implemented by means of an INTERSIL HI1179 ADC. It is an eight bits 35 MSPS (Mega Samples Per Second), CMOS analog to digital converter that use a two-steps parallel method to perform the conversion.

Due to the architecture of the ADC, digital output data are available with a delay of 3 clock cycles (data has to ripple through the stages) allowing to capture signals arriving before the trigger.

The ADC output bus is connected directly to the FPGA that perform the numerical integration.

5 NUMERICAL INTEGRATION

As already said, to integrate the signal coming from the chamber, we use a digital integration technique. A simple schematic diagram of the digital integrator is shown in figure 6 (a). The corresponding transfer function is

$$H(z) = \frac{1}{1 - z^{-1}}. \quad (2)$$

From the equation 2 it can be seen that there is a zero in the origin of the complex plane and a pole right on the unit circle, see figure 6 (b).

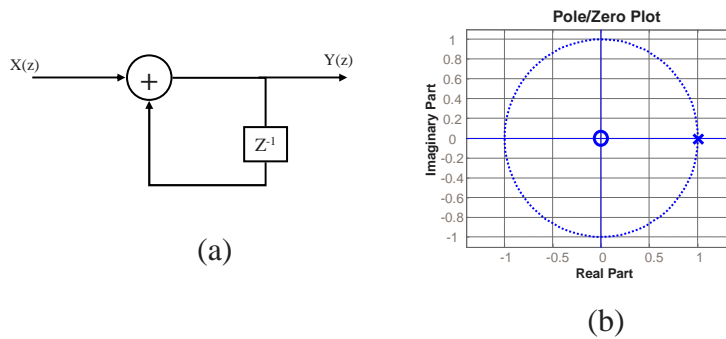


Figure 6: Digital integrator: (a) simplified scheme; (b) zero pole diagram.

Due to the pole position, right on the unit circle, the transient response of the circuit never decay, that is the impulse response of the integrator is a constant. As a consequence after the signal integration has been completed the result is stored in an internal register and the integrator has to be cleared. The integration is performed over a programmable number of samples allowing a variable gate.

The hardware implementation of the digital integrator is made by means of an 8 bits input register, a 16 bits full adder and a 16 bits feedback register that acts even as output register. This configuration allow to sum up to 255 eight bits samples without saturating the integrator, for a maximum gate width of about $13 \mu sec$.

The 16 bits integrator output is scaled into a 9 bits word to match the output bus. The scaling factor is programmable and is done selecting properly a range of 9 bits inside the 16 bits adder output.

Setting a zero scaling factor the integrator has the maximum resolution of $600 fC/count$ ($\approx 307 pC$ full scale). Using the greatest scaling factor the resolution in the measure drops to about $76 pC/count$ ($\approx 40 nC$ full scale).

The integration starts on the rising edge of the Lev-1 trigger signal. After each integration all the registers are cleared before a new trigger signal. The integration result is validated by the second level trigger and then stored in a FIFO hosted on the motherboard. The circuit performances have been measured for different input charges by means of a 1976 LeCroy programmable pulse generator exhibiting a linear response up to 600 pC.

6 On detector studies

The performances of the ADC have been studied with the KLOE drift chamber [1], equipped with two different cell configurations $2 \times 2 \text{ cm}^2$ and $3 \times 3 \text{ cm}^2$, in the following called small and big cells. Each ADC channel collects the signal from twelve cells. The distribution of the collected raw charge as a function of the drift time is shown in fig.7 for small and big cells.

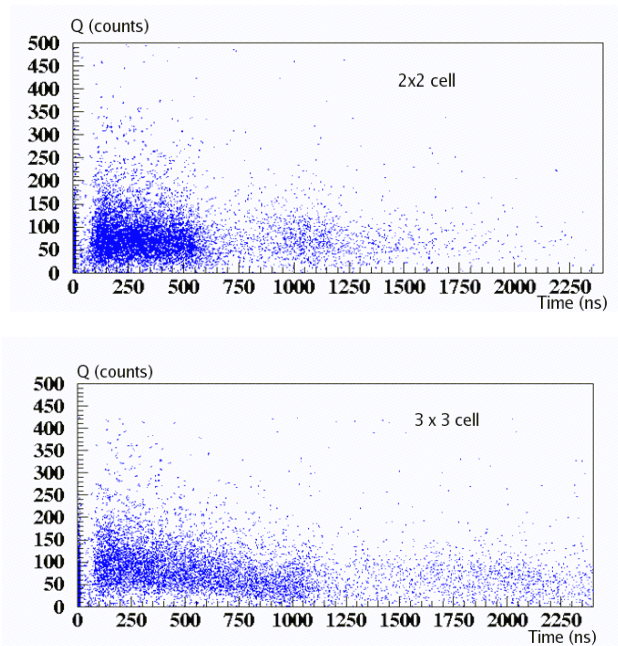


Figure 7: Collected raw charge as a function of the drift time for small cells (top) and big cells (bottom).

The amount of collected charge depends on the particle track length in the crossed cells. Therefore in order to use the charge information for particle identification purposes, it is necessary to normalize the raw charge to the track length (Q/L). The distribution of Q/L as a function of the reconstructed particle momentum p is shown in figure 8.

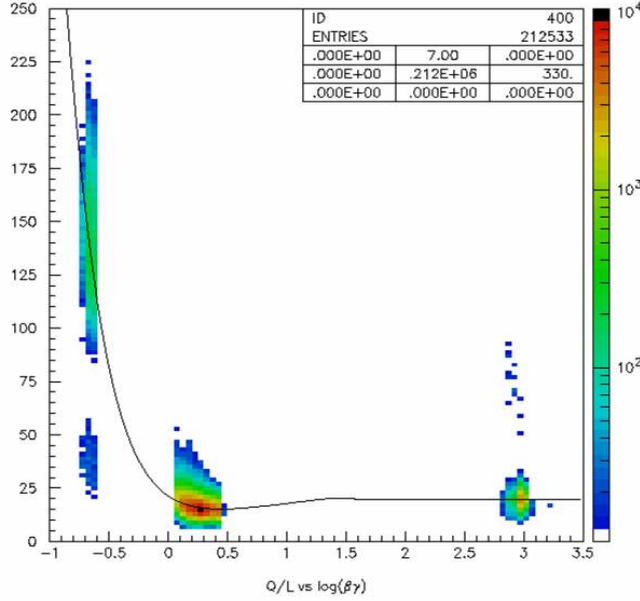


Figure 8: Top: The distribution of the charge normalized to the track length Q/L as a function of the reconstructed particle momentum p . Bottom: Q/L distribution as a function of the logarithm of $\beta\gamma = pm$.

We have selected [2] separate control samples of charged kaons, muons and pions from two-body decays of charged kaons and bhabha events. The distribution of their Q/L value as a function of the logarithm of $\beta\gamma = p/m$, obtained with the appropriate mass hypothesis m , is shown in figure 8 with the Bethe-Block function superimposed. The energy deposited in a sample of finite thickness fluctuates due to the discrete nature of the process. Its distribution departs from a Gaussian approaching a Landau distribution with a long tail towards high energies and therefore the energy deposited must be sampled many times for each track. To improve the energy resolution the truncated mean technique has been used. As pointed out in ref. [3], the 90%He-10% i C10H4 gas mixture exhibits an excellent resolution in the specific ionization (dE/dx) measurement using a 20% truncated mean cut and is competitive with the traditional argon mixtures. In spite of the small number of primary ion pairs of this helium-based mixture, the excellent performances in measuring dE/dx is due to the limited extension of the Landau fluctuations compared with the argon-based mixtures.

The resolution on the specific ionization measurement as a function of the number of samples is shown in fig. 9, for electrons (blue) and pions (red), for tracks orthogonal to the electron beam line.

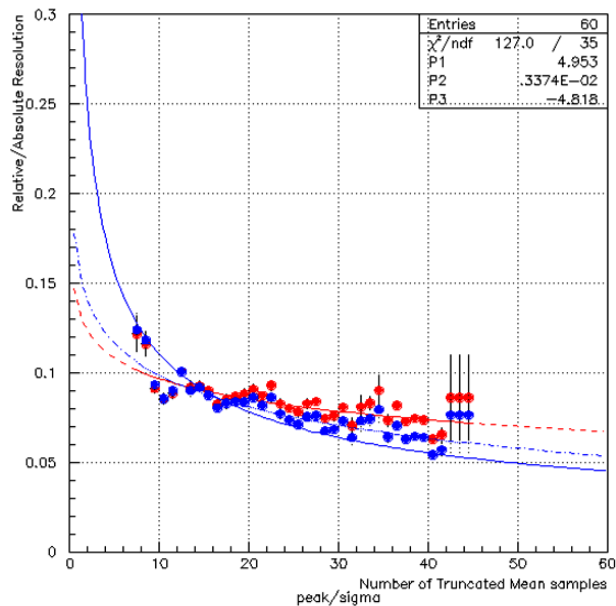


Figure 9: Resolution as a function of the number of samples.

The asymptotic values of the energy resolution for 60 truncated samples are about 6% for pions and 7% for electrons. These results are in agreement with the measurements obtained using the prototypes of the KLOE drift chamber [4,5].

7 Conclusions

An application of hardware implemented numerical integration method for charge measurements has been shown. Digital integration can be easily implemented in programmable logic (FPGA) allowing to simplify ADC design. Moreover it add flexibility to the system allowing to the user to set both range and integration time then matching different experiments requirements.

The ADC have been successfully included in the KLOE data taking and analysis since 2002 and used for particle identification. Given the excellent separation provided by the charge measurement between charged kaons and pions, muons and electrons, a tag procedure to identify charged kaons has been proposed to the collaboration.

References

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