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A POWER SUPPLY STUDY FOR THE RAMPING DIPOLES OF THE SYNCHROTRON RING OF THE CNAO PROJECT

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Abstract

A hadrons (Protons and light Carbon ions) synchrotron accelerator is in construction under the responsibility of the CNAO (Centro Nazionale di Adroterapia Oncologica) and INFN finalized to the therapy of deep tumours. The accelerator complex is composed of two ion sources, a linear accelerator, a low energy and medium energy transfer lines that will transfer the ion beam to the synchrotron ring, where the beams will be accelerated to the prescribed beam energy according to the deep to which the beam energy (Bragg peak) and the dose amount must be released. Only one high energy transfer line is foreseen at this stage of the project. This transfer line will drive the beam to three treatment rooms, corresponding to three horizontal beam lines and one vertical beam line. Additional high energy transfer lines are foreseen in second phase of the project. The synchrotron ring is constituted of 16 H shaped bending dipoles that will accelerated the ion beams till to the requested extraction energy. These bending dipoles must be powered by means of a suitable power supply, 3000 A – 1600 V, that must accomplish the acceleration cycle in less than 1.6 s. The characteristics and performances of such challenging power supply are described in this note. A 24 pulse SCR based topology is proposed, and control circuitry simulations are developed together with a deep analysis of the expected output current shape in terms of current ripple and residual current error.

1 INTRODUCTION

High-energy, ionising radiation has proved to be effective in the treatment of cancerous tumours by causing double-strand breaks in the cell DNA. In particular, hadrons (that is protons and light ions) have the advantageous property of penetrating the body by they initial energy. This is often referred as the Bragg-peak behaviour. The abrupt cut-off of the beam at a controllable depth and the easy penetration compares extremely favourably with conventional radiation techniques using electrons or X-rays that deliver the highest dose at the surface diminishing with depth. The Bragg-peak behaviour offers the possibility of a conformal treatment of deep seated tumours with minimum disturbance to the surrounding tissue. By treating the tumour in layers, defined by the depth of the Bragg peak, and applying collimators and shaped absorbers, a high degree of conformal treatment can be achieved. This

technique is well suited to large tumours and to ones that are difficult to immobilise. A second technique, called active scanning, uses a "pencil" beam to paint the tumour in the three-dimensional space with sub-millimetric accuracy. Longer times with smoother beam spills are required for this type of treatment to facilitate the on-line dosimetry and the accelerator has to produce a well focused beam with a high spatial precision and an exact energy. The primary aim of the project is to design and built a machine that would allow the proton and carbon ions cancer therapy using high precision active scanning. As secondary aim, the machine should also be capable of delivery proton beams by passive scattering. A synchrotron offers the flexibility needed for dual-species operation and the variable energy needed for active scanning. The high rigidity of the ions determines the size and the and the maximum power of the accelerator, while the protons for the passive spreading mode dominate the design of the injection system and the low-energy operation, due to their high space charge. The use of the slow resonant extraction extends the beam spill time sufficiently to perform on-line dosimetry at the patient and to switch the beam on and off according to the dose required. A dedicated foundation, the CNAO Foundation, has been instituted to design and build the CNAO centre, that will be located in Pavia (Italy). INFN's President has signed a collaboration agreement on November 2003, then INFN became co-responsible with CNAO in the construction of the accelerator complex. The collaboration will cover the period 2004-2007, when the CNAO Centre will deliver the first dose to the first patient.
This note describes the characteristics of the power supply for the dipoles of the synchrotron main ring. The control regulation circuitry has been simulated according to the chosen topology, a 24 pulse rectifying circuit, needed to fulfil the challenging performances requested to such a power supply. An output current of 3000 A is requested to accomplish the highest energy treatment cycle, with a total forcing voltage of about 1600 V, for a cycle period of about 1.6 s, with a maximum current ripple of 30 mA, during the injection, acceleration and extraction of the ion beams. The simulations include fault analysis and related protection devices.

2 BRIEF DESCRIPTION OF THE SYSTEM AND GENERAL REQUIREMENTS

This technical note concerns the Power Supply (PS) for the bending magnets of the synchrotron; the magnet layout can be found in Ref.[1]. The total number of magnets is 16 plus 1 that is placed off line and used for magnetic field measurements. The first preliminary electrical data of the magnets and of the connections are summarized in Tab.1. Simulations have been done according to these data. Appendix A and B report last simulations with the final electrical parameters. The magnets must follow a predetermined cycle between a bottom field/current level, according to the injection energy level, depending on the particle type, and a top field/current level, depending on the particular therapy cycle the patient must be subject to.

Table 1 - Magnets and connections characteristics.

N. of Magnets	16+1	All series connected
Resistance of each Magnet*	4.08 mΩ	Total 69.36 mΩ
Inductance of each Magnet*	11 mH	Total 187 mH
Connections length	230 m	Forth-Back and Up-Down
Connections Resistance	2.7 mΩ	6 Cables, 240mm^2, in parallel

* Values updated in Appendix B

The typical cycles, that are by no means exhaustive, are reported in Appendix-A. A cycle consists of:

- A starting bottom level, that is about the 5% of the maximum current level.
- A current/field ramp-up till the injection level, in a fixed time.
- A flat-bottom level during which the particles are injected into the ring.
- A current/field ramp-up till the extraction level, in a fixed time.
- A flat-top level during which the slow extraction takes place and the particles are extracted from the ring; this level does not necessarily coincides with the maximum current level.
- A ramp-up till the maximum field/current value, for a correct magnet "standardization"; no particles are in the ring during this phase of the cycle.
- A ramp-down to the starting bottom level.

The cycle shape, that will last about 1.6 seconds, will be defined according to the treatment plan the patient must be subject to. Obviously, the PS characteristics must be guaranteed only during the first part of the cycle, from injection to the end of the extraction. A typical current cycle is shown in Fig. 1(a) and the related Fourier spectrum is shown in Fig. 1(b). This last one is of fundamental importance and is the starting point to design the passive filter and the feedback loop.

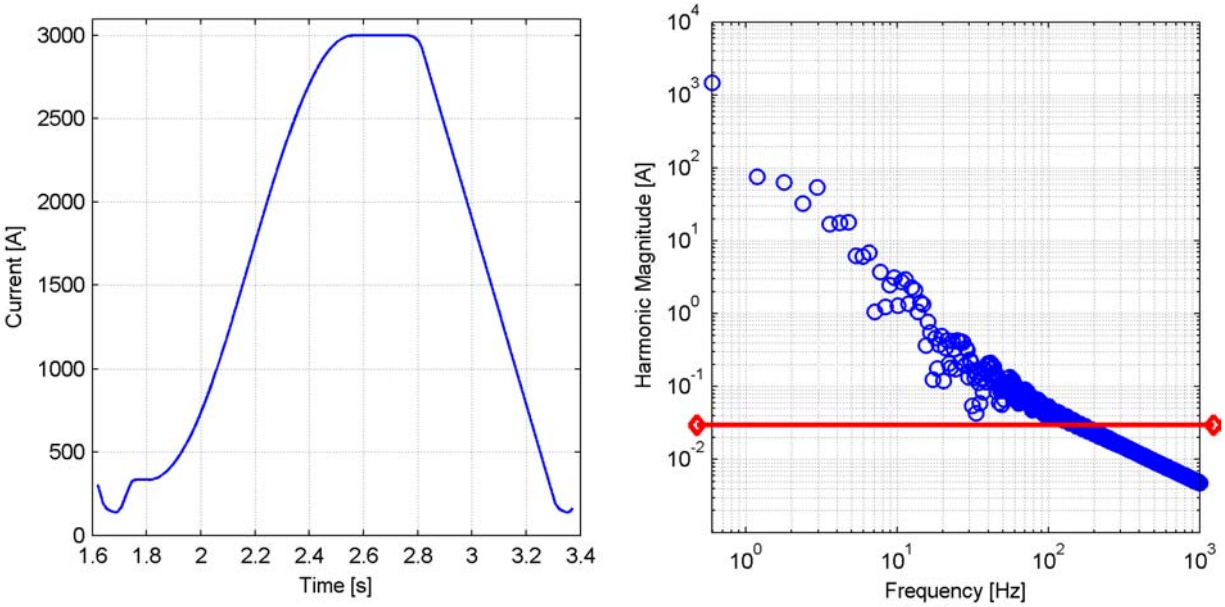

Fig. 1 - Typical current shape (a) and Fourier Analysis (b).

The frequency spectrum has been truncated at 1kHz. It is clearly visible the 0.6Hz component that is the fundamental frequency of the whole waveform (1.6 seconds period). The DC component is not shown due to logarithmic frequency axes. The red line is set to 30mA level that is the maximum allowed error – 10^{-5} of the maximum current of 3000A – and thus a frequency of about 100Hz is calculated. This is the maximum frequency to be considered in reproducing the reference signal with an ideal converter that in principle, for the Nyquist theorem, should have a bandwidth of 200Hz. Moreover, the frequency spectrum takes into account the higher frequencies coming from the linear ramps that are in the current reference waveform. These ramps can be neglected from the point of view of the current error because no particles are present in the synchrotron. In practice, however, a bandwidth of 100-200Hz is still needed, as will be clearer in the following, to get small transient tracking errors.

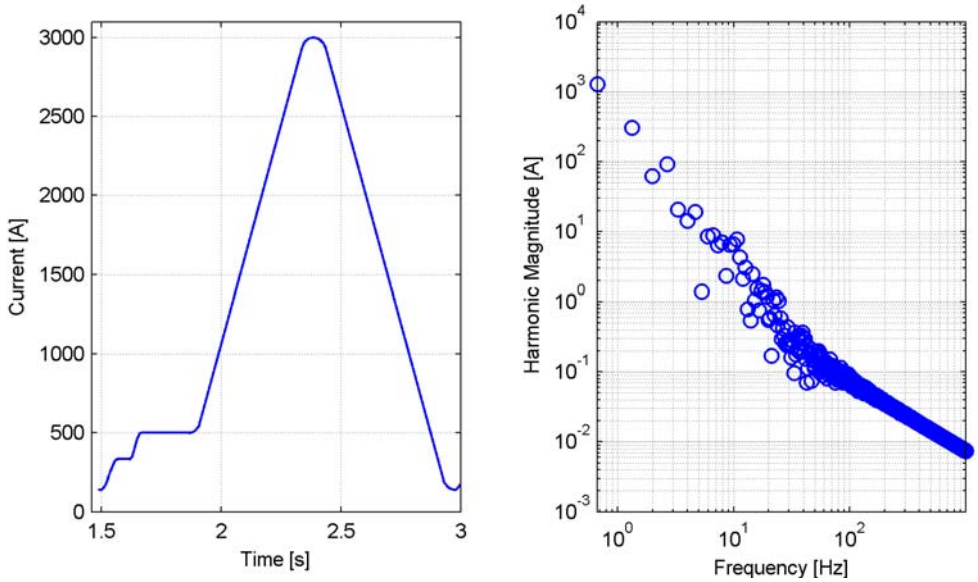

Fig. 2 – $I_{max}/6$ cycle

In Fig. 2 it is also shown the cycle at the minimum extraction level – $I_{max}/6$ or $B_{max}/6$ – that is foreseen for the treatment plan with its relative frequency spectrum. This cycle is important, as will be analysed in detail later, because it stresses to their limits the power supply performances.

Fig. 3(a, b) show the first and second derivative of the current shape of Fig. 1(a). These data are to be taken into account in evaluating the transient response of the system. The current derivatives are responsible of transient errors during fast variation of the reference signal. The reference current should be as smooth as possible and with no discontinuities in the first and second derivatives. It would be advisable in calculating the functions connecting flat-bottoms to flat-tops, to consider a class of maximally flat functions. The current shape considered in the following has not been optimised and should be considered only as an example. The parameters of the feedback circuitry have been calculated, and simulated, on the basis of these considerations.

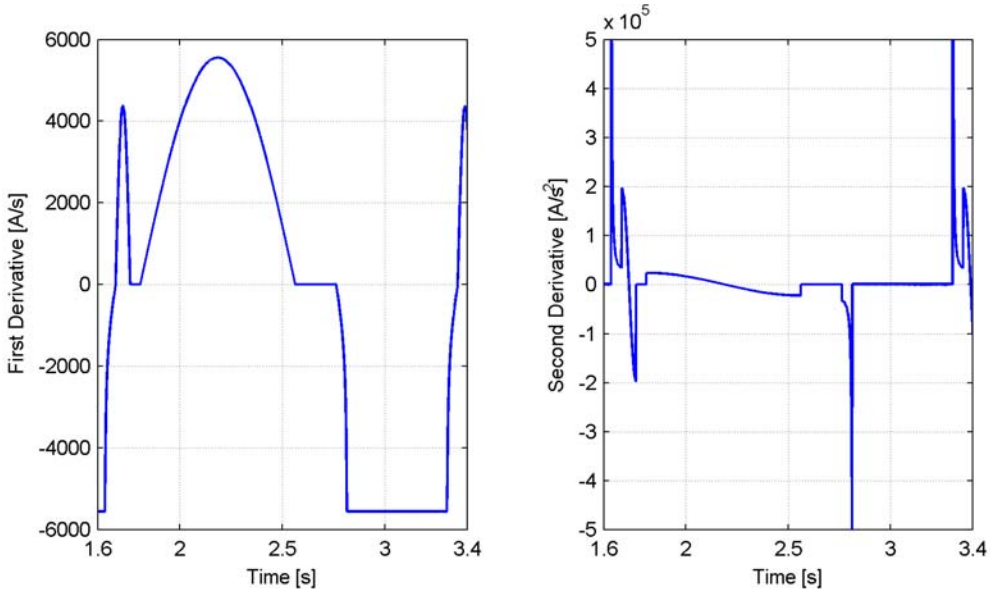

Fig. 3 - First (a) and Second (b) derivative of current shape of Fig.1a

Particular attention has been paid to the selection of the PS topology. In the Specification a 24-pulses two + two bridges in series-parallel connection has been proposed. The main issues that have lead to this choice are:

- ∞ high reliability that is a very important issue for the synchrotron;
- ∞ achieving as low as possible current ripple by increasing switching frequency;
- ∞ reducing harmonic distortion on the mains;
- ∞ improving dynamic performance of the power converter to reduce reference tracking-error by increasing converter frequency.

The last issue, although quite intuitive, needs some detailed explanation. The most critical ramp in the cycles shown in Appendix-A, is the ramp – cosine function – that links the flat-bottom (particle injection) to the flat-top (particle extraction). This part of the cycle has to be reproduced with a very small error (10^{-5} of maximum current), as requested in the specification. Thus, the cosine ramp of Carb2 cycle has been taken into account, as an example, to study the minimum frequency requirements to suite the specification parameters. In Fig. 4(a, b), the current shape that can be achieved with an ideal 12-pulse converter output voltage step function is shown; being this the best current shape that can be achieved in purely theoretical conditions of no voltage ripple and perfect synchronization of driving signals. The current reference signal could be tracked by generation of well determined output voltage steps, giving as a result a linear current ramp from one step to the other. So, in the theoretical hypothesis of having an ideal voltage source, free of ripple and noise, with a conventional 12-pulse rectifier, and thus a "cut-off frequency", due to a sort of sampling frequency limit, of 600Hz, the current can be followed and corrected every 1.6ms (see the dotted line in Fig. 4b). The error is shown in Fig. 5a, and magnified in Fig. 5b. The per-unit error has a magnitude of $3*10^{-6}$. Considering that actual power converter output voltage is not ripple free and that feedbacks are always affected by noise, it is necessary to increase the commutation frequency. Thus, 24-pulses converter is mandatory. The new curves are shown in Fig. 6(a, b) and Fig. 7(a, b). The error is a factor 3 less than in the 12-pulse configuration, giving a reasonable safety margin.

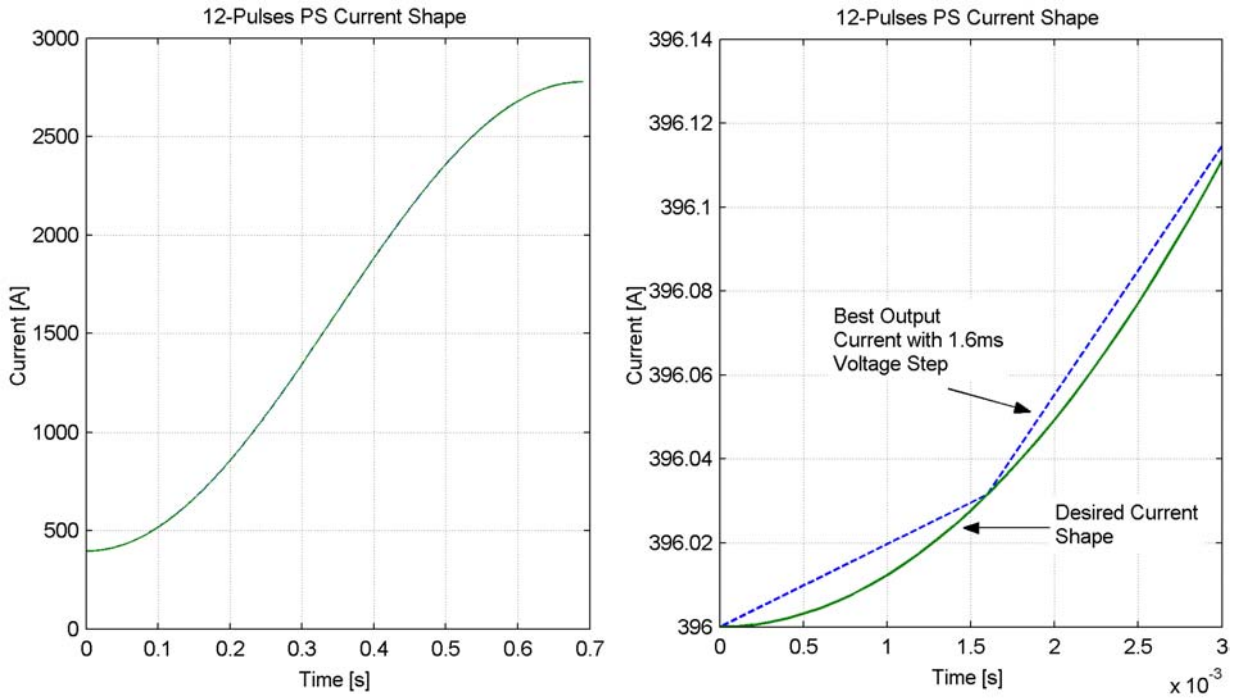

Fig. 4 - Twelve Pulses Tracking of Reference Current.

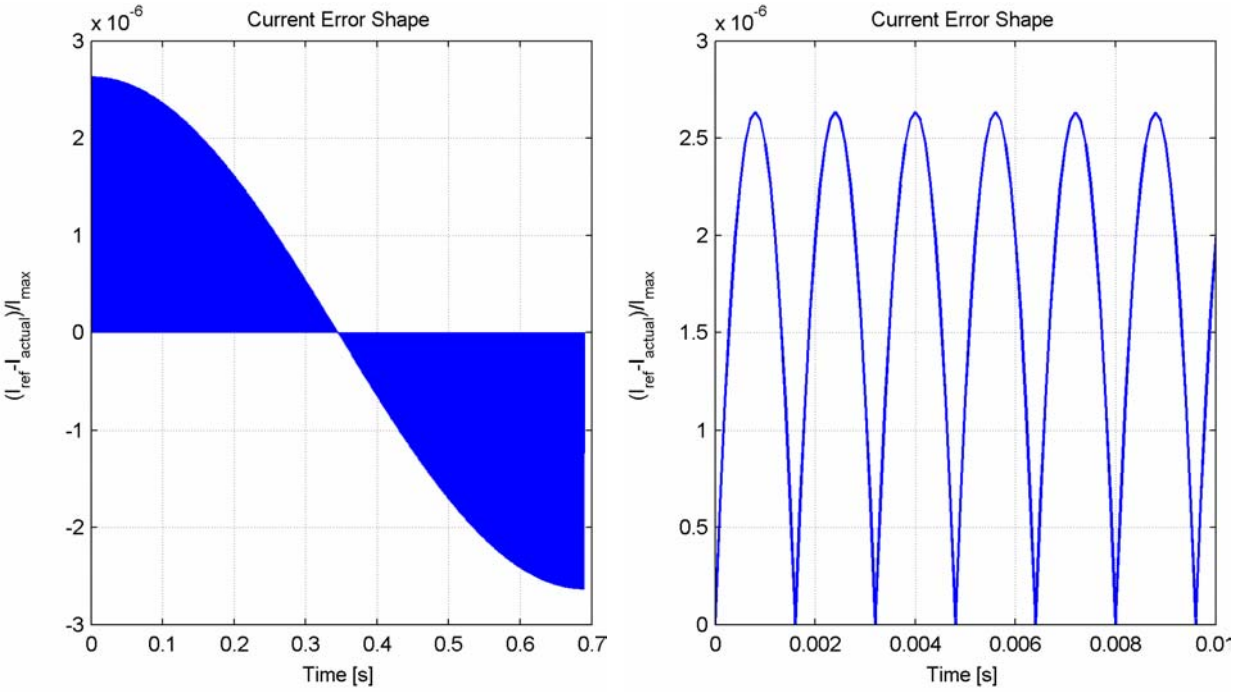

Fig. 5- Twelve Pulses Tracking error of Reference Current.

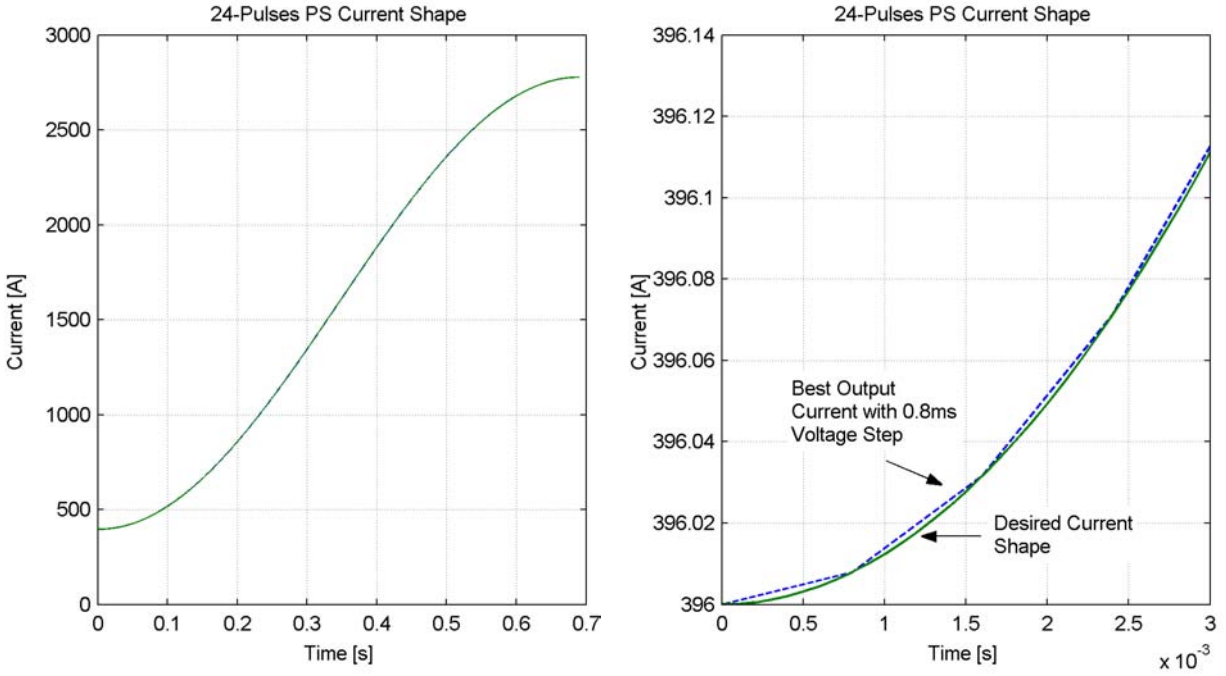

Fig. 6 - Twenty Four Pulses Tracking of Reference Current.

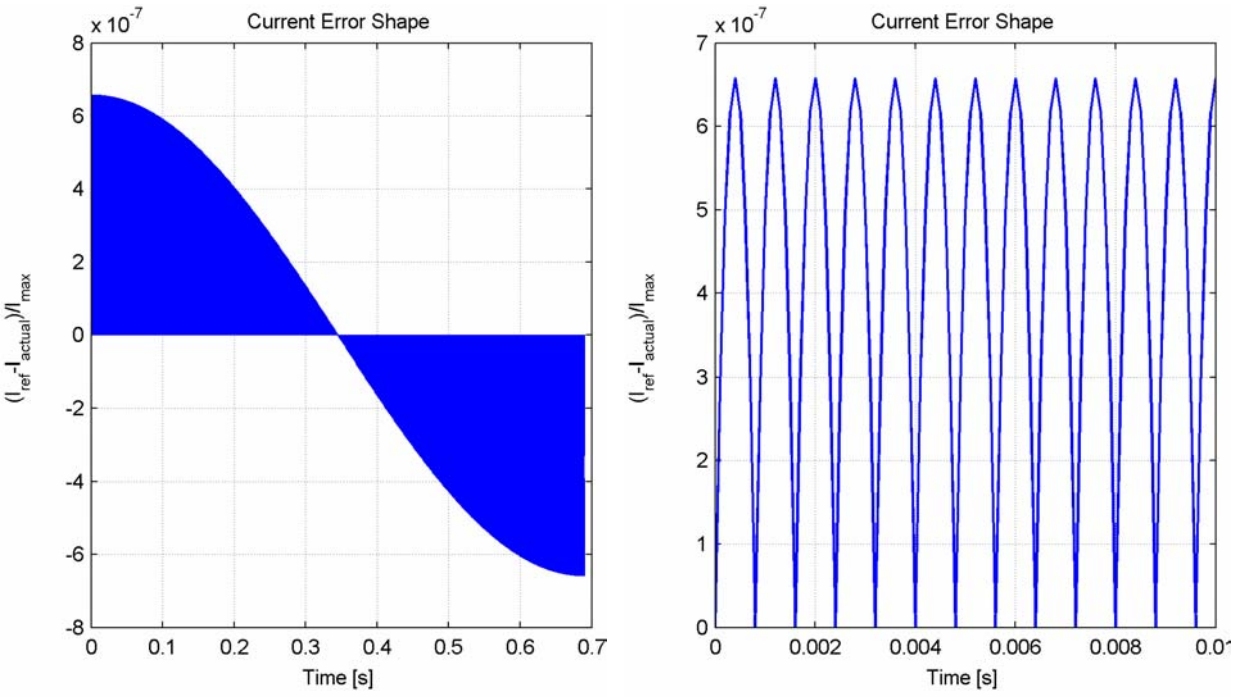

Fig. 7 - Twenty Four Pulses Tracking error of Reference Current.

3 ELECTRICAL PARAMETERS

This section describes how the parameters of the system, simulated with Simulink-MATLAB [4], have been calculated. The Simulink scheme has been drawn in Fig. 8 with the detailed sub-schemes in Fig. 9 and Fig. 10. For the simulation it has been assumed an almost infinity short-circuit power from mains. In particular two identical three-phase sources, phase shifted of 15 degrees, have been used to simulate, together with the Y-y-d transformers, the four three-phase voltage sequences shifted in phase of 15 degrees, to feed the thyristor

bridges. This was necessary because the DY-dy-dy transformer configuration was not implemented in the available Simulink version. The results of simulation are not affected by this choice.

However, the transformers parameters have been calculated as follows and a detailed analysis can be found in Appendix B.

$$\left(K_{rect} \cdot K_{ac,\min} \cdot V_s - K_{cdt} \cdot V_s\right) \cdot 2 = V_{d,\max} \Rightarrow V_s = \frac{1}{2} \cdot \frac{V_{d,\max}}{1.35 \cdot 0.9 - 0.1} \cdot 680V, \qquad (1)$$

where, V_s is the phase-to-phase transformer secondary voltage; K_{cdt} is the safety factor in which are estimated the voltage drops and regulation margins; K_{rect} is the rectifying constant, and $K_{ac,min}$ takes into account the minimum allowable line voltage; $V_{d,max}$ is the maximum DC voltage requested by the load that has been set to 1500V. The maximum RMS current of one secondary have been estimated as follows:

$$I_s = \frac{I_{d,\max}}{2} \cdot \sqrt{\frac{2}{3}} = 1224\,A, \qquad (2)$$

where the symbols have an obvious meaning. Thus, the apparent power of one transformer, considered as the sum of two secondary feeding the two bridges in series, can be estimated as:

$$S_n = 2 \cdot \sqrt{3} \cdot V_s \cdot I_s = 2.9\,MVA \qquad (3)$$

The following per-unit values have been considered as parameters of each three-winding transformer, and implemented in the simulation:

$$\dot{v}_{cc} = 0.07$$

$$\dot{z}_{cc} = 0.07 \;\; considering: Z_n = \frac{S_n}{3 \cdot I_n^2} = \frac{S_n}{3 \cdot (2 \cdot I_s)^2} \qquad (4)$$

$$\dot{P}_{cc} = 0.02$$

where, $\dot{v}_{cc}, \dot{z}_{cc}, \dot{P}_{cc}$ are the short-circuit voltage, the short-circuit impedance, and the short-circuit power losses respectively.

The L-C filter has been implemented taking into account the following guidelines:

- filter inductance must have a suitable value to make the bridges working in continuous conduction mode even at the lowest current level (5% of maximum);
- capacitor C1 must have a value so that the filter has a flat response in the frequency range requested by dynamic needs, although this is in some contrast with voltage ripple smoothing;
- capacitor C2 has been added to configure a classical Praeg filter that strongly reduces the thyristors switching frequencies. Its value has not been optimised, but simulations have shown that suitable values are much smaller than the ones usually adopted in conventional non-ramping PS. Thus, a careful evaluation of the capacitors values must be done by the builders to fulfil the technical needs such as avoiding undesirable oscillations and balancing sizing parameters of L-C filter and active filter.

The smoothing filter has been designed according to following parameters and equations:

$$\left.\begin{array}{l} L_f = 401 \propto H \ \text{single filter} \\ \qquad\qquad \textit{inductor value} \\ C_1 = 7.7\,mF \quad \textit{main capacitor} \\ C_2 = 385 \propto F \ \text{second order} \\ \qquad\qquad \text{capacitor} \end{array}\right\rangle \begin{array}{l} \infty_t = \dfrac{1}{\sqrt{\dfrac{(2L_f)}{2} \propto (C_1 + C_2)}} = 88\,Hz; \\ R_d = 3 \infty \sqrt{\dfrac{2L_f}{(C_1 + C_2)}} = 0.94 \end{array} \qquad (5)$$

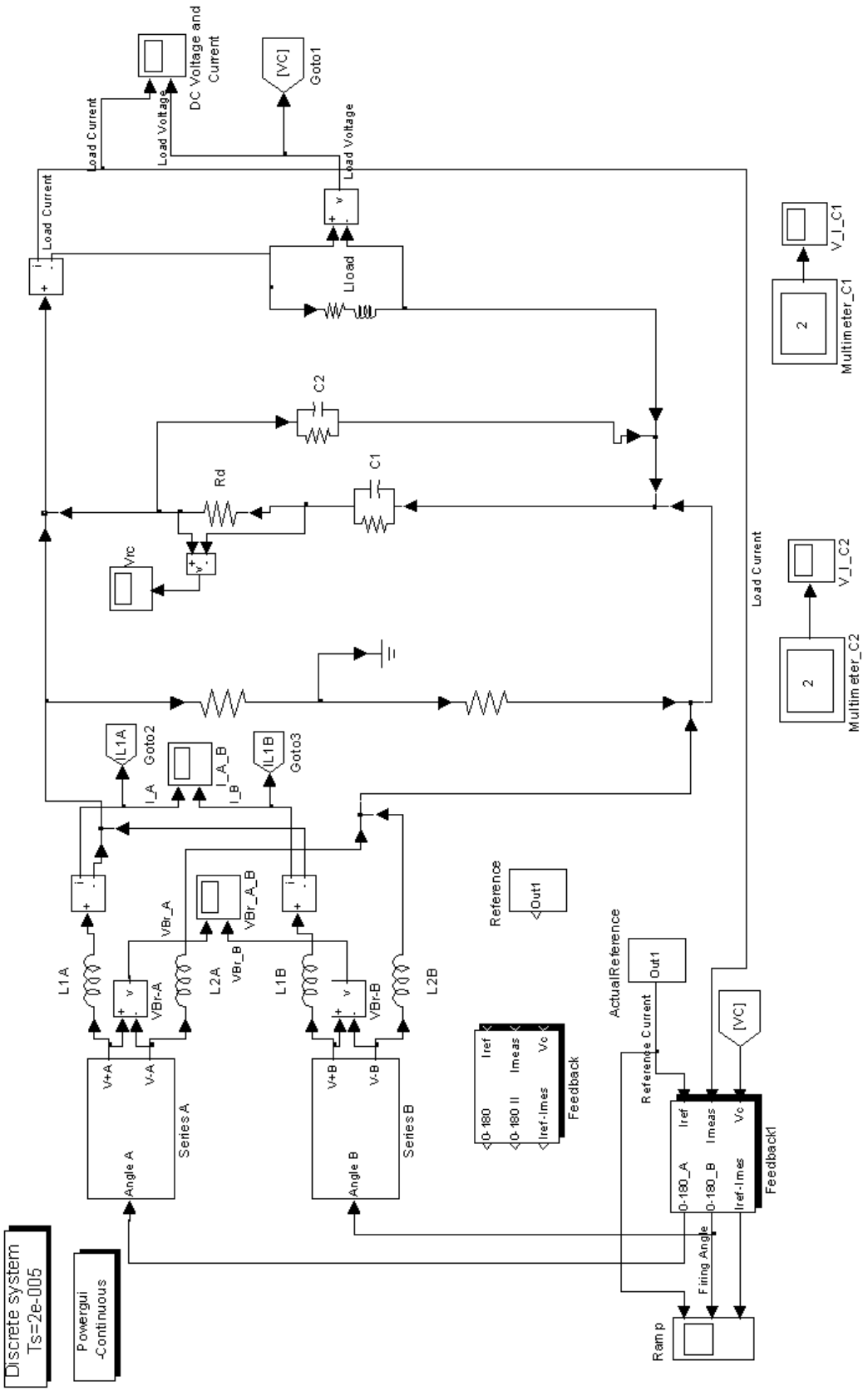

Fig. 8 - Simulink implementation of 24-pulses power supply.

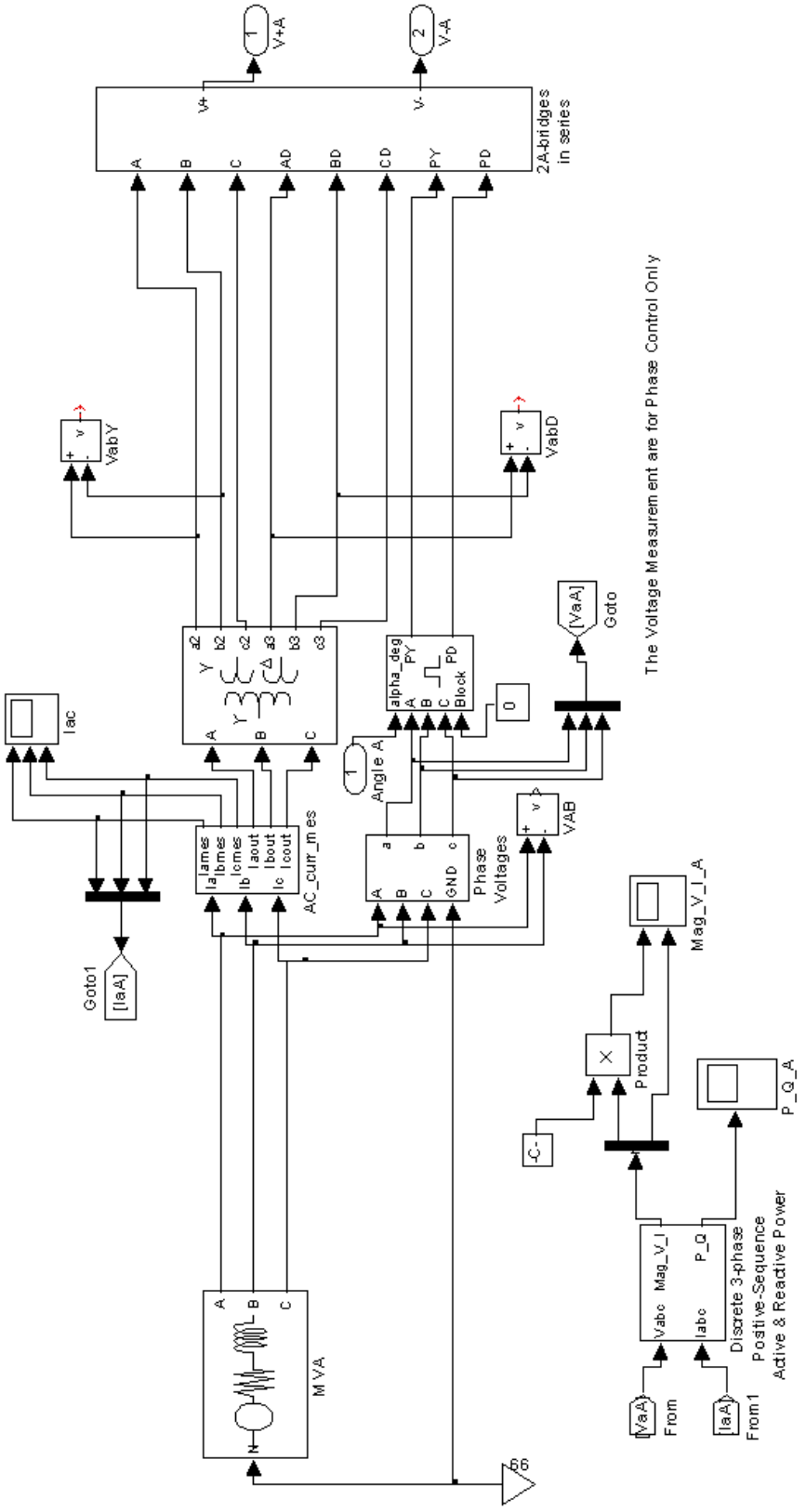

Fig. 9 - Power Transformer for series connected bridges.

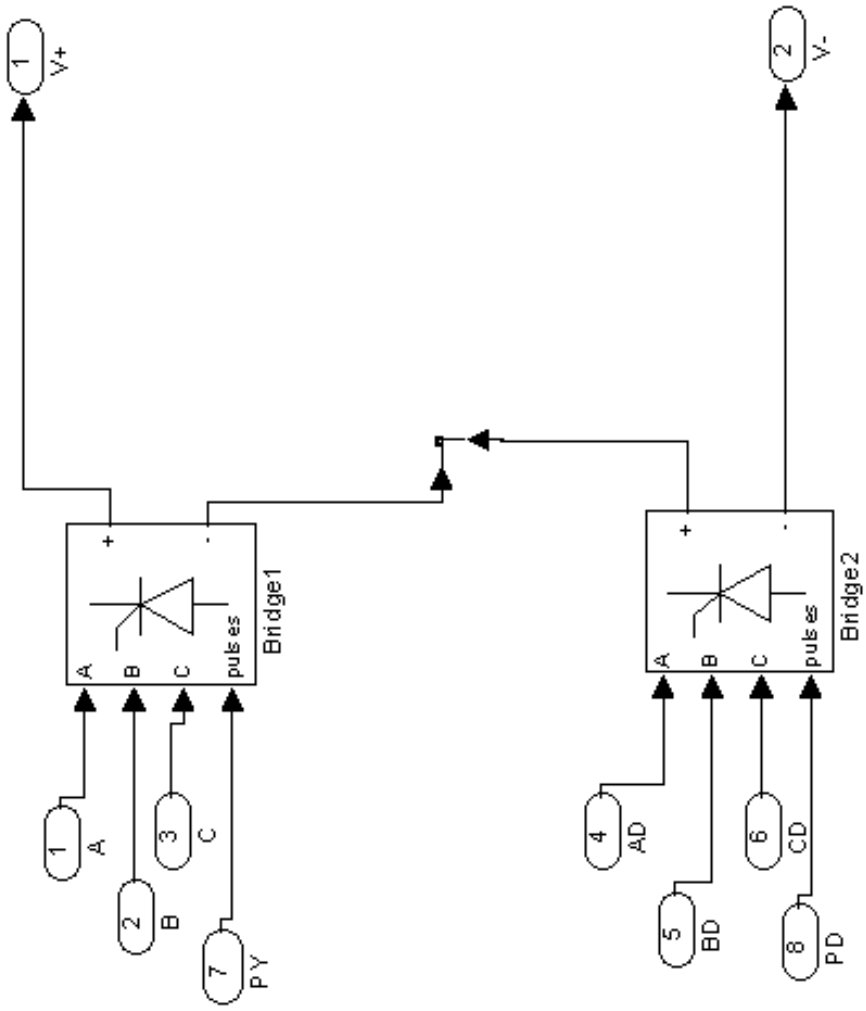

Fig. 10 - Series connected thyristor bridges.

The analytical transfer function of the filter, load included, has been calculated. The trans-conductance and phase variation of the transfer functions I_{load}/V_{input} are shown in Fig. 11 as function of the frequency, in the following situations: a) no LC filter, b) only C1 and c) C1+C2. The attenuation and phase variation of the transfer function V_{load}/V_{input}, are shown in Fig. 12. Although it is a common choice the use of the so called Praeg Filter using a relatively small capacitor C2 in parallel to the damped large capacitor C1 to improve ripple attenuation, as will be clearer in the following, its use in the design of the analysed power supply may pose stability problems. A solution, developed in the following, like the use of a state filter, could provide the required attenuation without degrading stability margins.

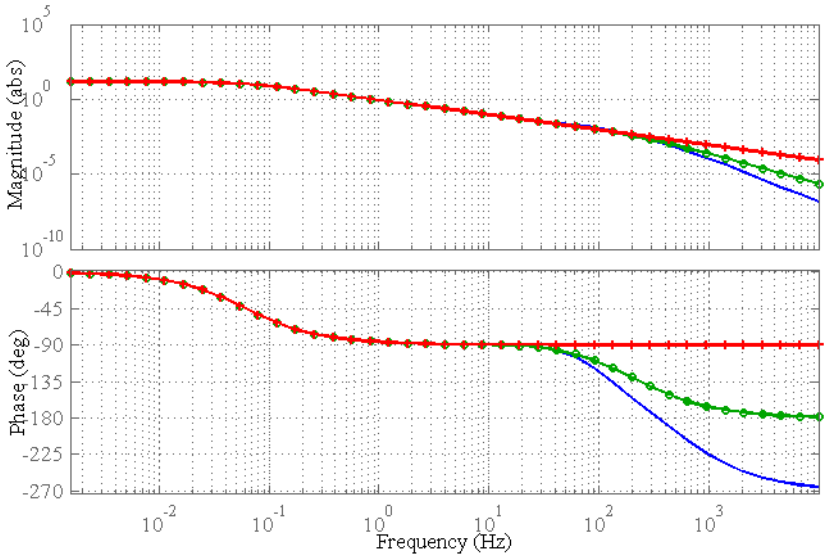

Fig. 11 - Output Current/Input Voltage transfer function of open loop system. Solid Line: C1+C2 – Circle: C2=0 – Plus: No low-pass filter.

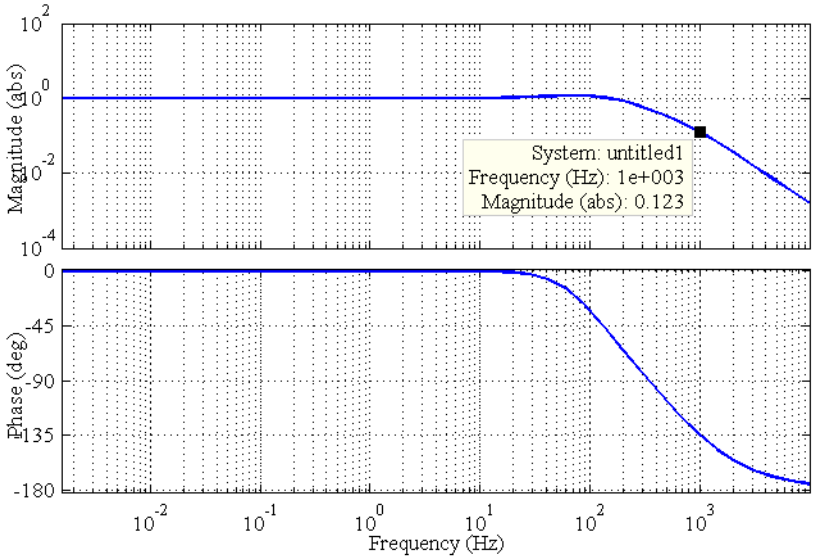

Fig. 12 - Output Voltage/Input Voltage transfer function.

In the simulation also the thyristors snubbers have been considered as well. Due to the impossibility of representing a detailed model of actual components, the RC-snubber network has been calculated with approximated formulae; the results are in agreement with values found in technical literature. The parameters used in the simulation are:

$$R_{sb} = 33\,\Big|\;; C_{sb} = 1 \propto F\,, \tag{6}$$

and the circuit parameters:

$$L_{trafo} = .5\,mH\,; \frac{\partial i_T}{\partial t} = 1\,A/\propto s\,; \frac{V_{\max}}{\hat{V}_{ac}} = 1.2\,. \tag{7}$$

where, $\partial i_T / \partial t$ is the rate of fall of the on-state current.

The maximum continuous average current is:

$$I_{AVM} = \frac{I_{DC\max}}{N_p \cdot N_{Ph}}, \qquad (8)$$

where N_p is the number of bridges in parallel, and N_{Ph} is the number of phases. Applying a suitable safety factor, chosen to be 3, for the current rating of the thyristors, the maximum average current for a 120° conduction angle is:

$$I_{TAVM} \geq 3 \cdot \frac{3000}{2 \cdot 3} = 1500\,A. \qquad (9)$$

Thyristors like Powerex 2200V-1800A TA 20 or WESTCODE N600SH12-16 should be the right ones provided that the value of the case temperature is not exceeded.

4 FEEDBACK CHARACTERISTICS

The four thyristor bridges, have been controlled by the use of suitable feedback implemented in the simulation. Taking into account that the active filter is not considered at this stage, a control system described in Fig. 14 has been used. As can be seen, a double PI (in the following PII) has been the first choice to achieve zero error immediately after the ramp start-up transient. In Fig. 14 a Forward Compensation is also shown because the second type of controller (in the following FCC) that has been used, is a single PI (thus without the K_{II} gain in the figure) with a forward compensation network. Frequency and time responses of this two feedback systems are compared in the following. It should be noted that the two controller typologies analysed in this note are not completely optimised and they are only two of the many possible choices. They are only meant as examples to point out the problems involved in the design of a suitable feedback.

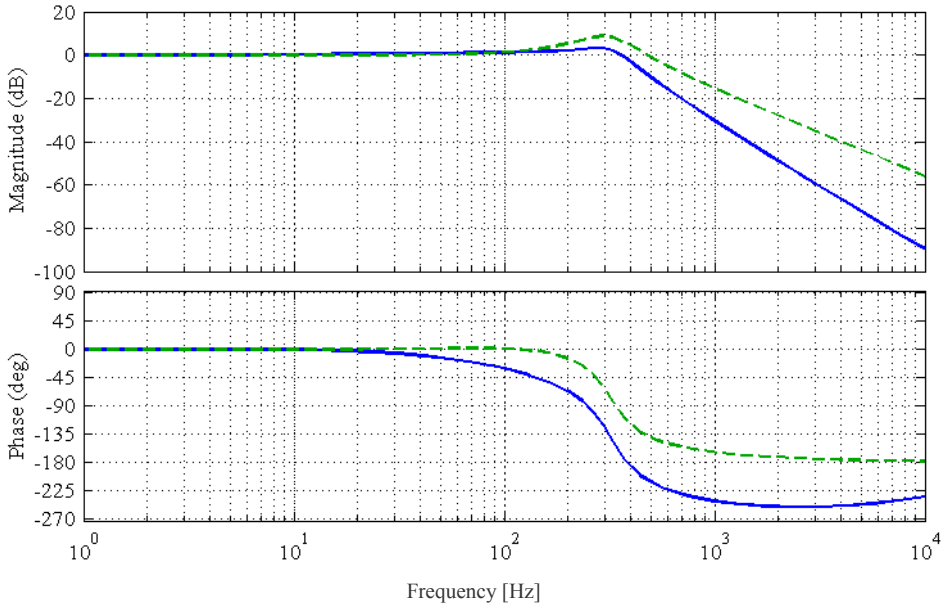

Fig. 13 - Solid Line: I_{out}/I_{ref} transfer function with PII, Dashed Line: I_{out}/I_{ref} transfer function with FCC.

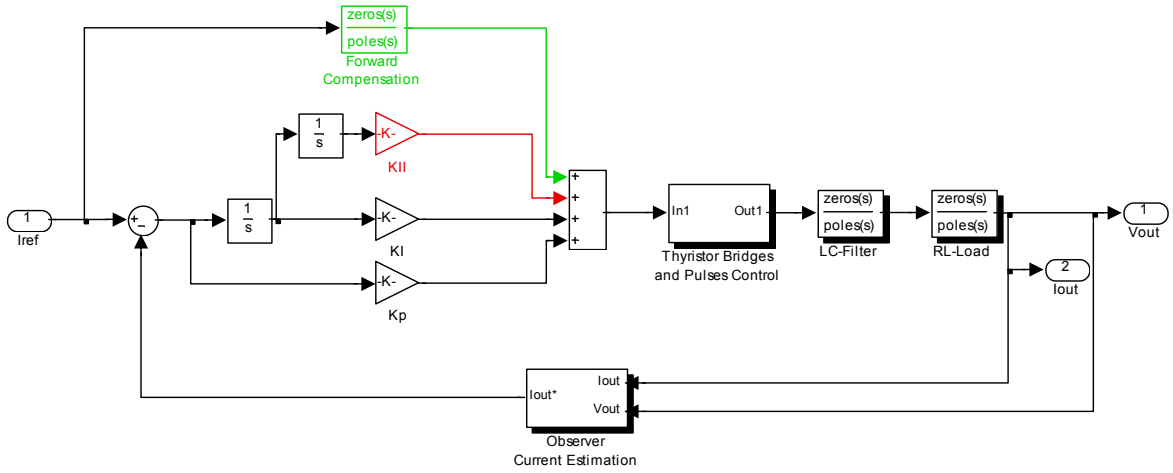

Fig. 14 - Control Scheme adopted in the simulation.

In Fig. 13 the Bode diagrams of the transfer functions of the two controllers are plotted. It can be seen that the cut-off frequency is around 300Hz and slightly more for the FCC. The frequency responses are a few dB peaked which have to be considered during transients to avoid saturation of the power supply. The gains of the feedback have been calculated to suite the maximum error with respect to a fundamental cycle frequency of 0.6 Hz. The error transfer functions $W_e(s)$ are shown in Fig. 15.

The error transfer function can be related to the current error in per-unit of the maximum current by the following equation:

$$\frac{\Delta I}{I_{\max}} = \Delta I_{pu} = \frac{I_{ref}}{I_{\max}} \cdot W_e(s) \qquad (10)$$

Thus the error shown in the text box in Fig. 15, that represents $W_e(s)$, can be interpreted as the maximum error to the 0.5 Hz sinusoid of amplitude I_{max}. It has been chosen to show the 0.5Hz error for historical reasons but the same consideration hold for the fundamental frequency of the actual cycle that is 0.6Hz. It can be seen that for both the controllers this error is around $2*10^{-5}$, thus close to the specifications, but the FCC controller has better performance at higher frequencies thus improving transient response.

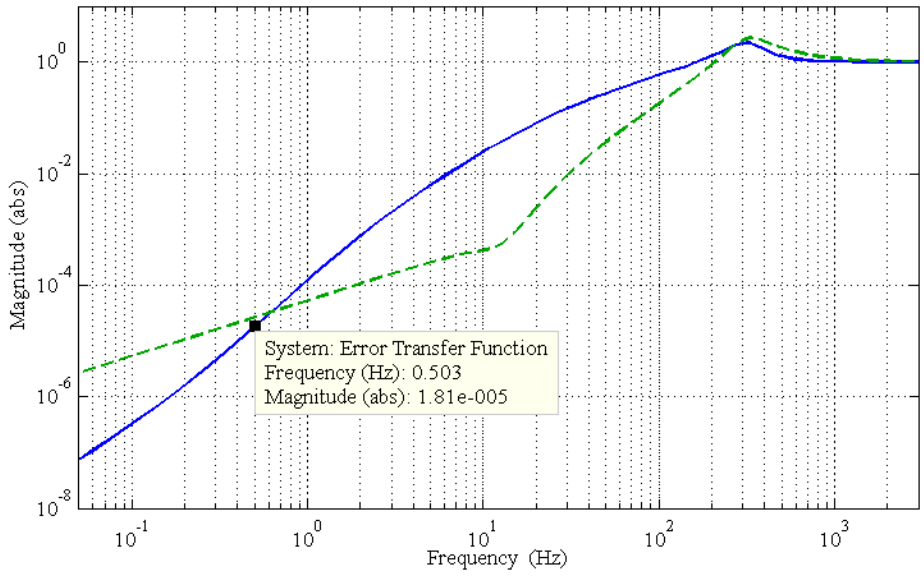

Fig. 15 - Error Transfer Function; Solid Line: with PII – Dashed Line: with FCC.

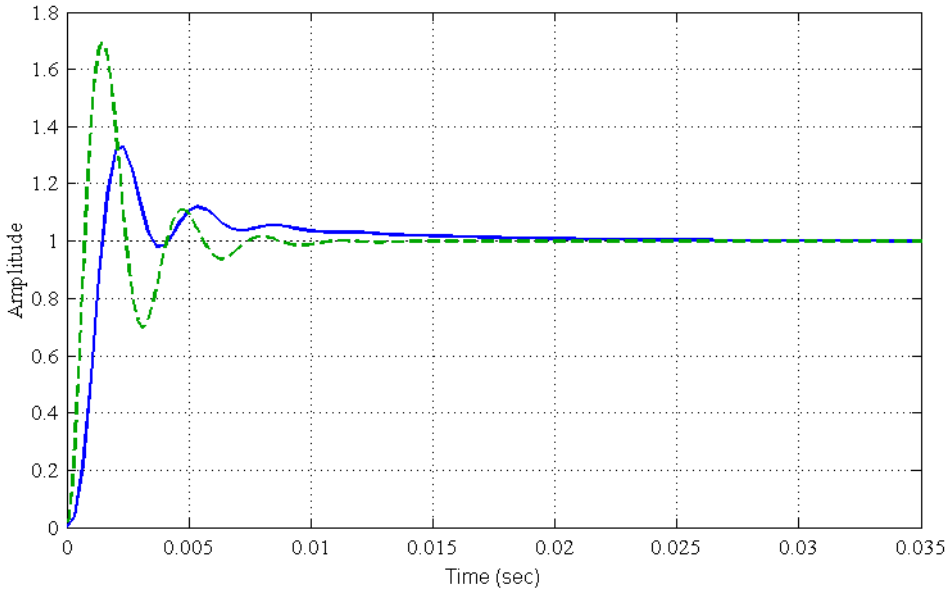

Fig. 16 - Step responses of PII, Solid Line, and FCC, Dashed Line.

The step responses of the PII and FCC controllers are shown in Fig. 16. Even if the FCC controller has a more peaked response, its settling time is less than the PII controller; considering the actual thyristor converter switching frequency this could result in a better performance of the FCC controller the simulations predict. A plot of the system response to the ramp input is shown in Fig. 17. It has been calculated with the maximum ramp rate, 6000A/s, as reference signal. It should be noted that the reference signal never changes from zero to 6000A/s but, as far as it is possible, there are always smooth transitions between one time interval to the following. Thus even if the per-unit error to the ramp of Fig. 17 is two orders of magnitude greater than the specification, it is reasonably assumed that the system will track the reference signal properly. The important information that can be drawn from Fig. 17 is related to the settling time that is much shorter for the FCC controller and is in the range of 10ms thus two orders of magnitude less compared to the cycle period. It is expected that in a few tens of milliseconds a ramp step can be tracked with zero error.

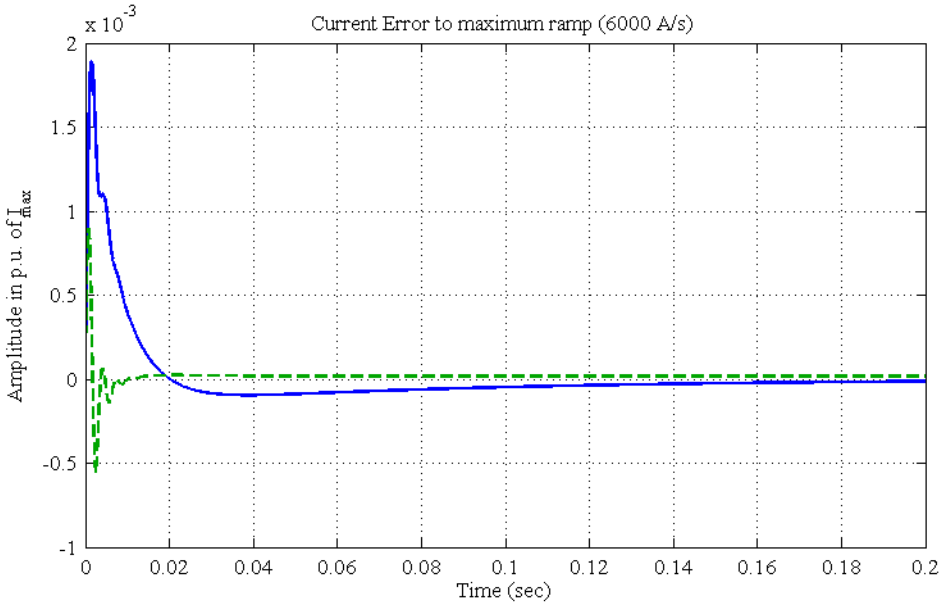

Fig. 17 - Per-unit Error to Maximum Ramp Input. Solid Line: PII, Dashed Line: FCC.

As last issue, the Loop Transfer Function of the system has been plotted in Fig. 18 to analyse open-loop stability. It is shown that the open and closed-loop system are stable. Nevertheless, even if a phase margin of 46 degrees may be sufficient to ensure insensitivity to parameters change, a gain margin of 7dB seems not to be suitable to ensure stability under all working conditions. A possible solution to this problem is to shift the cut-off frequency of the low-pass filter with the drawback of increasing the current ripple and thus the size of the active filter. Other compensation networks may be introduced in the loop to increase stability margins as well.

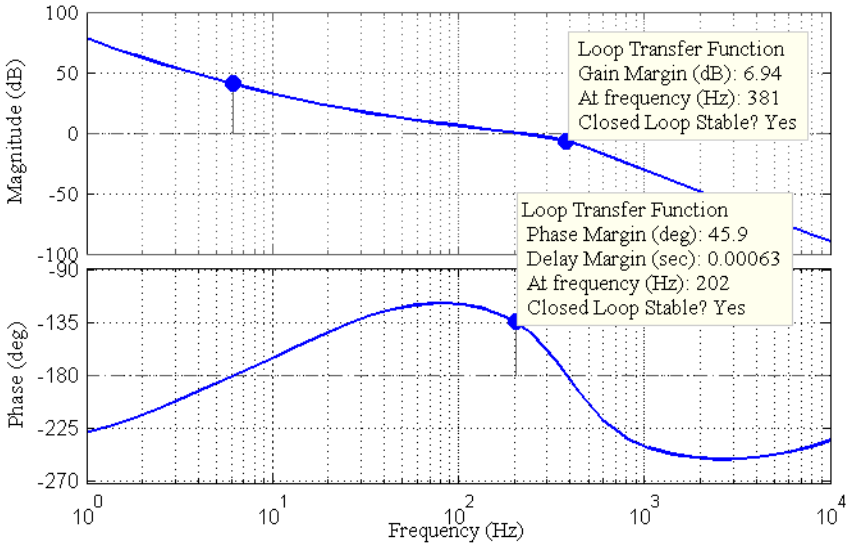

Fig. 18 - Loop Transfer Function of PII controller.

5 A DEEPER INSIGHT ON THE FEEDBACK CONTROL OF THE 24-PULSES THYRISTOR CONVERTER

In this section a complete study on the design of a multi-loop feedback control for the dipoles thyristor rectifier, is developed. The control principle scheme is shown in Fig. 19. It can be seen that three different loops are foreseen to achieve tracking specifications:

- A state filter is used to improve LC-filter characteristics; in particular a smaller damping resistor can be used in the filter, thus achieving a stronger reduction of voltage/current ripple at switching frequencies, while getting a better damping of LC resonance and a higher bandwidth at the same time.
- A voltage loop is used to achieve the thyristors rectifiers behave like an ideal, almost linear, voltage source; this loop also provides a high noise rejection for disturbances coming from mains line voltage fluctuations.
- A current loop provides the needed current reference tracking capability. Proper bandwidth selection, according to specification constraints and adequate phase margins, will be taken into special account in the following analysis.

Details on the specification requirements and typical reference currents are those just seen in the previous description. The design of each sub-loop will be outlined in detail and the behaviour of the whole system will be analysed as well.

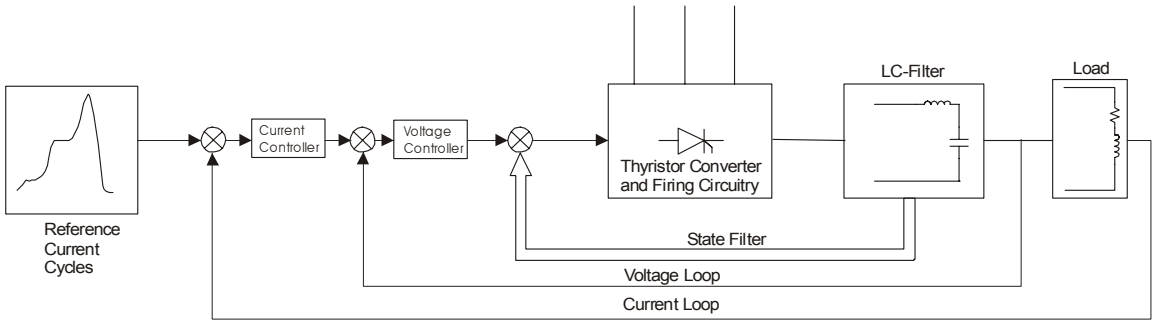

Fig. 19 - Principle scheme of control loops

5.1 State filter design for the low pass passive LC-filter

From the previous analysis, according to harmonic spectrum and taking into account thyristor rectifier bandwidth, it has been pointed out that the cut-off frequency of the LC-filter should be set to about 100Hz. With the state filter it is possible in principle to achieve this cut-off frequency while having the LC-filter tuned on a lower frequency and with a smaller damping resistance, thus reducing substantially the voltage ripple caused by thyristors commutations. To design properly the state filter, it is a good choice to represent the LC-filter with state equations. It should be noted that the low-pass filter can be considered decoupled by the load provided that the impedance of the inductance and the capacitor is much less than the impedance of the load at the frequency of interest. Under this conditions, basing on symbols in Fig. 20, it is possible to write the state equations as follows:

$$\begin{bmatrix} \dot{I}_C \\ \dot{V}_{out} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & -\frac{R_d}{L_f} \end{bmatrix} \cdot \begin{bmatrix} I_C \\ V_{out} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ \frac{R_d}{L_f} \end{bmatrix} \cdot V_{in} \qquad (11)$$

that is a system representation in the usual form d[x(t)]/dt=[A][x(t)]+[B]u(t).

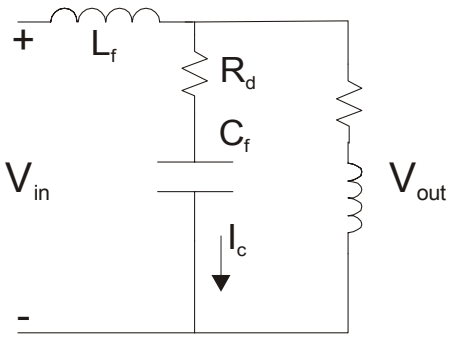

Fig. 20 - Low-Pass Filter scheme

The choice of capacitor current and output (load) voltage as state variables has been done considering that both these variables were easy to measure and that the output voltage is one of the control objectives.

A state filter is based on the assumption that the control is achieved by feeding back the state variables through real constant gains. Thus for the input voltage the control law is chosen to be:

$$V_{in}(t) = -[K] \cdot [x(t)] + r(t) \tag{12}$$

where [K] is the 1 x n matrix of feedback gains and [x(t)] is the n x 1 state vector. Thus, in the hypothesis of a completely controllable system, a matrix [K] exists that can give an arbitrary set of eigenvalues of ([A]-[B][K]). So we can get the matrix:

$$s[I] - [A] + [B][K] = \begin{bmatrix} s + \frac{k_1}{L_f} & \frac{1+k_2}{L_f} \\ -\frac{1}{C_f} + k_1 \frac{R_d}{L_f} & s + (1+k_2)\frac{R_d}{L_f} \end{bmatrix} \tag{13}$$

The determinant of this matrix gives the characteristics equation of the system:

$$s^2 + \left[(1+k_2)\frac{R_d}{L_f} + \frac{k_1}{L_f} \right] \omega s + \frac{1+k_2}{L_f C_f} = 0 \tag{14}$$

A graphical representation of the filter with the feedback constant gains is shown in Fig. 21 with the use of state diagram.

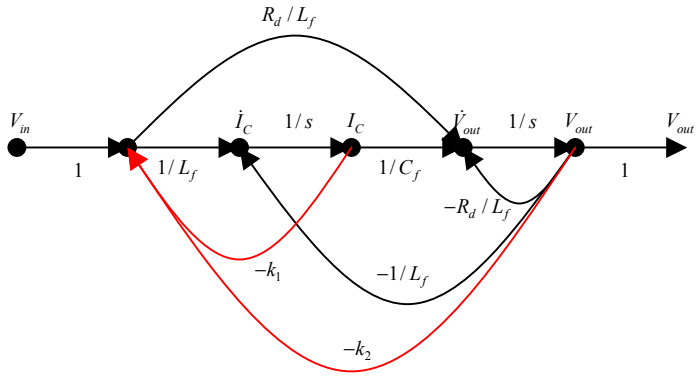

Fig. 21 - State diagram of LC-filter with constant gains feedback

From Eq.(14) it is clear that by varying k_2 the natural frequency of the filter can be increased, and that with the parameter k_1 the damping can be improved. As a matter of fact for the second order system the following equations can be written:

$$\begin{aligned} \omega^2 &= \frac{1+k_2}{L_f C_f} \\ 2\omega\omega &= (1+k_2)\frac{R_d}{L_f} + \frac{k_1}{L_f} \end{aligned} \tag{15}$$

with ω=natural frequency, ω=damping factor. For completeness the transfer function of V_{out}/V_{in} and of the error 1- V_{out}/V_{in} are reported here:

$$\frac{V_{out}}{V_{in}} = \frac{1}{L_f C_f} \frac{1 + R_d C_f \omega s}{s^2 + \left[(1+k_2)\frac{R_d}{L_f} + \frac{k_1}{L_f} \right] \omega s + \frac{1+k_2}{L_f C_f}}$$

$$\omega = 1 - \frac{V_{out}}{V_{in}} = \frac{s^2 + \left[k_2 \frac{R_d}{L_f} + \frac{k_1}{L_f} \right] \omega s + \frac{k_2}{L_f C_f}}{s^2 + \left[(1+k_2)\frac{R_d}{L_f} + \frac{k_1}{L_f} \right] \omega s + \frac{1+k_2}{L_f C_f}} \qquad (16)$$

It is interesting to observe the behaviour of a low-pass filter designed with and without the help of a state filter. We have chosen, according to the present application, an LC-filter with a natural frequency of 100Hz and a damping factor equal to 1. It is then redesigned with a lower cut-off frequency equal to 80Hz and a damping factor of 0.5, thus providing a higher attenuation to ripple frequencies. The state filter constants are calculated to achieve 100Hz and damping of 1. The results are shown in Fig. 22 and Fig. 23 for the time domain and frequency domain respectively. The feedback values for the state filter constants are k1=0.75, k2=0.56.

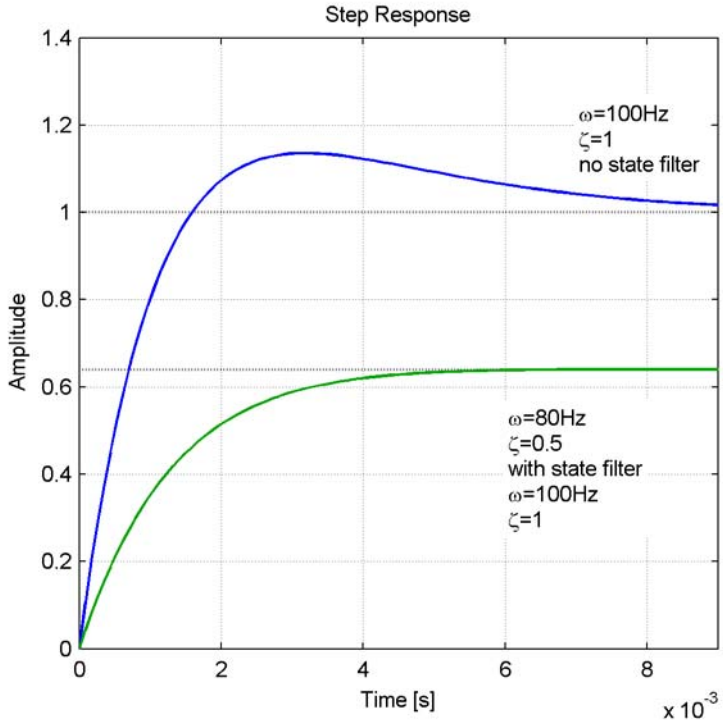

Fig. 22 - Step responses of the low-pass filter with and without state filter

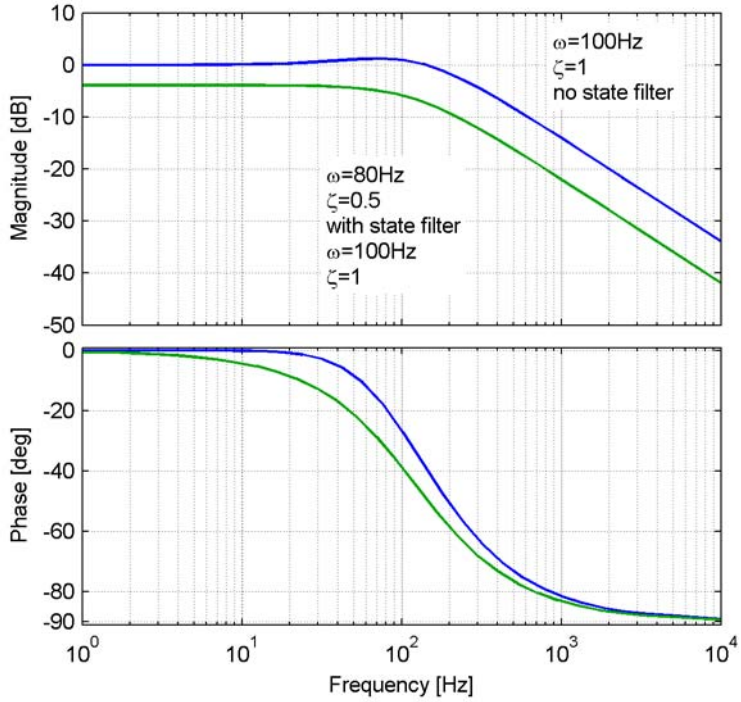

Fig. 23 - Bode diagram of the low-pass filter with and without state filter

The first interesting thing is that the filter designed with the state filter has a different steady state value and it is evident from Eq.(16) with which we get for the steady state at a step input:

$$\left.\frac{V_{out}}{V_{in}}\right|_{s\to 0} = \frac{1}{1+k_2} \tag{17}$$

Thus to get zero steady state error an integral action shall be used thus providing also a voltage loop action useful to increase network fluctuations rejection and improving converter linearity. The details of this controller will be analysed later.

The phase characteristic is also interesting. In particular it should be taken into account in the design of the voltage and current loops to achieve the appropriate phase margin. Under this point of view it should be noted that the LC-filter with state filter compensation has a phase lower than the equivalent LC-filter.

The previous considerations have shown that making use of the state filter it is possible to design a filter with a lower cut-off frequency and a lower damping resistance. It is a good choice however to select a frequency and a damping ratio not so far from the ones that must be achieved with the state filter feedback. The lower the cut-off frequency the higher is the volume, and thus the cost, of the filter.

5.2 Voltage loop design

The design of the voltage-loop controller is now developed. On the basis of the previous analysis we want to calculate the parameters of a proportional-integral (PI) controller to

eliminate steady state errors and to provide system linear behaviour and improve low-frequency noise rejection. It has been said above that the system thyristor rectifier + low-pass filter, shall have an equivalent cut-off frequency around 100Hz. The PI voltage controller can be designed by the following simple procedure [3]:

1) Determine the DC gain K_{VDC} such that the system is stable and the gain at the frequencies of interest is high enough. In Fig. 24 are shown the loop transfer functions of the LC-filter plus state-feedback with and without DC gain. It has been estimated sufficient to have a K_{VDC}=15.
2) Determine the proportional gain K_{VP} of the PI controller such that the gain at the frequency of interest is 0dB. So from Fig. 24 we can measure 14.2dB at 200Hz. It has been chosen the frequency of 200Hz a little higher than the target frequency of 100Hz to have margins for calculate correctly the integral gain without phase margin degradation. The proportional gain yields:

$$K_{VP} = 10^{-\frac{14.2}{20}} = 0.19 \tag{18}$$

3) The integral gain of the PI controller can be calculated in a proper way by the following equation:

$$\frac{K_{VI}}{K_{VP}} = \frac{\infty}{10} \tag{19}$$

where ∞ is the cut-off frequency previously obtained. In general this gives a stable system with sufficient phase margin. Nevertheless, in the case in object, it can be seen from Fig. 24 that the system has a phase always greater than 90 degrees. Thus, in principle, the ratio K_{VI}/K_{VP} can be taken greater without degradation of stability and improving transient response. We can thus calculate the integral gain as:

$$K_{VI} = \frac{\infty}{2} \cdot K_{VP} = \frac{2 \cdot \pi \cdot 200}{2} \cdot 0.19 = 120 \tag{20}$$

The controller block diagrams so far calculated is outlined in Fig. 25 and its Loop and Closed Loop responses are shown in Fig. 26. It can be seen that at 100Hz there is about 1dB attenuation and that the bandwidth (-3dB) is 200Hz. The phase margin is always grater than 90 degrees. In Fig. 27, the step response is shown. No overshoot is present. Rise time and settling time are respectively 1.8ms and 4.5ms that seem to be adequate and will be tested in following simulations.

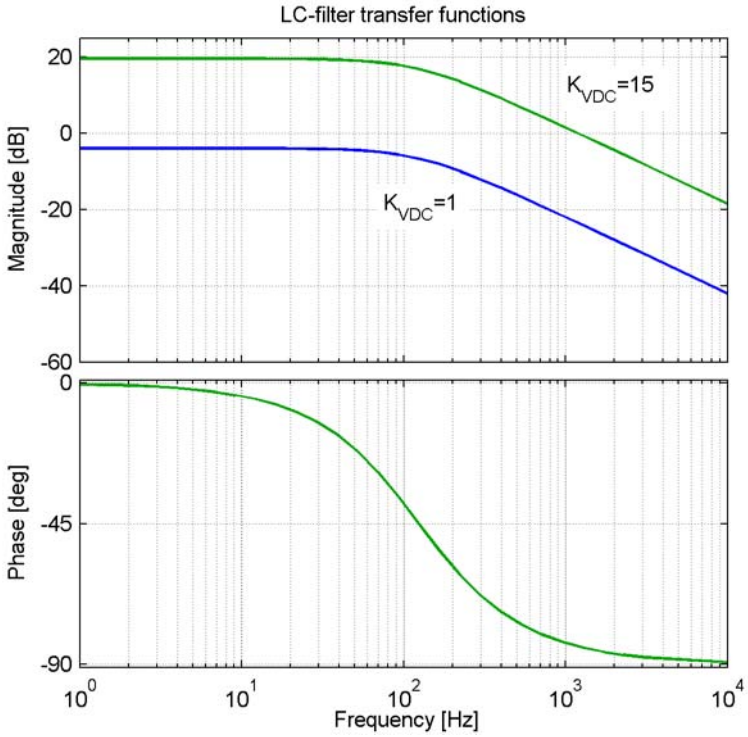

Fig. 24 - LC-filter transfer functions with and without DC gain

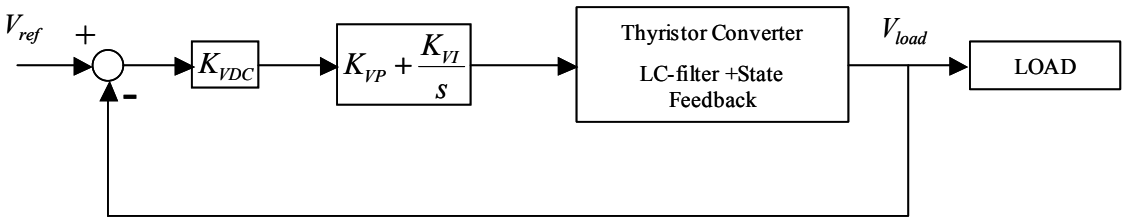

Fig. 25 - Voltage Loop Controller Block Diagram

From the block diagram of Fig. 25 and rearranging Eq.(16) we get the expression of the voltage error:

$$e_V = \frac{1}{1 + K_{VDC}\left(K_{VP} + \frac{K_{VI}}{s}\right)\frac{\omega_f^2 + \left(R_d/L_f\right)s}{s^2 + 2\zeta\omega_n s + \omega_n^2}} \qquad (21)$$

where ω_f is the natural frequency of the LC-filter and ω_n is the natural frequency of the system with state feedback. It is of particular interest to evaluate the error to the ramp input to better understand transient response of the system.

$$\lim_{s\to 0} s\frac{1}{s^2}e_V = \frac{1}{K_{VDC}K_{VI}\frac{\omega_f^2}{\omega_n^2}} = 8.6\times 10^{-4} \qquad (22)$$

It is interesting to note that this error is inversely proportional to the product of the DC gain and integral gain. This consideration may be useful to adjust the gains of the voltage feedback to better suite the transient response specifications. Also the natural LC-filter

frequency is important: if it is chosen too low, although the presence of state feedback, it may increase the ramp error thus degrading transient performance.

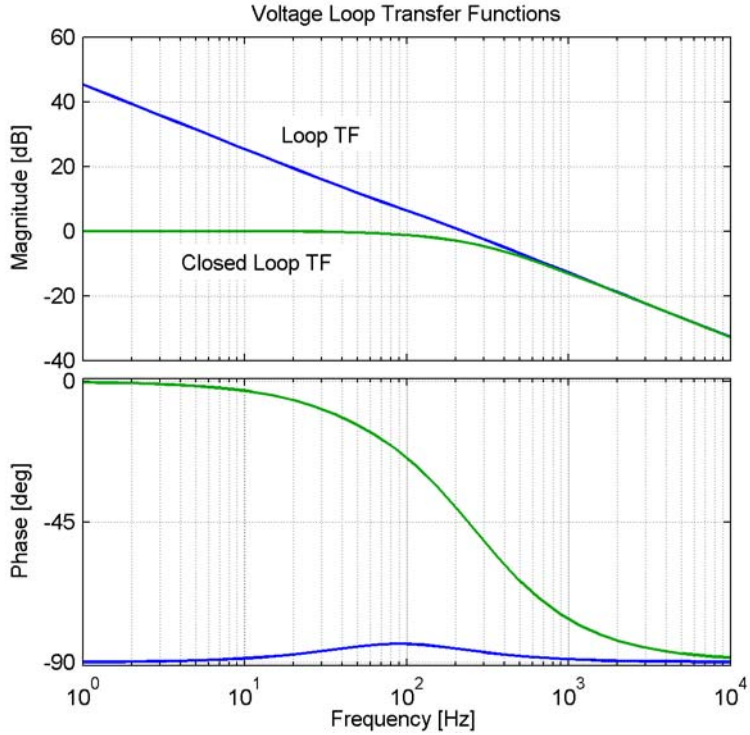

Fig. 26 - Loop and Closed Loop responses of Voltage Controller

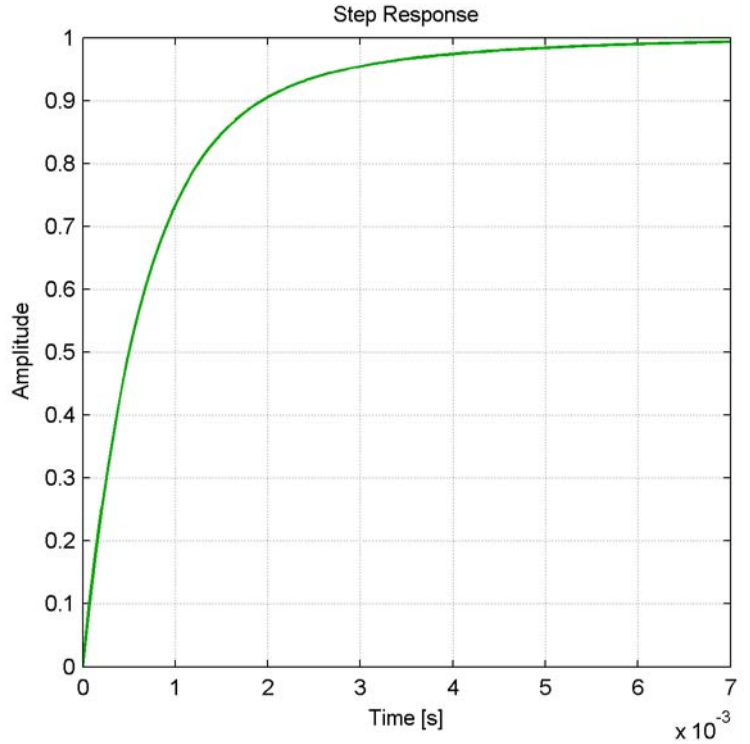

Fig. 27 - Voltage Loop Step Response

In Fig. 28 the disturbance rejection characteristic is shown comparing the case without the voltage loop (only LC-filter and state filter), with the one including the voltage loop so far designed. As expected the voltage loop provides a strong attenuation of all disturbances at frequencies below its cut-off frequency.

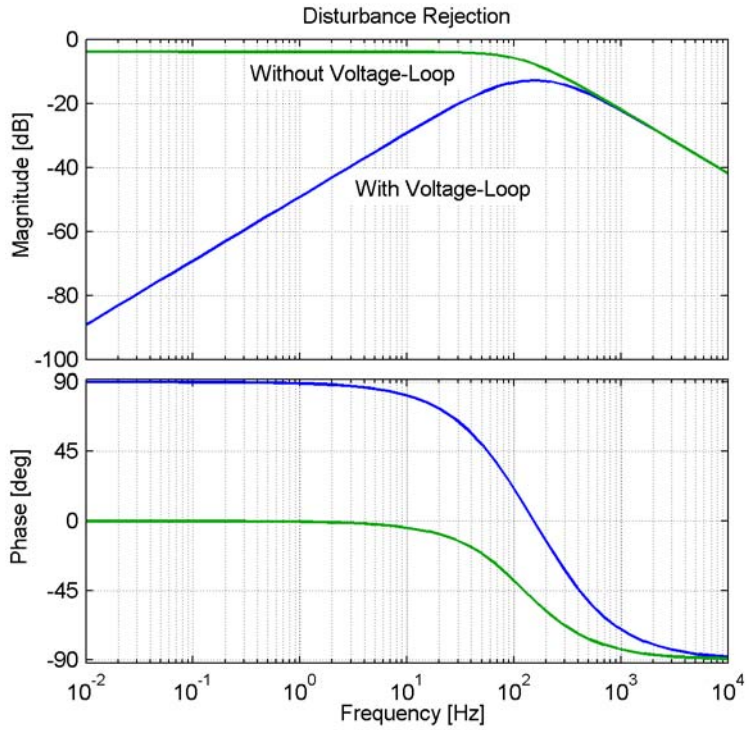

Fig. 28 - Disturbance Rejection with and without voltage loop

In Fig. 29 it is shown an analogical realization of the PI controller with the use of Operational Amplifiers. The resistors and capacitors values can be calculated as follows:

$$K_{VP} = \frac{R_2}{R_1} = 0.19$$

$$\Rightarrow \quad \left.\begin{aligned} R_1 &= 100k \\ C_2 &= 83nF \\ R_2 &= 19k \end{aligned}\right| \qquad (23)$$

$$K_{VI} = \frac{1}{R_1 C_2} = 120$$

These calculations clearly show that there are no critical values for the electrical components to be used for the actual implementation of the voltage loop controller.

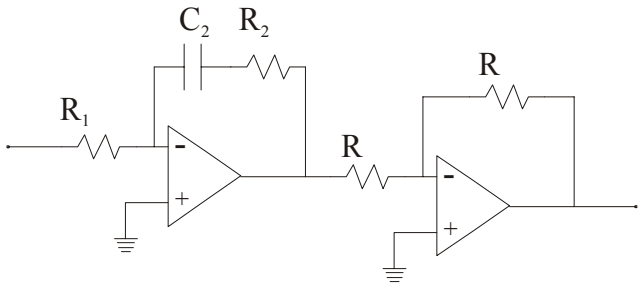

Fig. 29 - Op-Amp realization of PI Voltage Controller

5.3 Current loop design

The outer current loop controller is basically a PI controller with which we attempt to fulfil the error specifications. The design procedure is quite similar to the one for the PI controller for the voltage loop. It should be now considered that as a consequence of the previous analysis the rectifier and the filter behaves like shown by the closed loop response in Fig. 26. This is the (output voltage)/(input voltage) Bode diagram. To obtain the load current the load impedance (admittance) must be considered. The load characteristics can be summarized as follows:

$$L_{load} = 11.7\,mH \infty 17\,dipoles = 198.9\,mH$$
$$R_{load} = 5.12\,m\Omega \infty 17\,dipoles = 87\,m\Omega$$
$$R_{cables} = 3.11\,m\Omega$$

These data are known with some uncertainty margins and this could affect substantially the effectiveness of the current control as will be more clear later.

The DC-gain has been calculated such to bring the output/input current transfer function cut-off frequency at 100Hz as shown in Fig. 30.

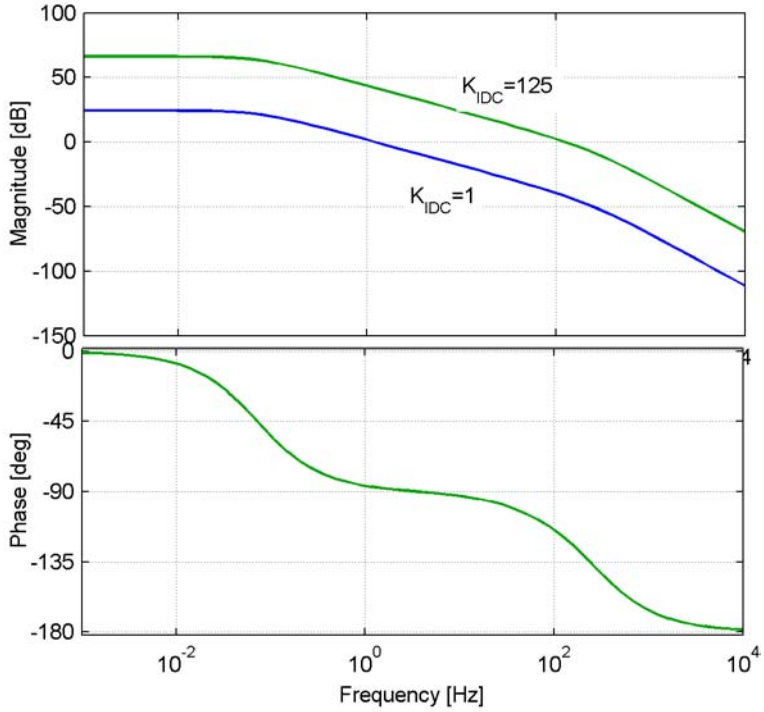

Fig. 30 - Output/Input current transfer functions

The gain of the current transfer function at 100Hz is –42dB and thus the DC-gain can be calculated by:

$$K_{IDC} = 10^{\frac{42}{20}} = 125$$

Basing on Fig. 30, a phase-margin of 80 degrees is found at a frequency of 40Hz and it is estimated to be sufficient to give a suitably damped response. The frequency of 40Hz has been chosen both for stability margins requirements and taking into account other

compensation networks that will be analysed in a following paragraph. The proportional gain of the PI controller can be calculated as:

$$K_{IP} = 10^{-\frac{G(40Hz)}{20}} = 10^{-\frac{7.5}{20}} = 0.42 \quad (24)$$

The integral gain can be calculated as follows to preserve the phase margin:

$$K_{II} = \frac{\infty}{10} \cdot K_{IP} = \frac{2 \neq 40}{10} \cdot 0.42 = 10.5 \quad (25)$$

The loop transfer function of the current controller with the parameters just above calculated is shown in Fig. 31 along with the closed loop transfer function.

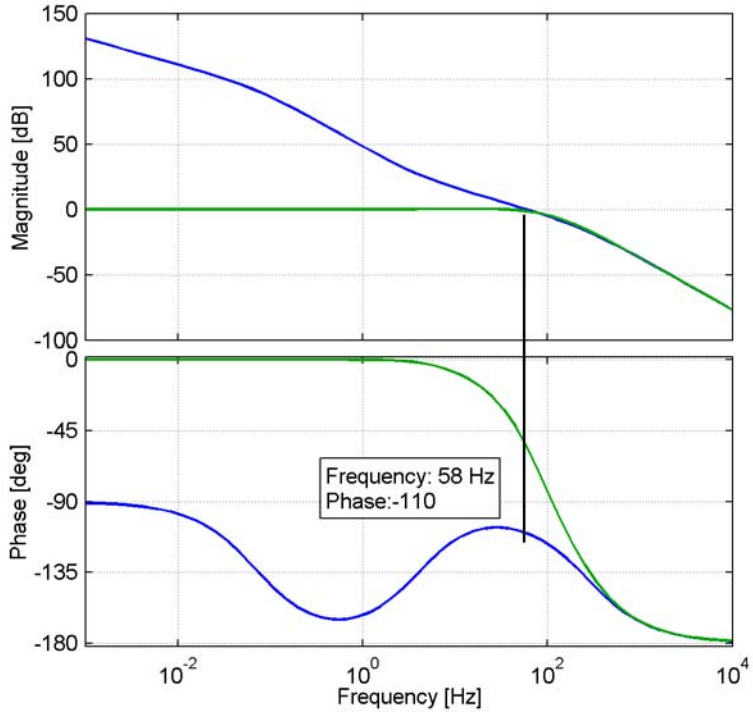

Fig. 31 - Loop transfer function (Blue) and Closed loop transfer function (Green) of PI current control

As can be seen the Loop transfer function has a cut-off frequency of 58Hz and a phase-margin of 70 degrees.

Once the stability of the system has been verified within some margins, the most important parameters to look at are the error as a function of frequency and the error step response. They are both shown in Fig. 32. The error shown can be thought as the peak-to-peak error in per-unit of maximum current. Thus, for our purposes, it is important to evaluate the error at a sinusoidal input of frequency 1Hz. The specifications ask for 10^{-5} peak-to-peak error in per-unit of maximum current. It is quite evident that more than two order of magnitudes are still missing to reach for specification requirements. It is not convenient, at this stage, to increase gains because the system would have a more peaked oscillatory response and eventually becomes unstable. The rise time is less than 4ms but the response exhibits a small overshoot of 6.5% and a relatively large settling time of 50ms.

It is now of interest to explore the effect of adding some additional blocks to the basic PI controller to reduce the error at 1Hz and improve transient response. In particular a lead-lag and a feed-forward blocks will be introduced and analysed. The block diagram can be seen in Fig. 33.

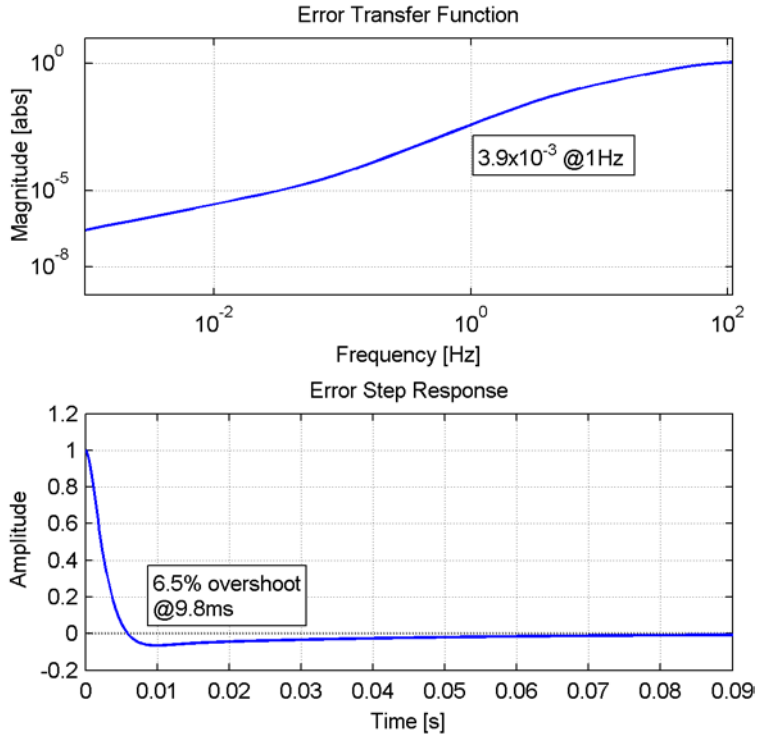

Fig. 32 - Error transfer function ad Error step response of the system with current controller

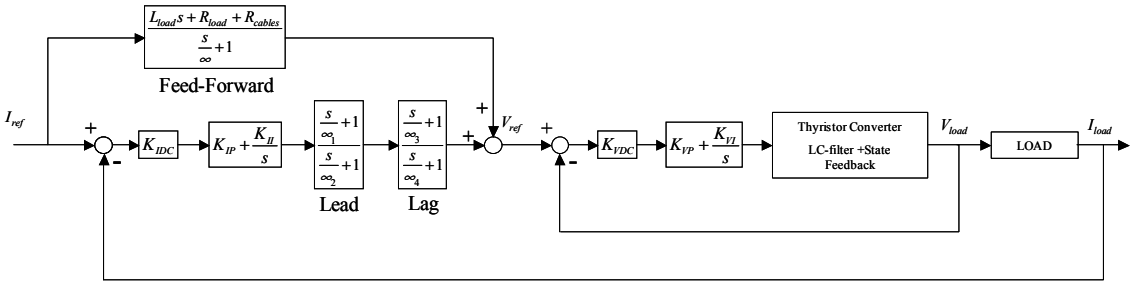

Fig. 33 - Block Diagram of PI controller with Phase-lead and Feed-Forward additional blocks

As can be seen in Fig. 31 if we want to increase the gain around the 1Hz frequency without increasing the cut-off frequency we could use a lead-lag controller with the parameters calculated to set the maximum gain at 1Hz. The calculations are shown in the following and the Bode plot is reported in Fig. 34.

$$Lead: \frac{\frac{1}{2\pi f_1}s+1}{\frac{1}{2\pi f_2}s+1} \qquad Lag: \frac{\frac{1}{2\pi f_3}s+1}{\frac{1}{2\pi f_4}s+1} \tag{26}$$

To set the maximum gain at 1Hz it is sufficient that holds $f_2=f_4=1Hz$; by adjusting $f_1=1/f_3$ the gain at 1Hz can be regulated. In Fig. 34 the Bode plot for two different values of f_1 is shown. It is clear that the values of f_1 and f_3 affect also the phase of the system that, although increased at lower frequencies, decreases at higher and may degrade the stability of the system. For our purposes the following values for the frequencies of the lead-lag controller have been chosen:

$$f_2 = f_4 = 1Hz$$
$$f_1 = 1/f_3 = 0.1Hz$$

It is important to point out that the lead-lag controller has been used here more like a so called "notch filter", because more emphasis has been put on adjusting the gain properly than on setting the phase at a specified level.

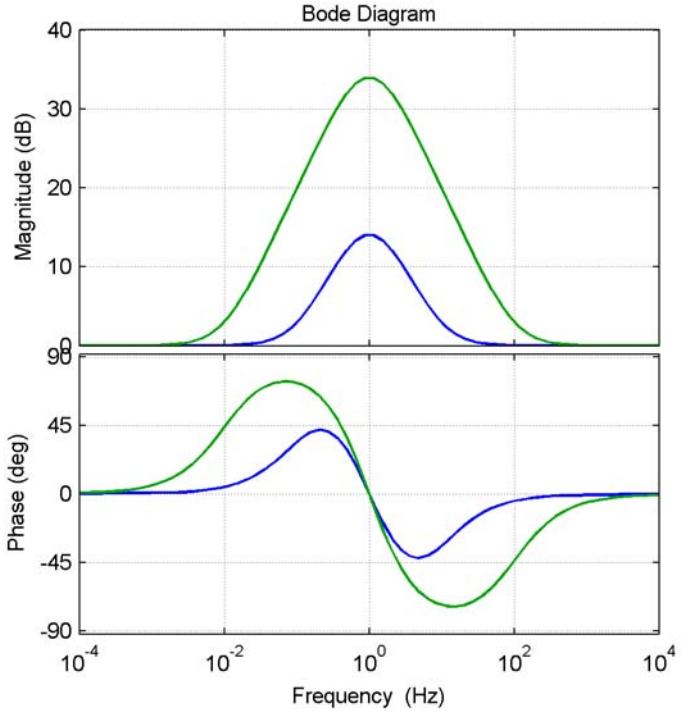

Fig. 34 - Lead-Lag controller Bode plot. Blue line: $f_1=0.1Hz$; Green line:$f_1=0.01Hz$

The frequency response of the system is shown in Fig. 35 where the magnitude and phase curves of the error with and without the lead-lag controller are compared. It is quite evident that with the lead-lag controller a factor 5 has been achieved in reducing the error at 1Hz. A further increase in gains from 0.1 to 10 Hz has been also achieved thus improving system performance.

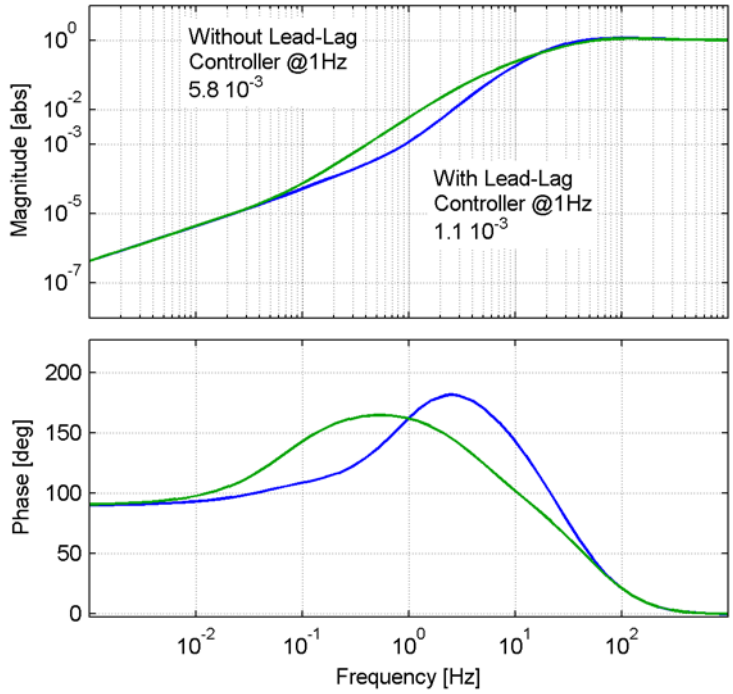

Fig. 35 - Error Frequency response of the system

The Error Step and Ramp Responses have been also calculated and shown in Fig. 36 and Fig. 37. The step response reveals that the system with the lead-lag controller is quite faster than the other but it also shows a more peaked behaviour. It is important so to avoid large step changes in the current reference signal to not running into possible overshoots that may degrade transient response or even get the system unstable by saturating the power amplifier.

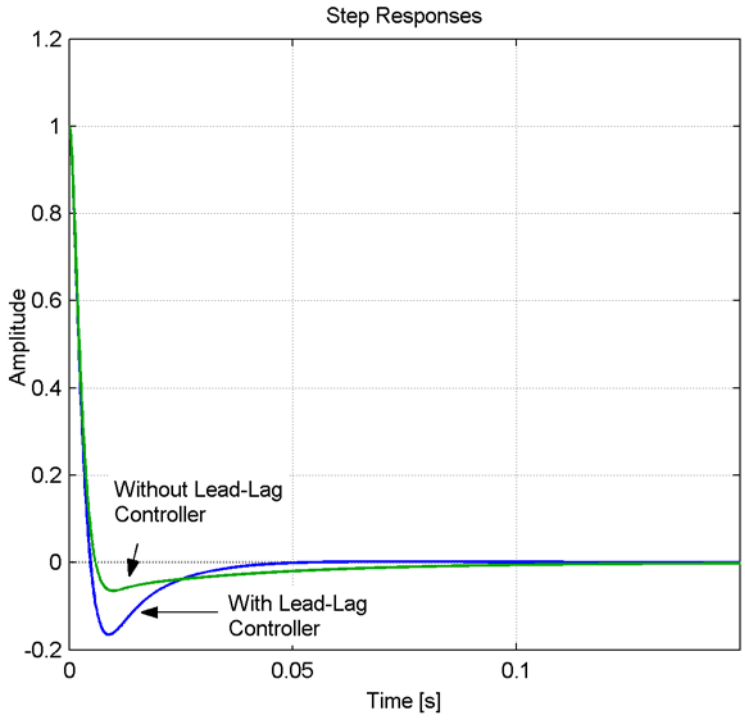

Fig. 36 - Error Step Responses with and without Lead-Lag controller

The Ramp response is very important for our purposes because it shows how big is the transient error to a ramp input. Although the reference signal has always smoothed ramps – no discontinuities on the first derivative of current reference signal – the ramp response can help the designer in estimating the transient error that occurs at the beginning of a ramp.

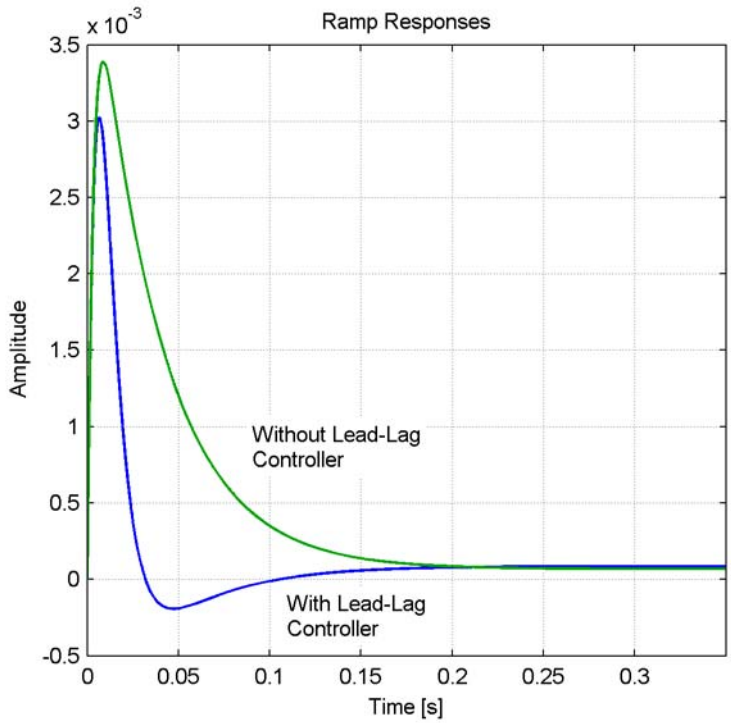

Fig. 37 - Error Ramp responses with and without Lead-Lag controller

For example, as will be shown later, a current reference that is requested in the specification is a cosine function with some restrictions on maximum frequency and maximum derivative. In Fig. 38 and Fig. 39 are shown the current error together with a 0.7Hz cosine reference. It can be clearly seen that, although the first derivative of the current reference is zero at the beginning of the cosine function, there is an overshoot in the error. As shown in Fig. 37, the error ramp response is characterised by a peak that extends over a time span of about 30ms. It is thus reasonable to think that an average ramp reference is seen by the system during this period of time as shown in Fig. 38. The peak current can be calculated as follows:

$$\text{Average ramp over 30ms} = \frac{10\,A}{30\,ms} = 333\,A/s$$
$$\text{peak current reached} = (333\,A/s) \cdot (\text{error ramp peak}) = 333 \cdot 3 \cdot 10^{-3} = 1\,A \qquad (27)$$

The calculation method shown in Eq.(27) is not rigorous but helps in giving both an estimate and a physical interpretation of transient errors occurring at initial instants of ramping periods.

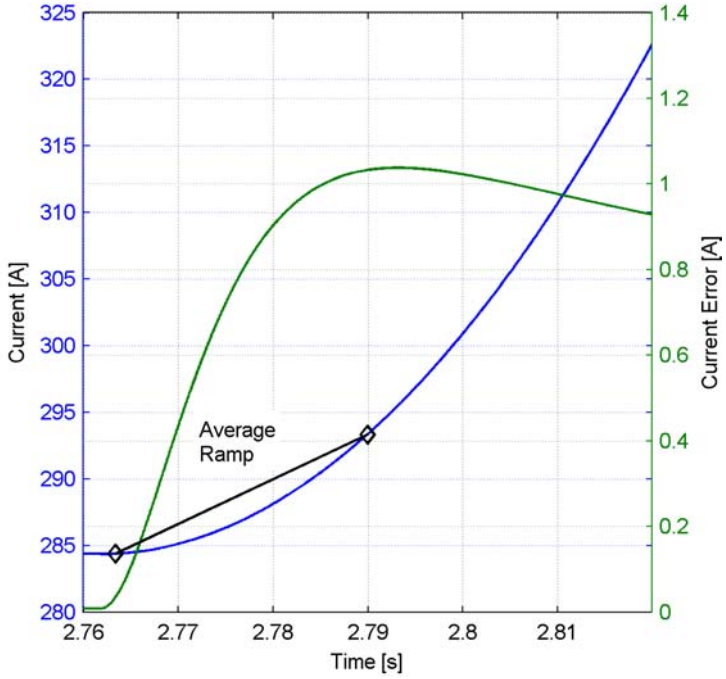

Fig. 38 - Initial overshoot of current error (green) due to average ramp of current reference(blue)

In Fig. 39 is shown the plot of the current error on the whole cosine ramp. The start and end peaks and also the steady state cosine error shape are clearly visible. The steady state error is easy to calculate by the use of frequency response plotted in Fig. 35.

$$E_{\substack{\text{steady-state}\\ \text{peak-to-peak}}} = E(@0.7Hz) \cdot I_{\text{peak-to-peak}} = 6.2 \cdot 10^{-4} \cdot (3000 - 284) = 1.68\,A \qquad (28)$$

Result that is in strong agreement with the error shown in Fig. 39.

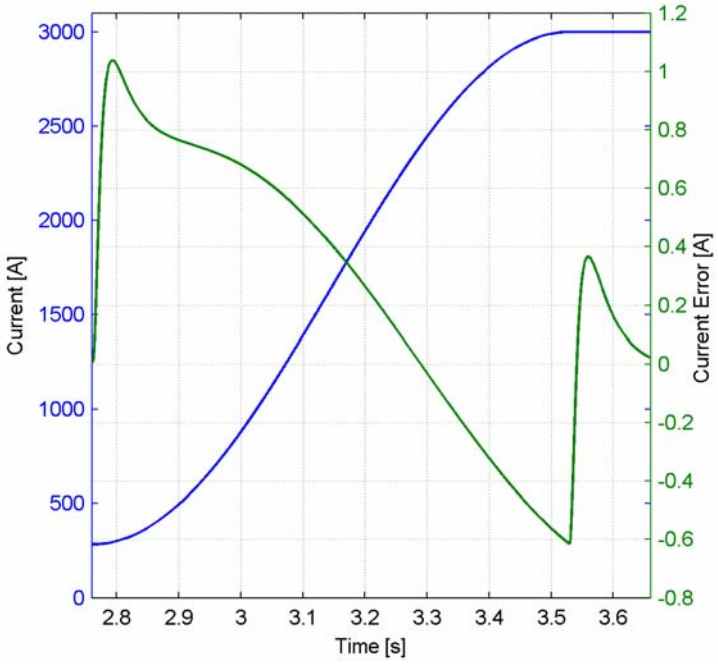

Fig. 39 – Error shape for a 0.7 Hz cosine current reference.

The use of the Feed-Forward controller is based on the purely theoretical assumption of knowing exactly the load parameters (resistance and inductance) and neglecting, for the frequencies of interest, the effect of the low-pass filter and the non-linearity of the thyristor rectifier. As can be understood by the block diagram in Fig. 33, feed-forward action should feed the right voltage driving signal in response to the reference signal; this way, if the system were ideal, the feedback network would be useless. The feedback controllers have only the purpose of correcting for errors and system actual behaviour.

The simplest feed-forward controller, that suites present system requirements and characteristics, is a high-pass filter with load resistance and inductance as parameters. The transfer function is:

$$FF = \frac{L_{load} \cdot s + R_{load} + R_{cables}}{\frac{s}{\omega_{hi}} + 1} = \frac{0.198 \cdot s + 0.09}{\frac{s}{2 \cdot \pi \cdot 1000} + 1} \qquad (29)$$

The denominator has been added for the actual realization of the controller. A corner frequency of 1000Hz has been estimated sufficient both for correct feed-forward and for noise prevention. Higher frequencies can be nevertheless taken into account according to physical feasibility of the controller and overall system behaviour.

The error frequency plot, step and ramp responses are shown in figures from Fig. 40 to Fig. 42, comparing the three kind of controllers. It can be noted that the feed-forward controller improves substantially the error frequency response of the system. We get at 1Hz and error of $7.5 \cdot 10^{-6}$ that is 22.5mA peak-to-peak for 3000A maximum current. The specifications asked for 30mA peak-to-peak and thus they are fulfilled. Nevertheless it is important to point out that the feed-forward controller design is based on the knowledge of load parameters, it is also very sensitive to load parameters changes. The sensitivity of the system to load changes will be analysed later in the note.

From step response, it can be seen that feed-forward controller has reduced the rising time and improved the damping. In particular from the ramp response, the peak error has been reduced of a factor 5 and also the response time has been reduced thus making the average ramp seen by the system lower. Following the same procedure previously outlined, the peak transient error for a cosine current ramp can be calculated as follows:

$$\text{System response time} = 8\,ms$$

$$\text{Average ramp (8ms)} = \frac{0.75\,A}{8\,ms} = 93.75\,\frac{A}{s} \qquad (30)$$

$$\text{Peak transient error} = \text{Avg}_{\text{ramp}} \cdot \text{Peak}_{\text{err.ramp.rsp.}} = 93.75 \cdot 6.8 \cdot 10^{-4} = 63\,mA$$

Simulation, not shown here for brevity, have shown a peak transient error of 63mA. Although specifications claim for 30mA maximum error it seems physically reasonable to accept a factor 2 greater error at the beginning of the ramp if the Radio Frequency follows this deviation. It is nevertheless important that this error decays as fast as possible (few milliseconds).

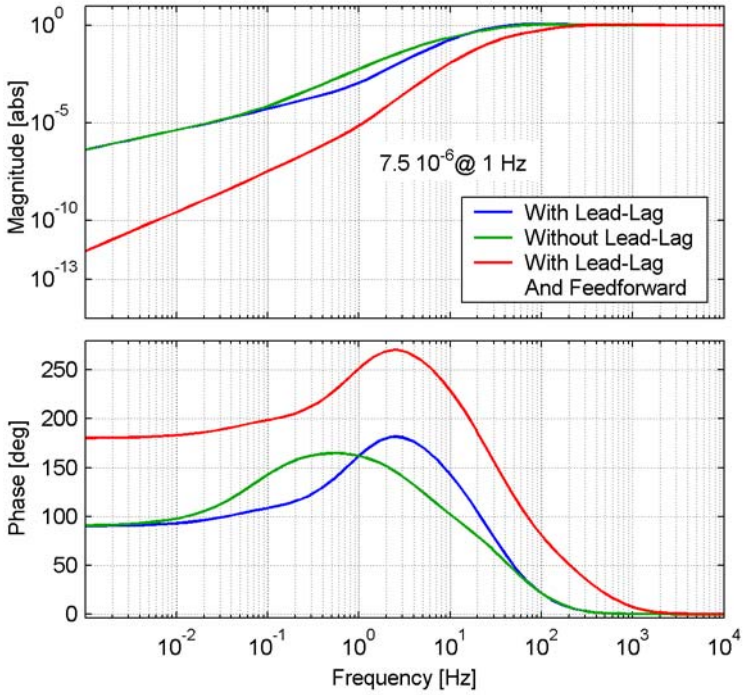

Fig. 40 – Error Frequency plot

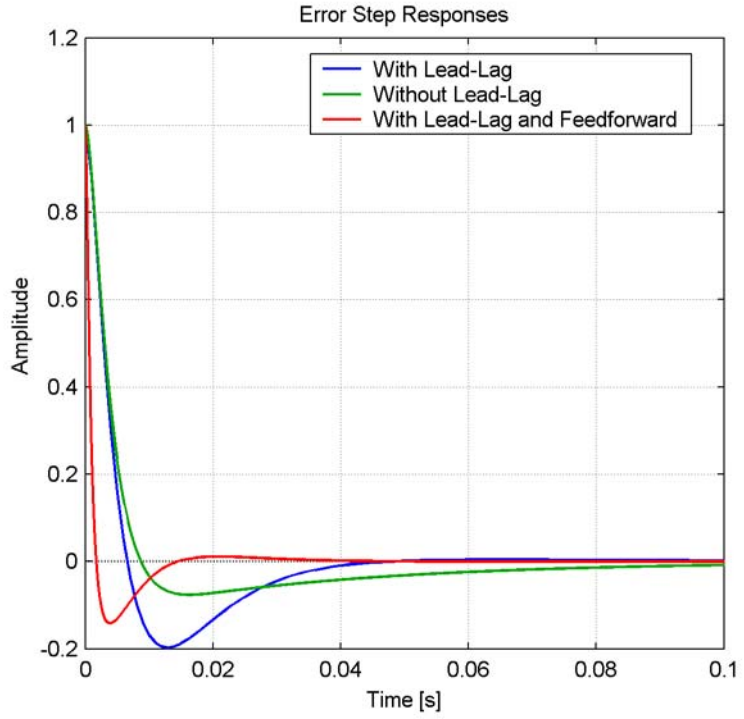

Fig. 41 – Error Step Response

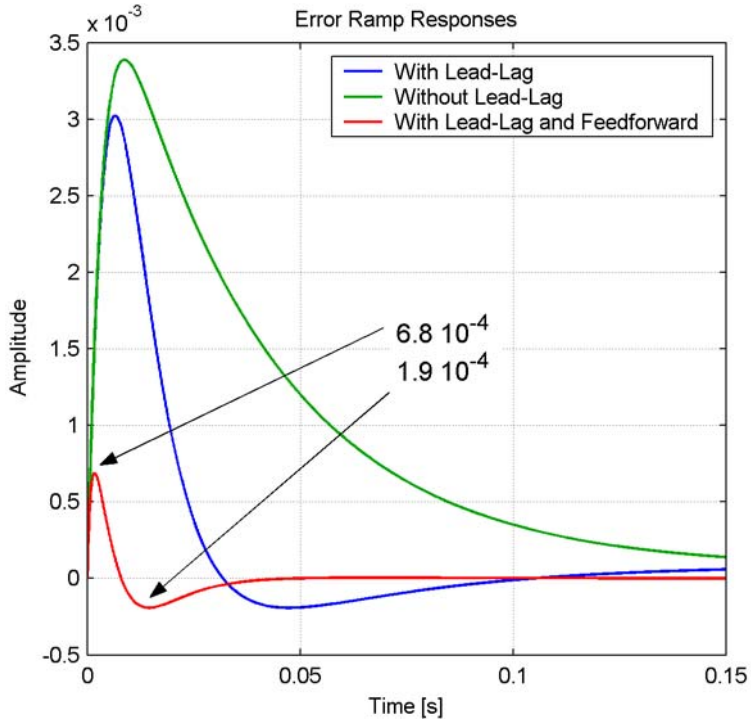

Fig. 42 – Error Ramp Response

As done previously we can analyse the controllers so far outlined in term of their analogical realization with operational amplifiers to investigate their actual implementation. The electrical scheme for the current PI controller is identical to the voltage loop one, and can be found in Fig. 29. The calculated resistors and capacitor are:

$$K_{IP} = \frac{R_2}{R_1} = 0.42$$

$$\Rightarrow \quad \begin{aligned} R_1 &= 100k\,| \\ C_2 &= 95nF \\ R_2 &= 42k\,| \end{aligned} \qquad (31)$$

$$K_{II} = \frac{1}{R_1 C_2} = 10.5$$

This controller does not seem to show any problem for practical implementation.

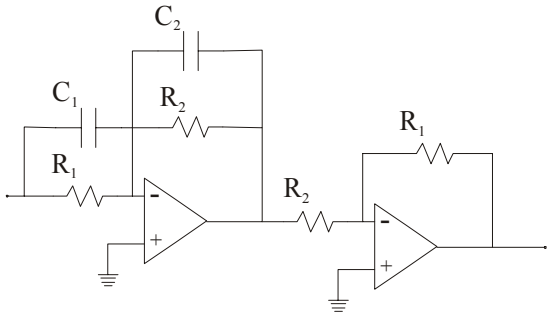

Fig. 43 – Lead, Lag, and Feed-Forward controllers operational amplifiers realization

A suitable scheme for the lead or lag and even for the feed-forward controller can be seen in Fig. 43. To get a lead-lag controller two stages must be connected in series. The calculations for the resistors and capacitors are as follows:

Phase-Lead:

$$\frac{1+aT\propto s}{1+T\propto s}=\frac{1+R_1C\propto s}{1+R_2C\propto s} \qquad R_2=50k\,|$$

$$aT=\frac{1}{2\neq f_1}=1.6 \quad \Rightarrow \quad C_1=C_2=C=3.2\propto F$$

$$T=\frac{1}{2\neq f_2}=0.16 \qquad R_1=500k\,|$$

Phase-Lag:

$$\frac{1+aT\propto s}{1+T\propto s}=\frac{1+R_1C\propto s}{1+R_2C\propto s} \qquad R_2=200k\,|$$

$$aT=\frac{1}{2\neq f_3}=0.016 \quad \Rightarrow \quad C_1=C_2=C=800nF$$

$$T=\frac{1}{2\neq f_4}=0.16 \qquad R_1=20k\,|$$

(32)

For the lead-lag controller a relatively large capacitor is needed. Also the resistors have high values. Precision and linearity of these elements may become important issues. Nevertheless, the realization of these controllers seems to be relatively easy.

The same scheme of Fig. 43 can be used for the feed-forward controller by keeping the two capacitors different. The calculations are:

Feed-Forward Controller:

$$\frac{C_1}{C_2}\frac{s+\frac{1}{R_1C_1}}{s+\frac{1}{R_2C_2}}=\frac{L_{load}s+R_{load}+Rcables}{\frac{1}{2\neq 1000}s+1}=1237\frac{s+0.45}{s+6250} \qquad R_1=555k\,| \quad R_2=49k\,|$$

$$\frac{1}{R_1C_1}=0.45 \qquad \Rightarrow$$

$$\frac{1}{R_2C_2}=6250 \qquad C_1=4\propto F \quad C_2=3.2nF$$

(33)

5.4 Simulations Comparison

In this paragraph we will analyse some simulations results that have been obtained by implementing on MATLAB/Simulink [4] two equivalent systems. In the first system the 24-pulses thyristors bridges have been considered simply as a linear gain. The rectifier has been implemented with some detail: it is essentially a voltage source with an internal impedance equivalent to the voltage drops of the actual rectifier. Also the voltage drop due to the different output current has been taken into account. A saturation block limits the maximum output voltage to the maximum of the actual converter thus considering also possible instabilities due to saturation effects. The low-pass filter, cables resistance, load impedance

have been implemented by suitable transfer functions blocks. The voltage and current loops have been implemented with the values of the parameters so far calculated.

An “actual” power converter has been simulated by the SimPowerSystem blockset of Simulink. Four thyristor bridges, two in series and parallel coupled, have been implemented with some detail on actual thyristors voltage drops, resistance and snubbers circuitry. Inductances, resistors and capacitors forming the various elements of the electrical network have been used for the simulation. Two three-windings transformers 2.8MVA each, have been also used with actual parameters to match the utility network voltage level of 15kV of the future installation to the one required by the converter. Utility network has been considered to have an infinite short circuit power. The same control system of the linear representation has been used to compare results.

In Fig. 45 the load current and voltage waveforms can be seen. The test reference current cycle used in the simulations is similar to the actual. Of particular interest is the acceleration ramp with cosine shape. The red curves are the output of the linear equivalent system, the blue ones are of the “actual” system. A perfect match of the results can be observed. In Fig. 44 the current error for the two systems is shown. In particular the start and end of the accelerating ramp is magnified in the second plot. It can be seen that the theoretical predictions on the maximum transient error are reproduced by the simulations. The specifications claimed for a maximum deviation of 30mA; by the plots it can be seen that the peak error is 70mA. This error is nevertheless restricted in a small time and it is possible to discuss with physicists if this short-time bump is acceptable. The tracking error of the cosine reference is well inside the admissible band (see the +0.015/-0.015 ticks on the plot). The major component of the error in the actual system is the one due to the switching of the thyristors at 1200Hz.

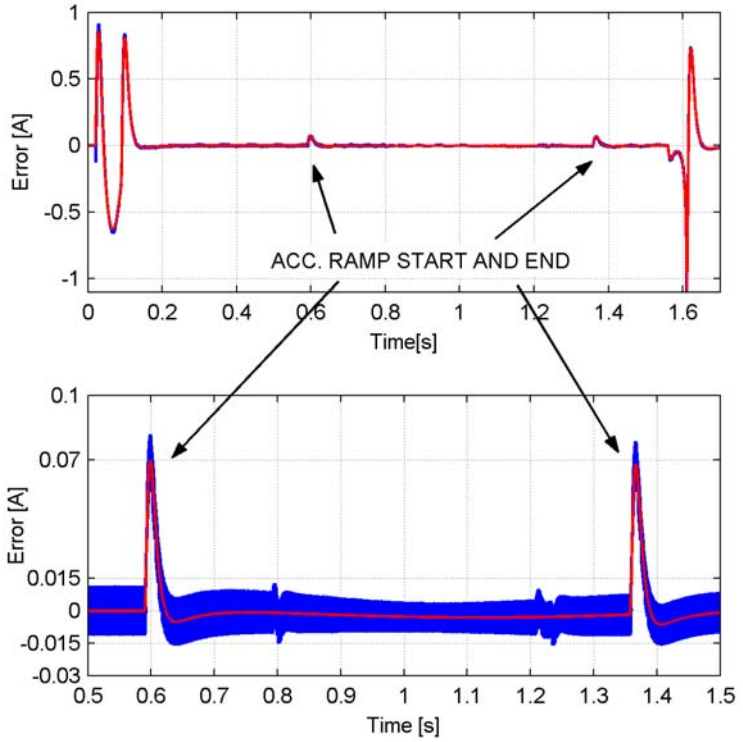

Fig. 44 – Current Error : linear system (red) actual thyristor converter (blue)

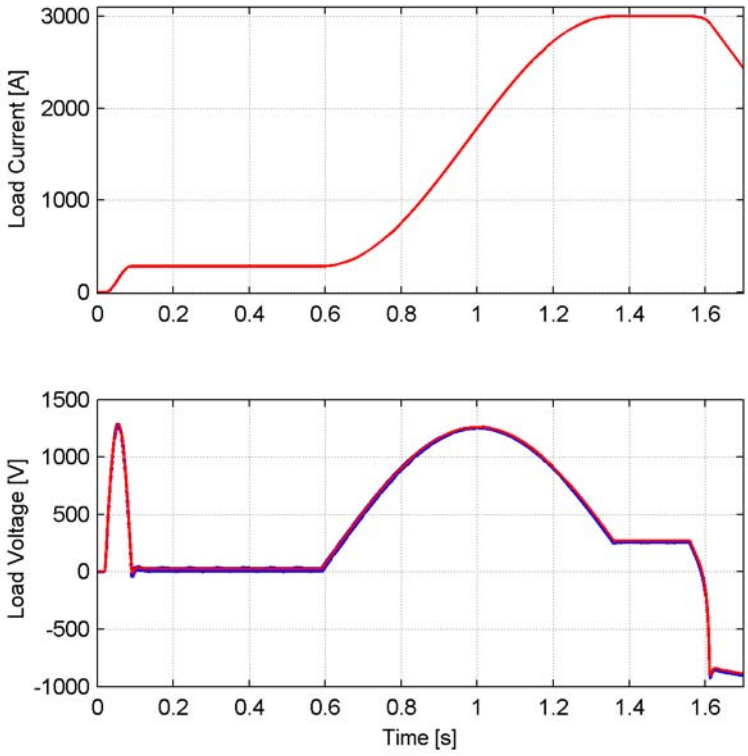

Fig. 45 – Load Current and Voltage: linear system (red) actual thyristor converter (blue)

A different current reference cycle has been also simulated to see the behaviour of the systems under more stressing conditions. In particular the accelerating cosine ramp have been increased in frequency although the maximum current flat-top have been reduced. From Fig. 46 and Fig. 47 it can be seen that the linear system and the actual system behaves in the same way. Thus the linear system representation can be used to make simulations on a large number of different cycles with a considerable reduction of simulation time. Once the cycle shape has been decided, a more detailed simulation can be run to have a deeper insight in system performance.

In Fig. 46 a relatively large peak error can be observed. The 300mA peak error is 10 times higher than the admissible one. This is why the design of the control system has been done considering a maximum cosine frequency of 1Hz. In this simulation the cosine frequency has been intentionally set to 2.5Hz to verify system performance and stability.

Another important issue to be discussed in detail with physicists is the small cosine ramp at the start of the cycle that brings the converter from the minimum current to the lower injection level (flat-bottom). This ramp has a fixed frequency of about 7Hz that is well above the 1Hz design frequency. Thus the peak transient error is relatively large, and also the time to achieve steady state conditions for the flat bottom is longer. It could be advisable to accept this error, thus not stressing the design parameters of the power converter, and delay of 50-100ms the injection of the beam in the ring thus waiting for the current to reach its steady state value and stability. In Fig. 44 and Fig. 45 this delay was set at about 400ms to test the simulation. The plots show that a smaller delay of 50-100ms is sufficient and the whole treatment would not suffer of excessive lengthen of the cycles period.

To increase system performance, for example reducing transient errors and current switching ripple, it seems demanding to foresee a suitable active filter that will have the task

of smoothing the current ripple components, as usually done by active filters used in particle accelerators power supplies, but it will have also the task of improve system transient response. The study of such a filter will be object of a future note.

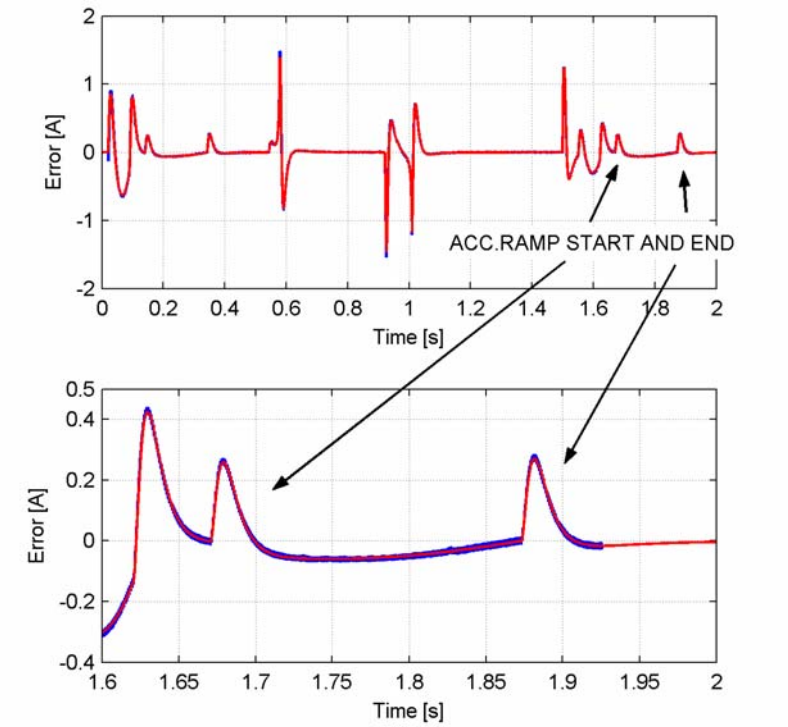

Fig. 46 – Current Error: linear system (red) actual thyristor converter (blue)

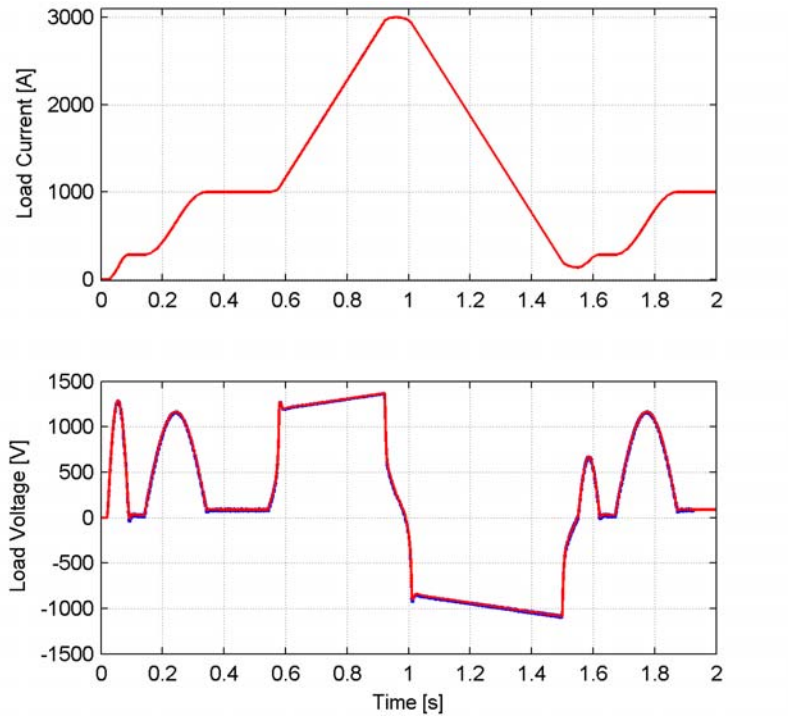

Fig. 47 – Load Current and Voltage: linear system (red) actual thyristor converter (blue)

As a further analysis the “highest performance cycle” has been simulated by the equivalent linear system to evaluate the magnitude of the current error under the most stressing conditions. The cycle has a flat-bottom current level of 334A corresponding to the one of Carbon ions injection and has the minimum flat-top level of $I_{max}/6$ thus giving the acceleration cosine ramp the maximum frequency. The results are depicted in Fig. 48 and Fig. 49. The plots clearly show that, although the converter maintains a still valuable performance (only 1A maximum error!), the current error during acceleration ramp is well behind the specifications. It is an obvious result if one looks at the acceleration ramp; it has been built, as asked, maintaining the maximum derivative constant at about 6000A/s – or (dB/dt)max=3T/s for the dipoles magnets – and setting the flat-top at the minimum level that is $B_{max}/6$. This way the half period of the cosine function becomes 46ms that means 10Hz equivalent frequency. Basing on the error plot of Fig. 40 a peak-to-peak error at 10Hz of 1.6A can be calculated for the steady state for the assumed cosine ramp.

The variations on load parameters have been also considered to evaluate the performance of the controller. The results are shown in Fig. 50 and Fig. 51 where both the variations in the load resistance and inductance have been considered. A maximum deviation of 10% from the estimated value have been taken into account but no study has been done to guess a reasonable value for this deviation, it is thus a completely arbitrary choice. The possible variations of load parameters during the cycling of the magnets have not been taken into account. It is clear from the analysis of the plots that, because the control performance relies for an important part on the feed-forward compensation, a deviation of some percents from the ideal values of the load parameters is reflected in the current error with a proportional percentage. In particular inductance variations are of major importance making the system losing performance at higher frequencies. Resistance variations are also important but, in the considered range seem to have a minor effect.

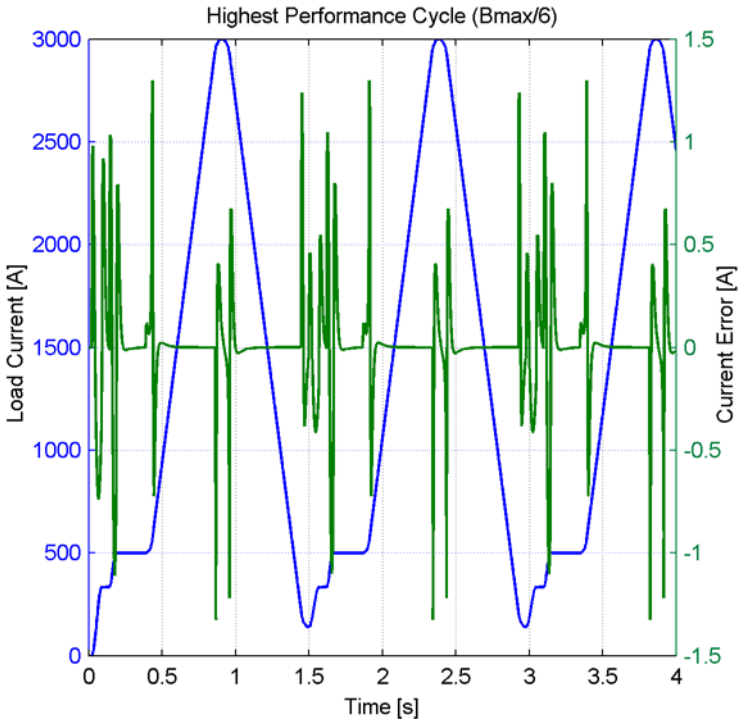

Fig. 48 – Load Current (blue) and Error (green) under strong operating conditions

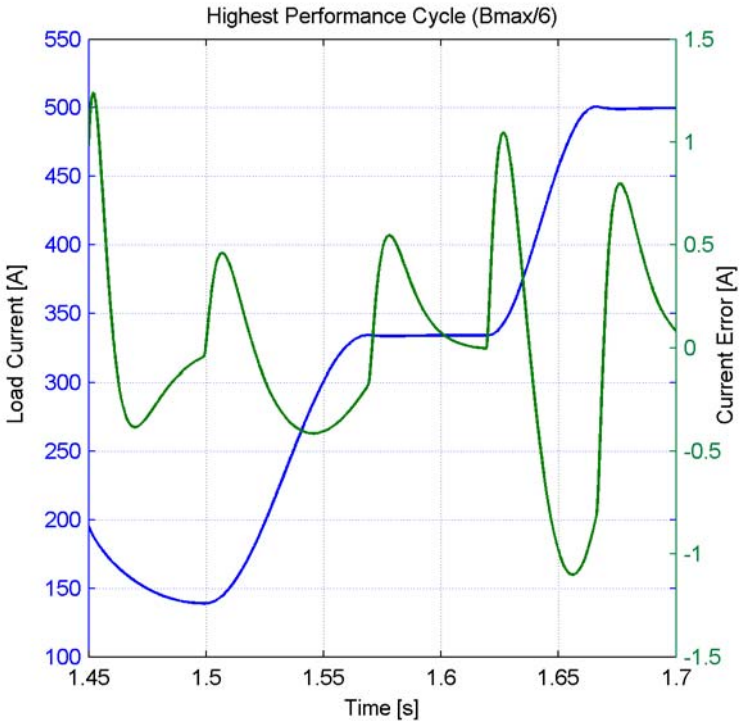

Fig. 49 – Load Current (blue) and load current error (green) under strong operating condition. Enlargement of Fig.47

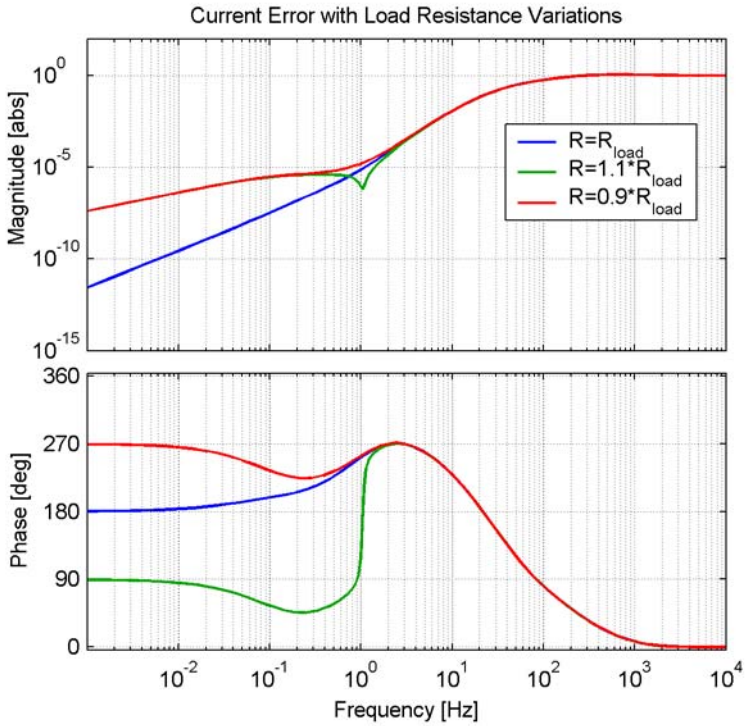

Fig. 50 – Current Error with Load Resistance Variations

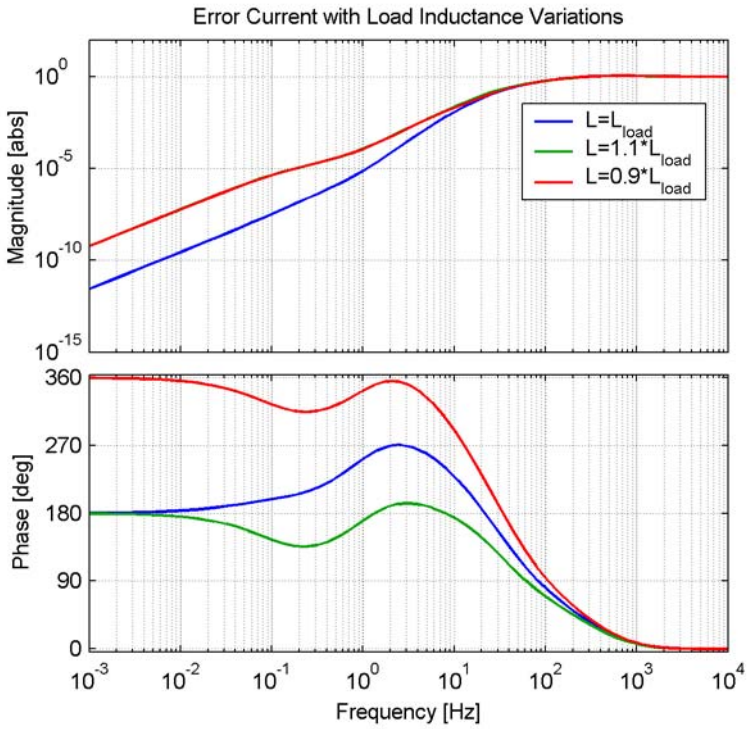

Fig. 51 – Current Error with Load Inductance Variations

6 SIMULATION RESULTS

The following simulation results are reported to point out some details of the simulated power supply that could be useful for a proper design. The cycle that has been chosen is the Carb2 cycle only as an example.

The load current and voltage of the Carb2 cycle are shown in Fig. 52. This cycle has been modified to improve the tracking capability, but in any case in agreement with the physics needs. The feedback here analysed is the one with a double integral controller (PII). The current error (I_{ref}-I_{meas}) is plotted in Fig. 53 together with the firing angles of the thyristor bridges. It can be easily seen that the load current suffers of three different sources of errors.

1) Switching Frequency Ripple: This is the ripple (Fig. 55) at thyristors switching frequency (1200Hz) and other spurious frequencies; it has an order of magnitude of about 80-90mA ($3*10^{-5}$ in per-unit of maximum current). The further reduction, needed to meet 10^{-5} specification, has to be achieved by active filter compensation.

2) Slow Transient Error: This is due to slow variation of the ramp rates. Although the double integral action determines zero steady-state error at ramp inputs, time constants of the system must be taken into account in determining transient performance.

3) Fast Transient Error: This error is due to fast variation of the ramp rates and it is due to the finite value of the switching frequency of thyristor bridges. Non-linear behaviour generates errors higher (Fig. 54) than the ones predicted by linear analysis. However, if these errors occur when there is no beam in the ring, they can be neglected.

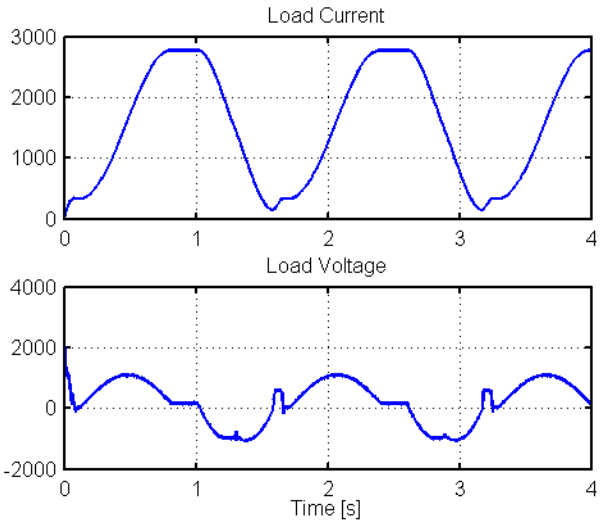

Fig. 52 – Load Current [A] and Voltage [V].

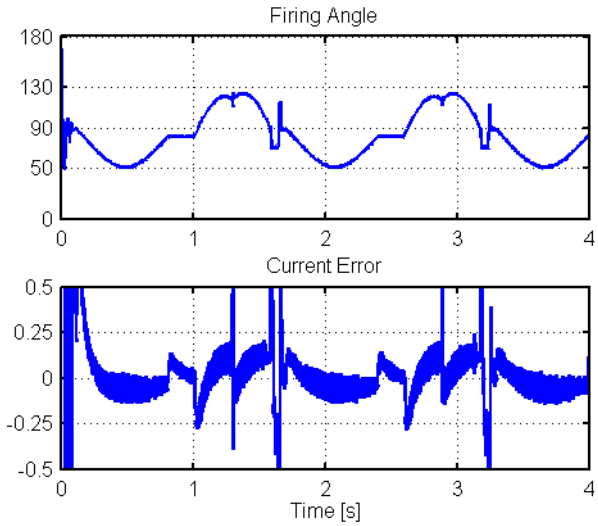

Fig. 53 – Firing Angle [deg] and Current Error [A].

The components recalled in the following are the ones shown in Fig. 8 to Fig. 10.

The peak value of the capacitor current is of great interest for the choice of the component. In Fig. 56 the current and voltage of the blocking capacitor C1 are shown. The maximum peak values of the current are in coincidence of fast voltage transitions especially when the load voltage must be reversed. Fig. 57 shows the current flowing through the capacitor C2, driven by the voltage ripple.

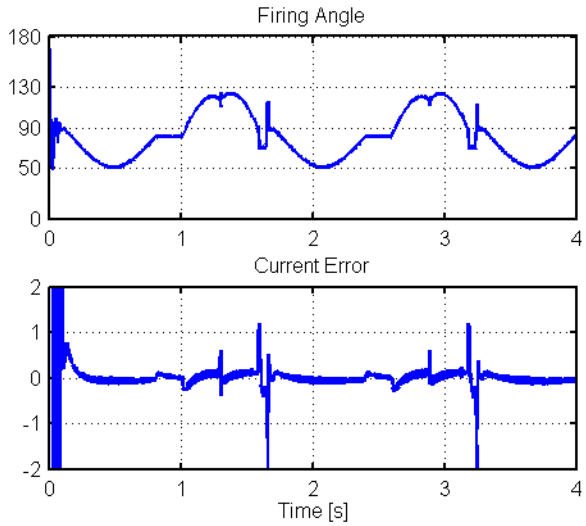

Fig. 54 – Firing Angle [deg] and Current Error [A] with higher scale.

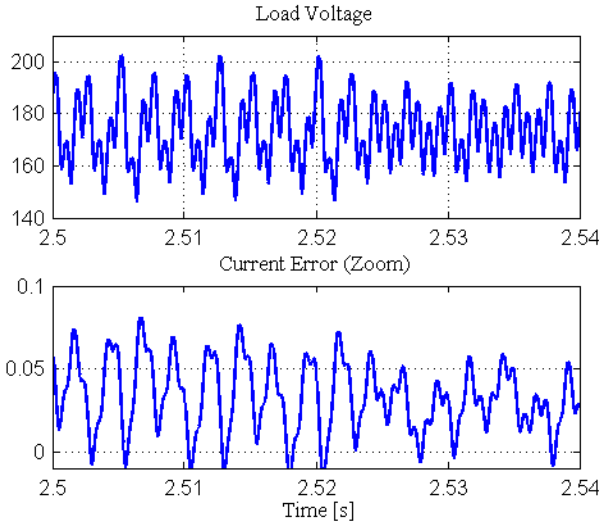

Fig. 55 – Load Voltage [V] and Current Ripple [A] (Enlargement).

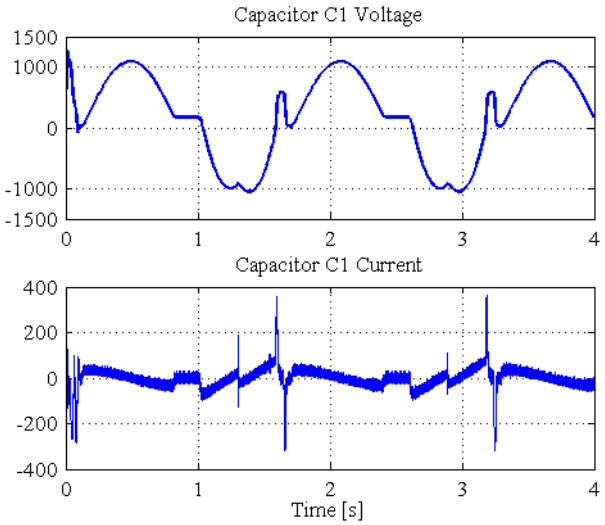

Fig. 56 – Capacitor C1 and C2 Voltage [V] and Current [A].

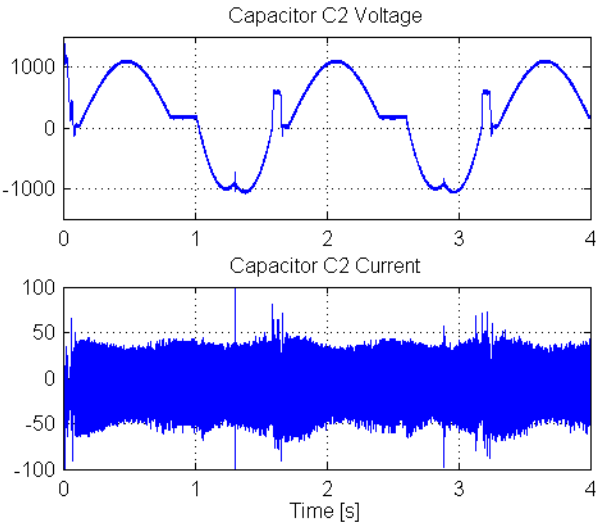

Fig. 57 - Capacitor C1 and C2 Voltage [V] and Current [A]. (Enlargement)

The currents flowing into the filter inductances are shown in Fig. 58 and Fig. 59. In the simulation, no additional loop was added to improve the correct current balance among the four bridges. Although the simulation shows a good current balance behaviour, the actual control system must provide also a suitable balancing loop to ensure an equal current sharing in the bridges that work in parallel.

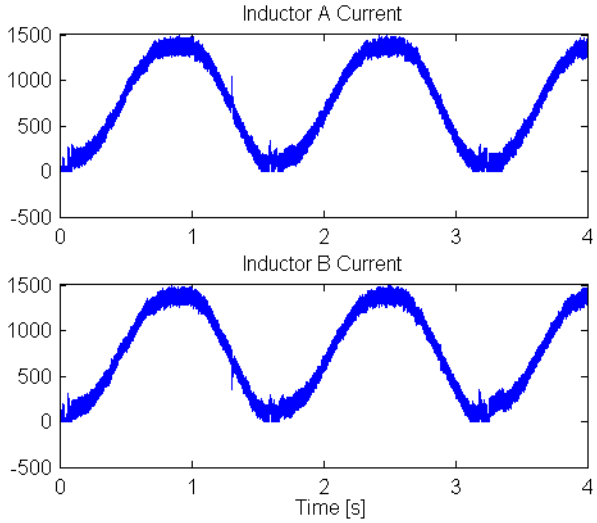

Fig. 58 – Filter inductors Currents [A].

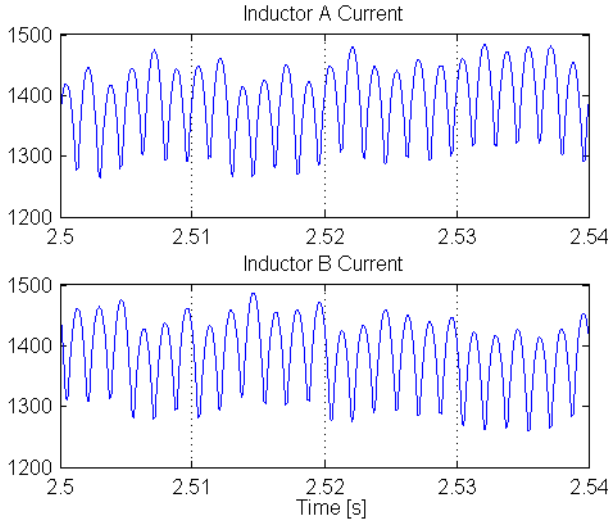

Fig. 59 – Filter inductors Currents [A]. (Enlargement)

The voltages across the two couples of bridges in series are shown in Fig. 60 as useful reference for low-pass filter dimensioning. Fig. 61 and Fig. 62, show the instantaneous active and reactive power. They have been “measured” directly with a virtual instrument in the simulation. The virtual instrument samples the line voltages and currents and calculates the average values over a 20ms period; these values are used to calculate the powers every 20ms. The total AC-power of the two three-winding transformers is shown in Fig. 62.

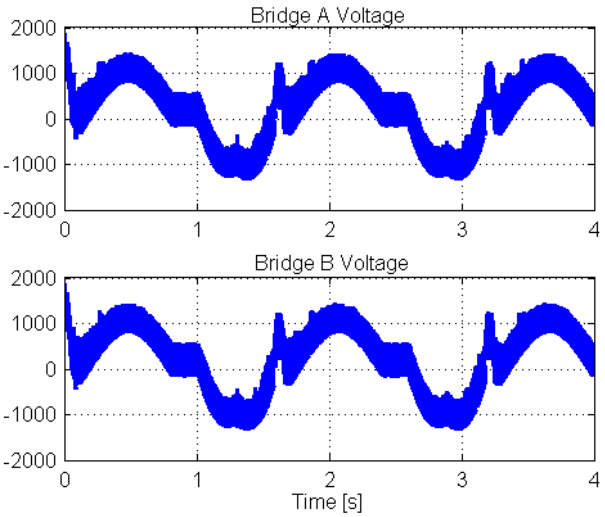

Fig. 60 – Series Bridges Voltages [V].

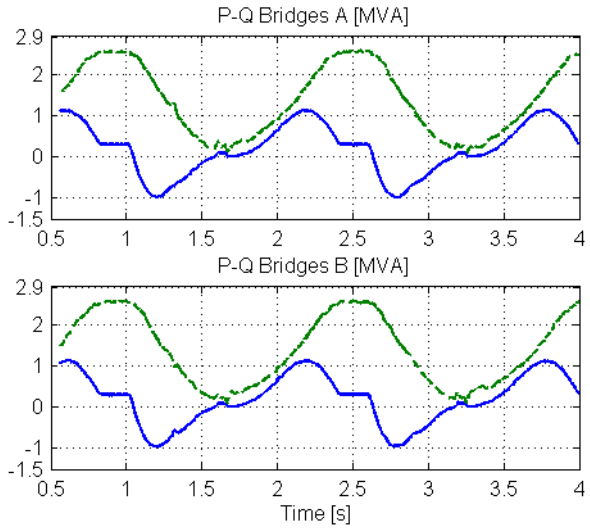

Fig. 61 – Line Active (Solid line) and Reactive (Dashed) Powers.

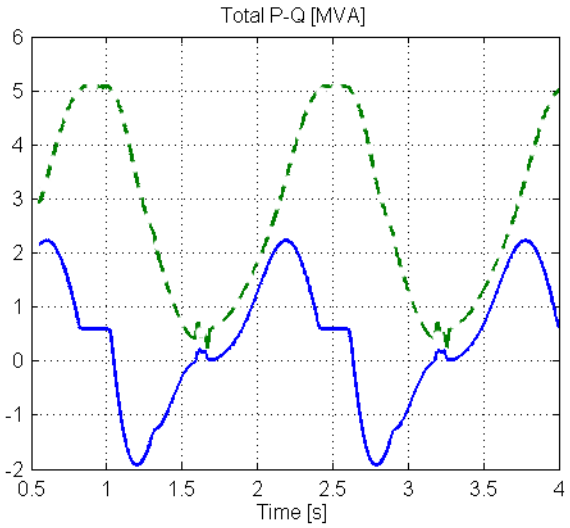

Fig. 62 – Total Line Active (Solid line) and Reactive (Dashed line) Powers

Different feedback controllers have been used to simulate the control feedback system. Fig. 63 shows the errors on the output current in the two cases with double and single integral controller. Although the PII feedback control gives zero steady-state error, both controllers are affected by relatively large transient errors, which could vanish the increased complexity of the double PI controller.

Another possibility that gives some improvements is shown in Fig. 65 where a forward action has been implemented in the control scheme. This solution seems to be the most suitable in our case but must be carefully evaluated considering also the type of the controller, analogical or digital, that will be employed. A zoom of the current errors in the last configuration is shown in Fig. 64 where the current ripple is affected by the switching component only.

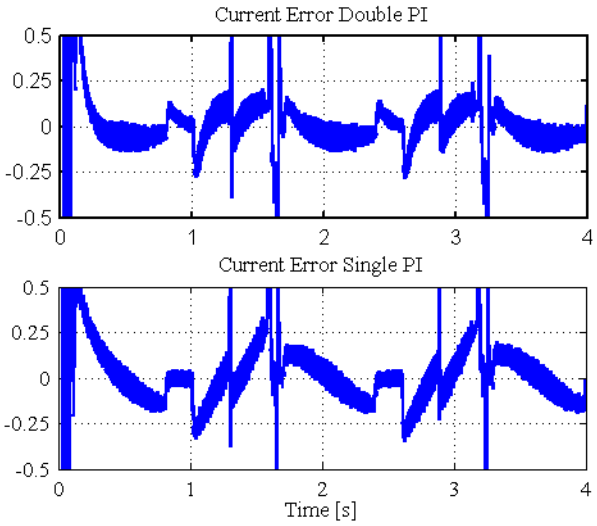

Fig. 63 – Comparison of Double and Single Integral Controller(Currents [A]).

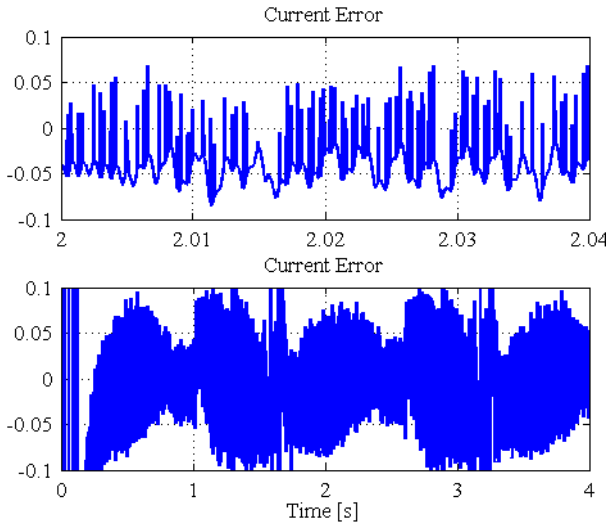

Fig. 64 – Current Errors [A] of Single PI and Feed Forward FCC (Enlargements).

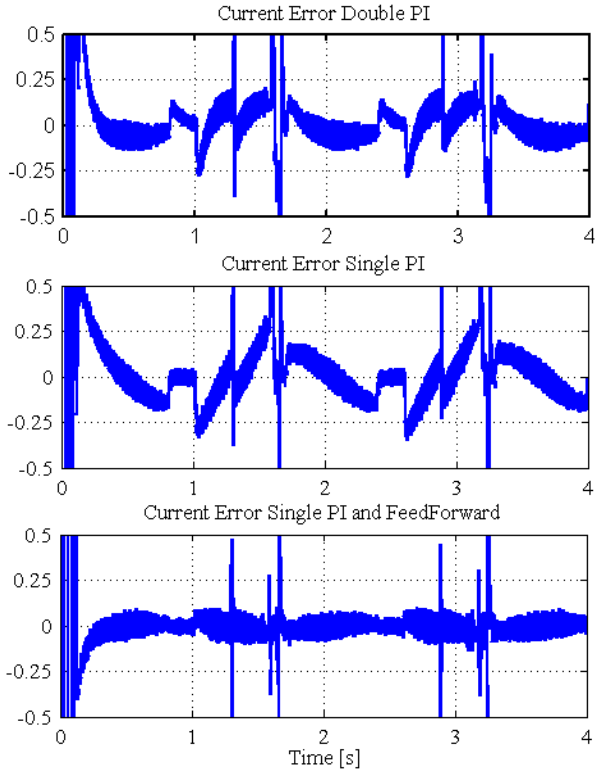

Fig. 65 – Current Errors [A] with different controllers.

7 FAULTS ANALYSIS

Some simulations have been done to study the effect of possible fault conditions on the elements of the power supply. The first fault taken into account was the interruption of thyristors gate signals to one bridge. The fault has been analysed with and without the crow-bar protection requested in the specification. This protection consists of two thyristors connected back-to-back, in series with a damping resistor, and in parallel with the load, as

shown in Fig. 76 at the end of this section. The damping resistor has been assumed to have a resistance of 50mOhm.

Let us consider first the situation without crow-bar protection. If an interruption of thyristors driving pulses occurs, the thyristors that were conducting at that moment cannot find an alternative path for the current; they remain in conduction feeding the filter and load with 50Hz un-rectified voltages. The load voltage is a 50Hz sinusoid, with 2000V peak amplitude, (see Fig. 66). The filter inductors begin to conduct a high current as shown in Fig. 67, which is also the current of the thyristors . This current is well behind the ratings of chosen components.

The same situation has been analysed with a crow-bar protection as described above. The protection has been delayed of 5ms, to take into account of possible intrinsic delays of actual circuitry. The results are shown in Fig. 69 to Fig. 72. It is crucial, for the crow-bar to work in a proper way, that means to be turned on before the current reaches high values, as shown previously in Fig. 67. The damping resistor has been added both to decrease the time constant of the load and to avoid large discharge current of auxiliary capacitor C_2.

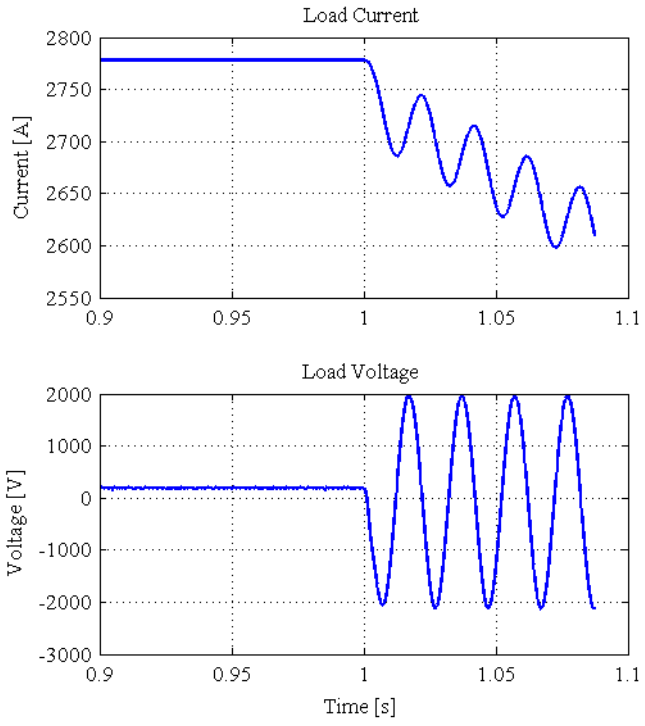

Fig. 66 – Load Current and voltage with thyristors stopped signals, without crow-bar.

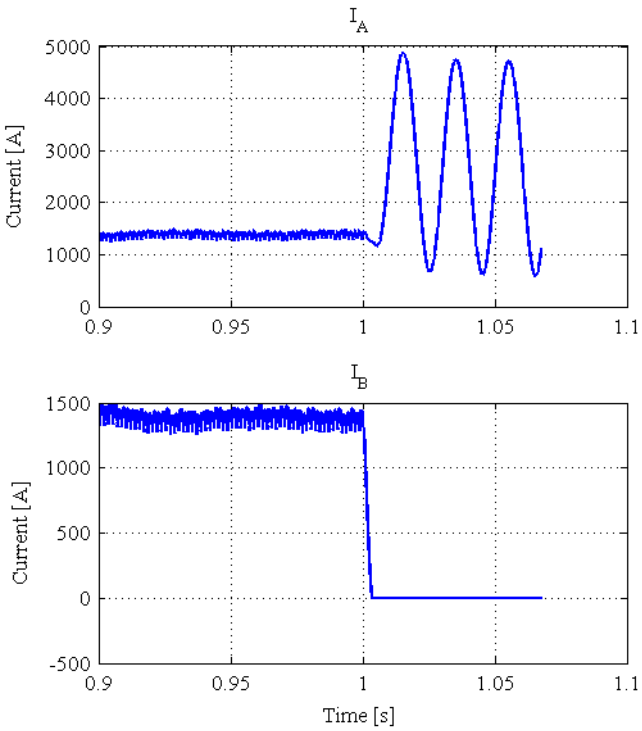

Fig. 67 – DC Inductors Current with thyristors stopped signals, without crow-bar.

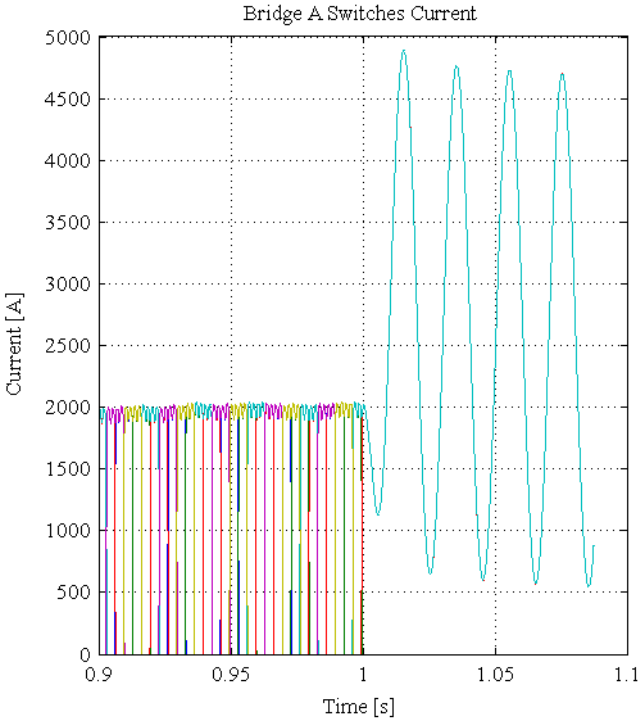

Fig. 68 – Thyristors Current with thyristors stopped signals, without crow-bar.

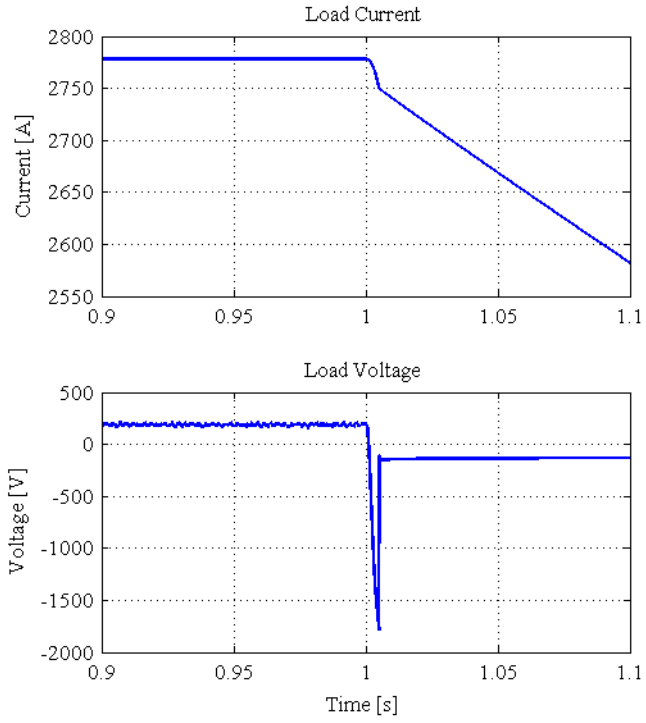

Fig. 69 – Load Current and voltage with thyristors stopped signals and Crow-Bar.

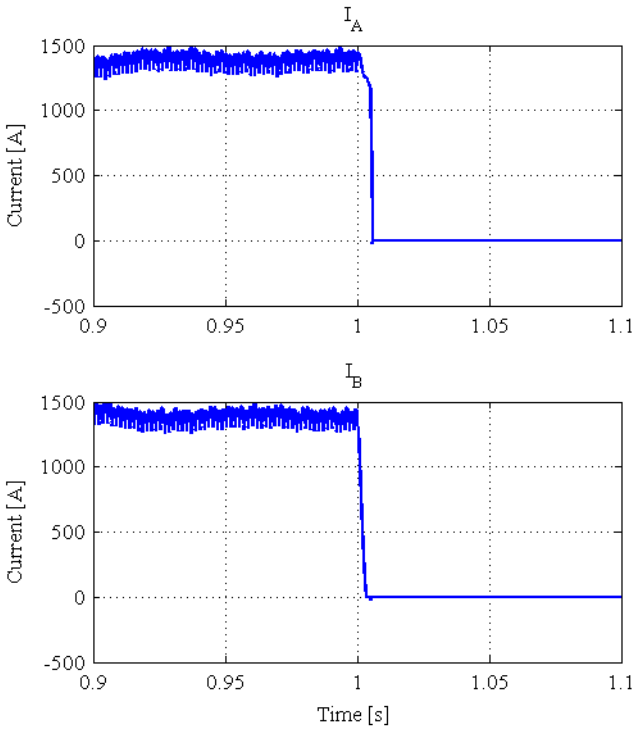

Fig. 70 – DC Inductors Current with thyristors stopped signals and Crow-Bar.

The crow-bar carries the load current in freewheeling and the energy is dissipated on the load resistance and the damping resistor. Filter inductances and bridges thyristors are not subject to anomalous currents. Filter capacitors are quite stressed during this fault condition.

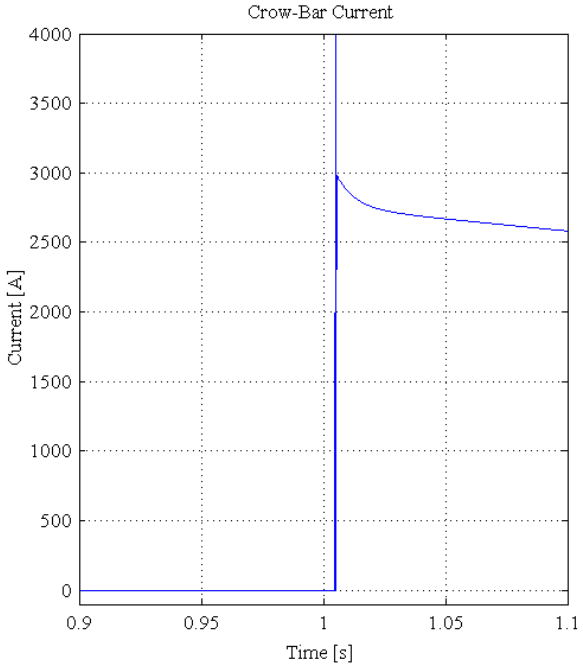

Fig. 71 – Crow-Bar Current with thyristors stopped signals.

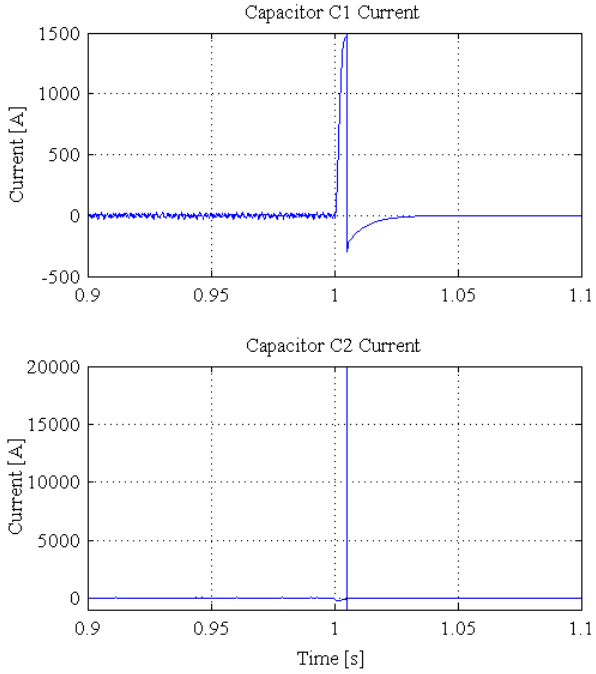

Fig. 72 – Capacitors Currents with thyristors stopped signals and Crow-Bar.

Other simulations have been done taking into account a black-out of the mains as fault condition. Results are shown in Fig. 73 to Fig. 75. In this case, all the thyristors share the load current, equally split between the two couples of bridges in parallel. In ideally symmetric conditions the current of every thyristor is within the continuous conduction limit of the components. However, it should be noted that the system in this situation is completely uncontrollable. The same simulation has been done with the crow-bar protection. It does not affect substantially the behaviour of the system under this fault condition; nevertheless, the crow-bar protection should be activated to prevent from some unbalances that could lead to different and dangerous current values in the bridges thyristors.

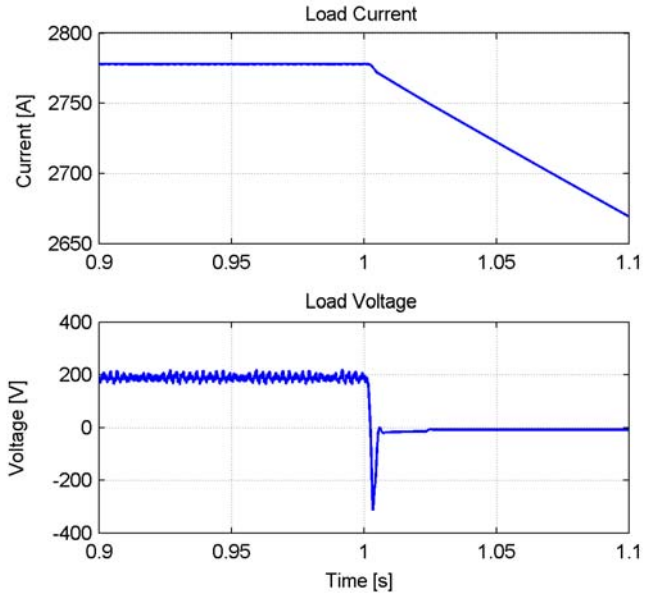

Fig. 73 – Load Current and Voltage mains black-out.

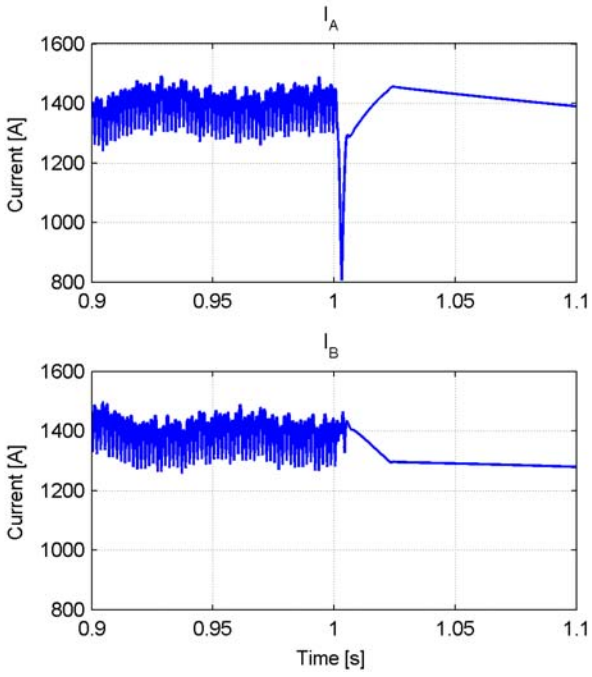

Fig. 74 – Filter Inductors Currents with mains black-out.

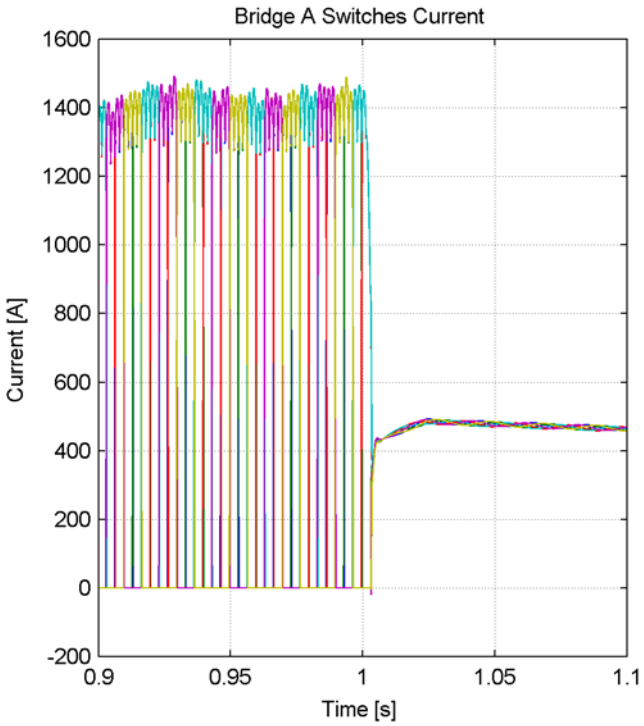

Fig. 75 – Bridge A Switches Currents with mains black-out.

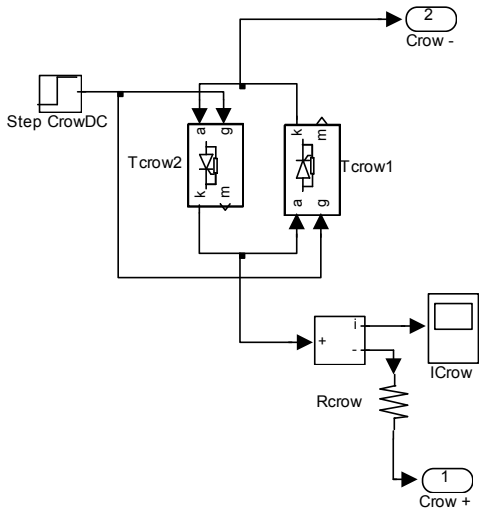

Fig. 76 – Crow-Bar protection implemented in the simulation.

8 CONCLUSIONS

12-pulse and 24-pulse converters have been compared and has been demonstrated that the stringent requirement on the 10^{-5} range output current ripple could be achieved, with some safety margin, only with the 24-pulse converter topology. A reasonable dimensioning of the power supply components is possible and realistic values have been given. Different possible feedback configurations have been studied. They work well but some little advantages arise from the FCC configuration. The final choice will come even after discussion with the builder and according to his experience. The results of the simulations show the feasibility of such a power supply and finally the fault analysis shows the absolute necessity to protect the power supply with a crow-bar protection immediately upstream the load series circuit.

Even if other possible topologies can be adopted and can work as well as the proposed one, this solution, based on a well-known technology, seems to meet all the requirements requested by the treatment plan. For the said reasons, the Specification will be based on this type of power converter, even if an exhaustive discussion with the builder will bring to a different topology if, not only the power supply requirements, but also the redundancy and reliability criteria will be met at the same, or better lower, cost.

9 APPENDIX A – SOME CALCULATED CYCLES

The following cycles have been calculated with the most recent values of the load 11.76mH inductance and 4.17mohm resistance per magnet and 2.7mohm of total cable connections resistance.

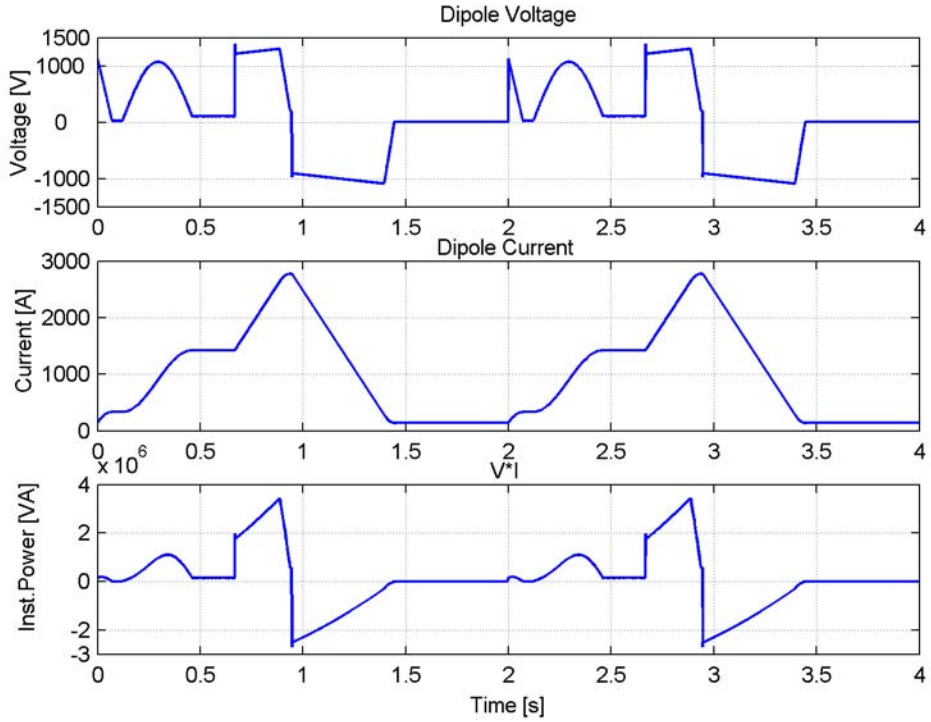

Fig. A1 - Carb 1 Cycle.

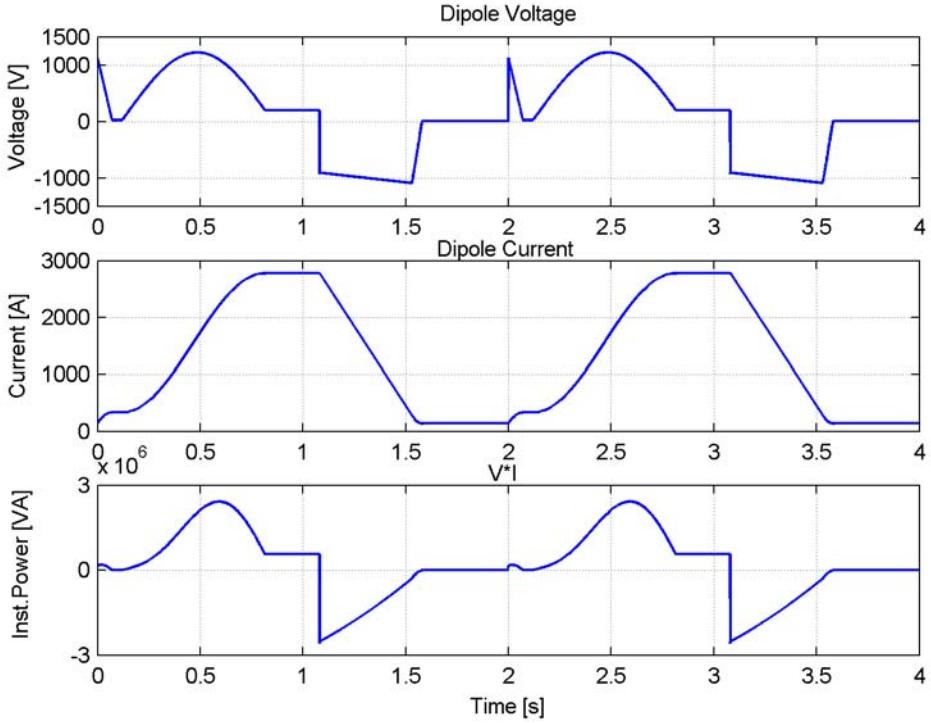

Fig. A2 - Carb 2 Cycle.

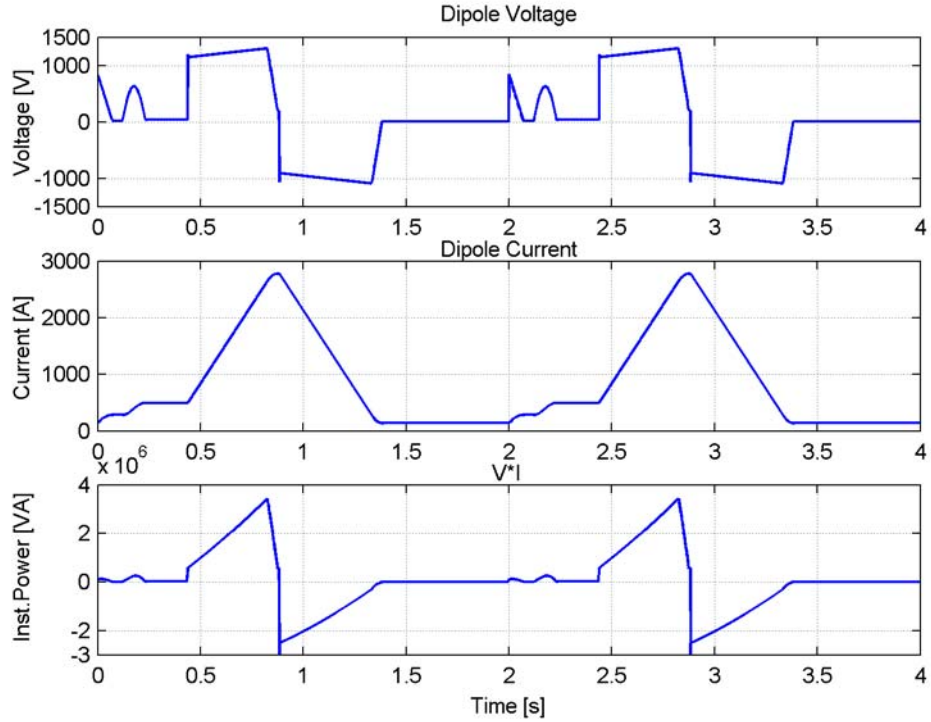

Fig. A3 - Prot 1 Cycle.

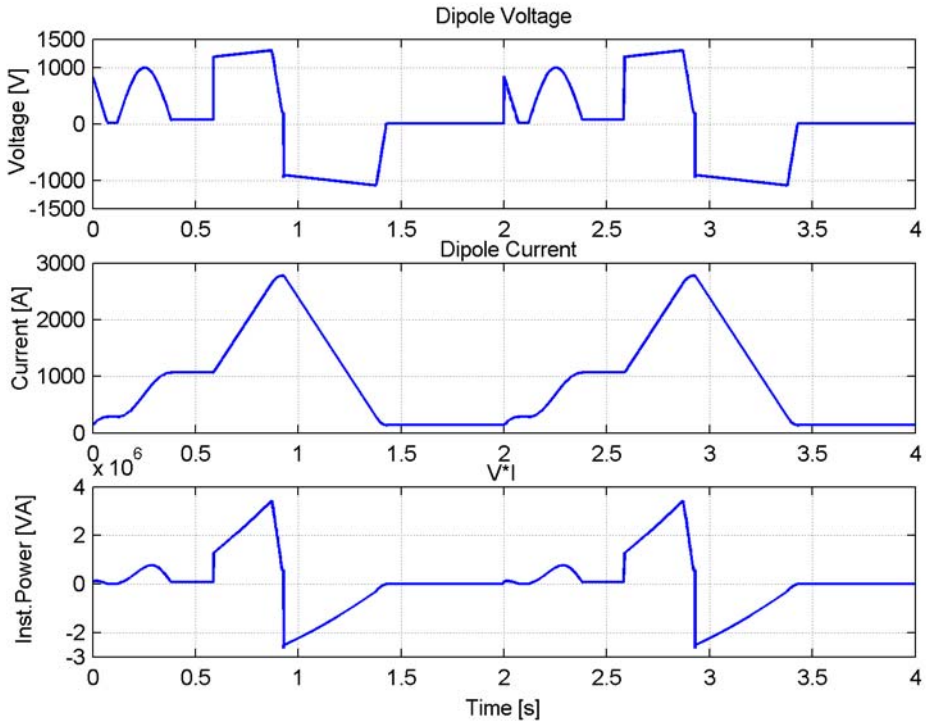

Fig. A4 - Prot 2 Cycle.

10 APPENDIX B – UPDATED SIMULATIONS

The following plots show the most recent simulations of the dipoles power supply so far described with an updated set of electrical parameters that have come out from the progress of the magnetic design of the magnets and from a tighter analysis of feedback parameters to improve transient behaviour of the system. In the following Table the most interesting parameters can be found.

Table B1 – Updated system parameters list

Load	
Resistance	74.8 m
Inductance	199.1 mH
Cables	Total Length: 280m 8 Cables in parallel, 240 mm^2 each Total Resistance: 3.11 m
Converter	
Maximum Voltage	±1600 V
Maximum Current	3000 A
Series Bridges Filter Inductance	2*800 ∝H
Filter Capacitor	2.46 mF
Filter Damping Resistor	0.8
Transformers	
Number	2
Windings	Ext.D-ext.d-ext.d
Primary Voltage	15 kV
Secondary Voltage	660 V
Secondary Current	1225 A
Apparent Power	2.8 MVA

The following simulations results have been obtained with the electrical parameters shown above. The details of the feedback control constants can be found in the preceding paragraphs.

We would like to point out the guidelines that lead to the design of the filter inductors and of the rectifiers transformers.

For the design of filter inductors, an exclusively technical point of view, has been taken into account; no technical-economical balancing between inductor and capacitor size has been considered. The size has been calculated to avoid non-linear behaviour of the rectifiers at low currents. In particular the equation used was:

$$I_{\underset{\min}{\text{average}}} = \frac{\varnothing V_{pk-pk}}{2 \infty \infty L}$$

where, $I_{average\ min}$ is the minimum average inductor current and $\varnothing V_{pk\text{-}pk}$ is the peak-to-peak voltage ripple (at minimum current) and L is the total filter inductance.

In the cycles to be tracked by the converter, it is foreseen a minimum load current of about 140A. This means for the minimum average inductor current a value of 70A. From the simulation it comes out a peak-to-peak voltage at minimum current of 800V at 600Hz. By substitution of these values in the above equation a value of 1.51mH is calculated that has been rounded at 1.6mH with some safety margin.

A more accurate evaluation of transformers size has been done too. It is based on the following equation:

$$V_{\mathrm{DCmax}} = 2 \cdot \left(k_1 \cdot V_{LL} - 0.1 \cdot V_{LL} - \frac{3}{\pi} \cdot x_{cc} \cdot \frac{V_{LL}}{\sqrt{2}} \right) - \alpha \cdot V_{\mathrm{DCmax}} - 0.05 \cdot V_{\mathrm{DCmax}}$$

where:

2→	is the constant for two bridges in series
k_1→	is the no-load rectifier constant that is taken 1.35
V_{LL}→	is the line-to-line AC voltage of one secondary of the transformer
0.1→	takes into account the minimum allowed line-to-line voltage (-10% of nominal)
$\frac{3}{\pi} \cdot x_{cc} \cdot \frac{V_{LL}}{\sqrt{2}}$ →	takes into account the voltage drop across the commutation inductance that is the transformer one. The original equation has been rearranged to use 50Hz per-unit reactance and line voltage as parameters.
$\alpha \cdot V_{\mathrm{Dcmax}}$→	takes into account the voltage drop on an equivalent resistance of the converter that has been calculated to have 90% efficiency at maximum current. For this value α=0.1.
$0.05 V_{\mathrm{Dcmax}}$→	takes into account a 18Ύregulation margin for the rectifiers at maximum voltage.

By substituting the values and rearranging for V_{LL} it is possible to calculate a value of 656V (rounded at 660V) for the line-to-line voltages of the secondary side of the transformers. As a consequence, a 2.8MVA apparent power is the transformer design power. By considering also the maximum allowed AC voltage (10% more of nominal) a 2000V maximum no-load DC voltage is calculated.

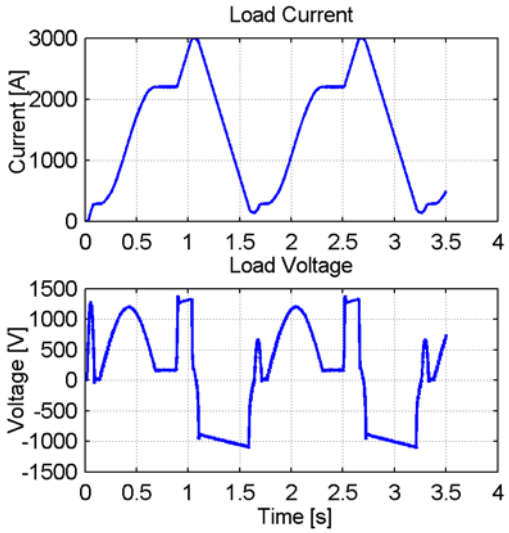

Fig.B1 – Load Current and Voltage

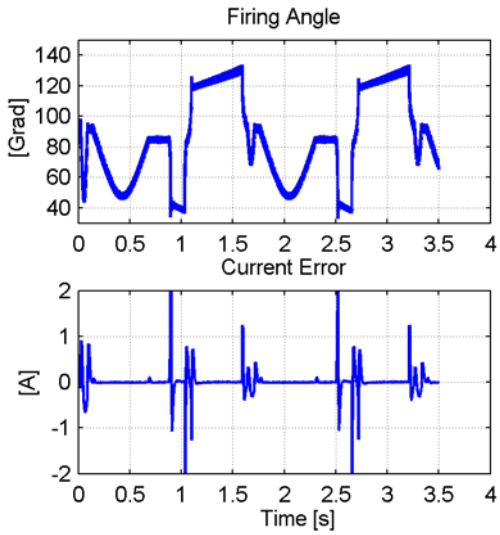

Fig.B2 – Thyristors Firing Angle and load Current Error

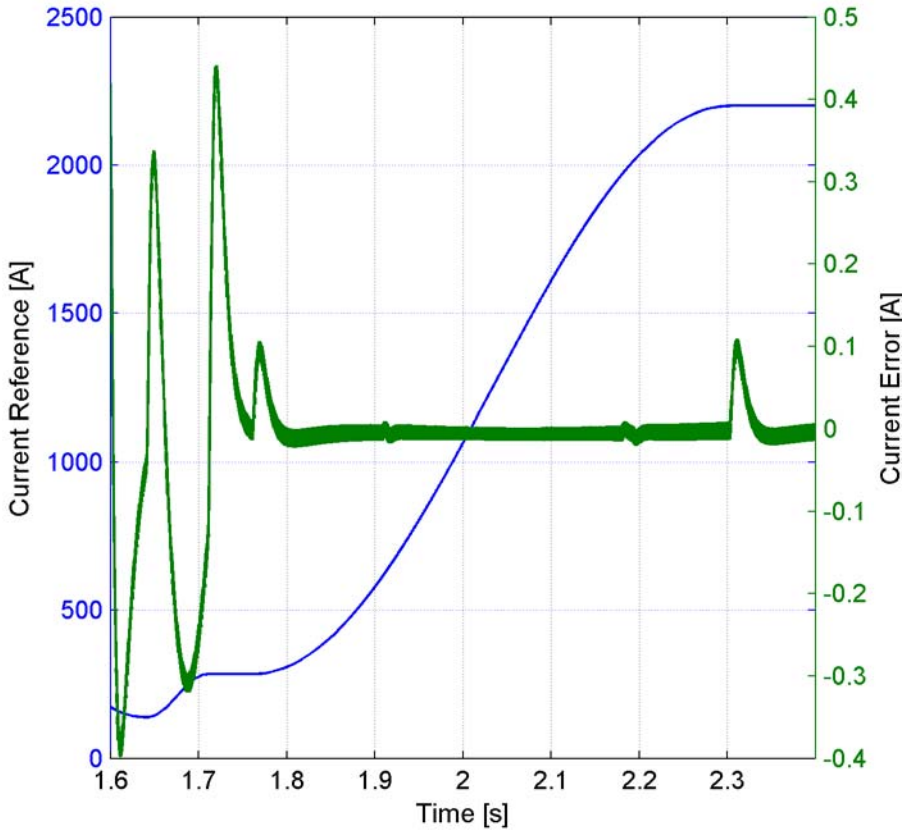

Fig.B3 – Transient errors at injection and acceleration.

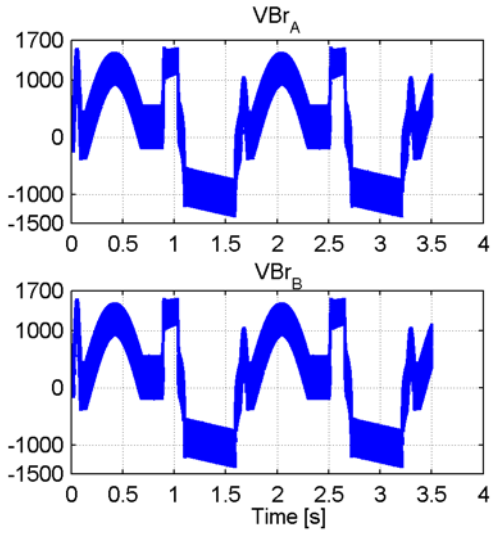

Fig.B4 – Series Bridges Voltage [V]

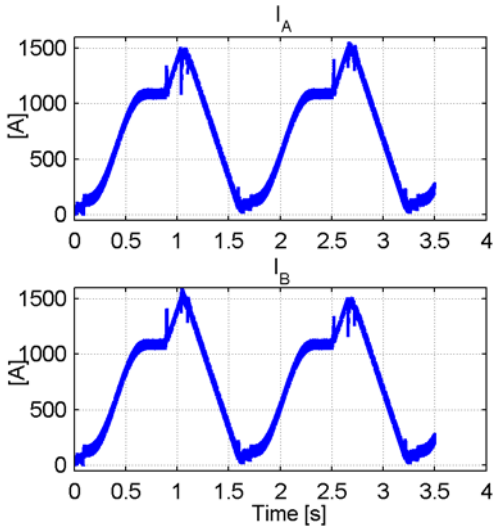

Fig.B5 – Inductor Currents

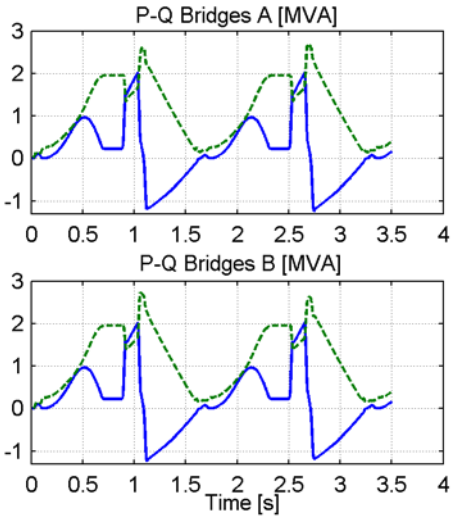

Fig.B6 – Line Active (Blue solid) and Reactive (Green dashed) Powers

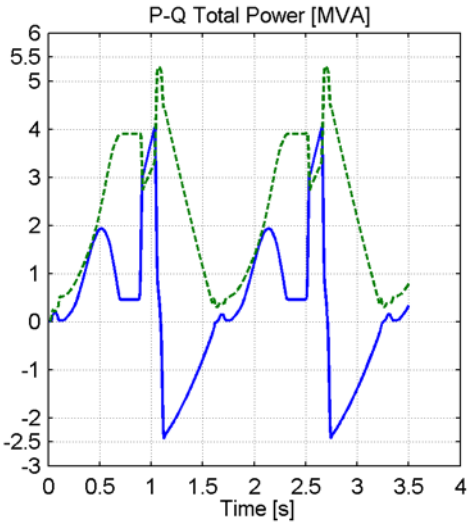

Fig.B7 – Line Active (Blue solid) and Reactive (Green dashed) Total Powers

The principle scheme of the proposed power supply is shown in Fig.B8 and can be found on the "Dipoles Power Supply Specification" [2]. It is worth noticing that an Active Filter is shown and proposed as a linear inductive coupled with series compensation filter. From the previous analysis it has been pointed out that the residual current ripple is of about 30 mA peak-to-peak, and cannot be compensated by thyristor bridges or by increasing low-pass filter size due to dynamic requirements. Although the ripple is within the specifications requirements – 30 mA that corresponds to 10^{-5} in p.u. of full-scale current – an active filter is demanding to compensate for line voltage fluctuations and to increase transient performance. As shown in Fig.B3, and well analysed in paragraph 4 of this note, the error bumps at the start and at the end of each ramp of the cycle are well behind the specifications and cannot be reduced by increasing the feedback gains or by increasing the low-pass filter corner frequency that would result in an increase of the current ripple and thus in the need for a suitable active filter.

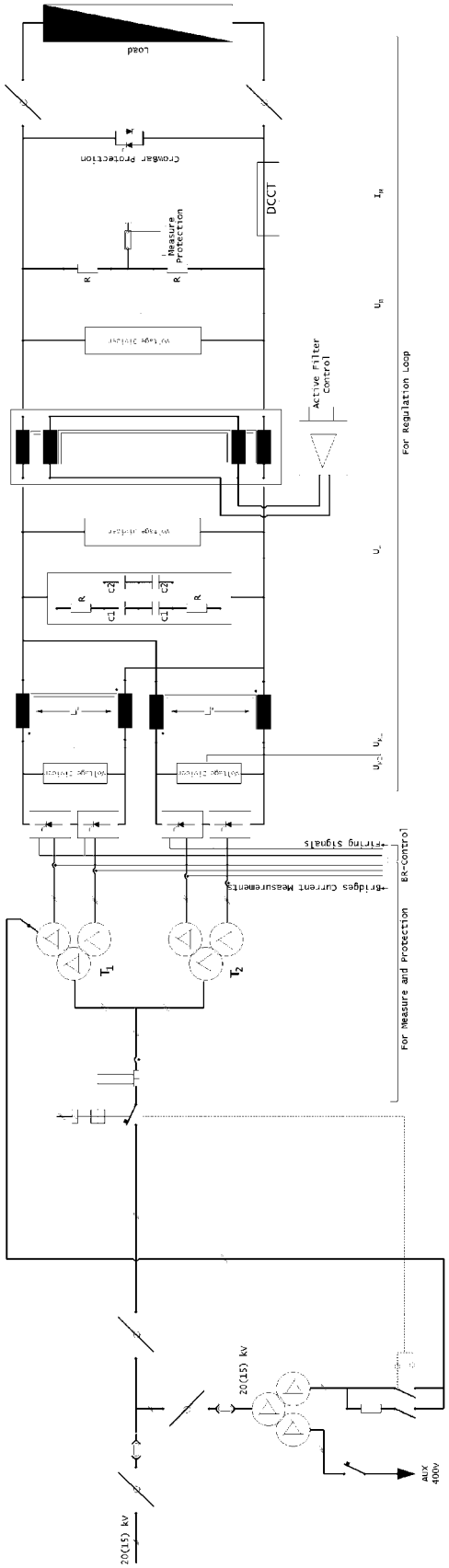

Fig. B8 - Power Supply Principle Scheme.

REFERENCES

[1] C.Sanelli – "Specification for dipole, quadrupole, sextupole and corrector magnets of the synchrotron accelerator CNA Project" — CNA-SPDP-005WXX-00270
[2] M.Incurvati, C.Sanelli – "Specification for n.1 power supply for dipole magnets of the synchrotron accelerator CNAO project" – CAN-SPDP-009WXX-00273
[3] B.C.Kuo – "Automatic Control Systems" – John Wiley and Sons, 7th Edition
[4] MATLAB/Simulink∞