LABORATORI NAZIONALI DI FRASCATI
SIS – Pubblicazioni

LNF-03/007 (IR)
6 Maggio 2003

LHCB MUON OFF-DETECTOR ELECTRONICS: THE IB SYSTEM

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Abstract

The LHCb muon trigger system is based on logical channels. For some stations and/or regions the logical channels correspond to the DIALOG outputs, while other stations and/or regions require a combination (OR) of channels coming from more than one chamber or more than one DIALOG output channels. In these cases special boards called Intermediate Boards (IB) are used to generate the logical channel. The 152 IB to instrument the muon detector will be located outside the chamber on the racks near the apparatus. Because of the radiation level foreseen near the detector (≅ 2 krad) radiation tolerant device must be used to implement the logic.

3. OVERVIEW

This document describes the Intermediate Board (IB) system used to build up the logical channels required by the LHCB muon trigger. Chapter 2 describes the geometry of the readout electrodes requiring the IB boards to generate the logical channels while chapter 3 explains the adopted solution to fulfil the topology experiment requirements. Lastly chapter 4 shows the results of measurements made on the IB board first prototype and chapter 5 gives the status of the project.

4. CHAMBER GEOMETRIES

The most elementary part of the LHCB muon trigger system is build by the ODE board and is defined as *sector (or Optical Link)*. The ODE board generates the *sectors* starting from the *logic channels*. For some stations/regions the *logic channels* correspond to the DIALOG outputs; for example all the DIALOG outputs of station M1 correspond to *logical channels*. On the other hand, for some regions of station M2-M5, DIALOG outputs coming from different chambers are required to make *logical channels*. Table 1 shows the station/region requiring further electronics (with respect to the ON-Chamber electronics) to build up *logical channels*. While fig 1-5 show the readout electrodes geonetry listed on table 1.

Table 1: Number of IB required to build up logical channels per Station/region

	M1	**M2**	**M3**	**M4**	**M5**
R4		24	24	8	8
R3		24	24	8	8
R2				12	12
R1					

3.1. M2/M3-R3

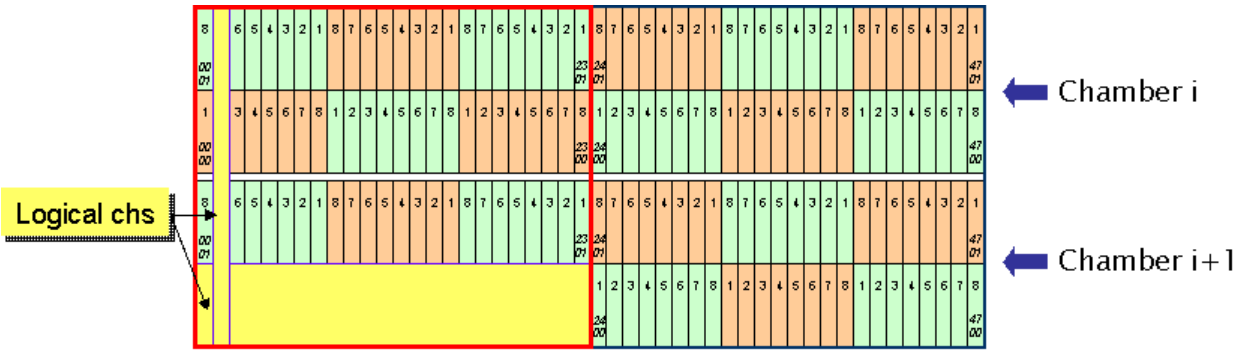

Figure 1: M2/M3-R3 Optical Link structure

The Optical Link structure for region R3 of station M2 and M3 is shown in red in fig. 1. It is made of 28 *logic channels* built starting from 96 DIALOG outputs. The DIALOG outputs come from two different chambers. Details are given in table 2.

Table 1: M2/M3-R3 chambers readout channels

Number of chambers	48 (M2) + 48 (M3)
Chamber type	48CP2
Phys chs (1 chamber)	96x2
DIALOG out chs (1 chamber)	96
Logic V chs (1 OL)	24
Logic H chs (1 OL)	4
Output signal modularity	8 differential (LVDS)
Number of connectors / FEE cards (1 chamber)	12
IB modularity	96x2 in – 28x2 out (2 chambers/IB)
IB number	24 (M2) + 24 (M3)

3.1. M2/M3-R4

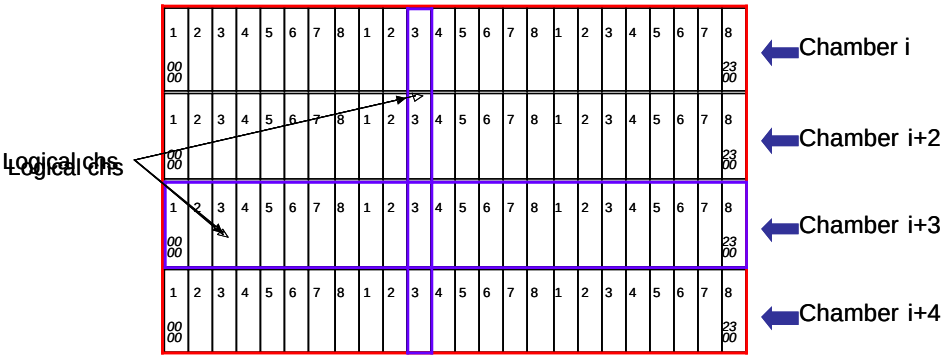

Figure 2: M2M3-R4 Optical Link structure

The Optical Link structure for region R4 of station M2 and M3 is shown in red in fig. 2. It is made of 28 *logic channels* built starting from 96 DIALOG output channels. The DIALOG channels come from four different chambers. Details are given in table 3.

Table 2: M2M3-R4 chamber readout channels

Number of Chambers	192 (M2) + 192 (M3)
Chamber type	24WP
Phys chs (1 chamber)	24x2
DIALOG out chs	24
Logic V chs (1 OL)	24
Logic H chs (1 OL)	4
Output signal modularity	8 differential (LVDS)
Number of connectors/FEE boards (1 chamber)	3
IB modularity	192 (96x2) in – 56 (28x2) out (8 Chambers/IB)
IB number	24 (M2) + 24 (M3)

3.1. M4/M5-R2

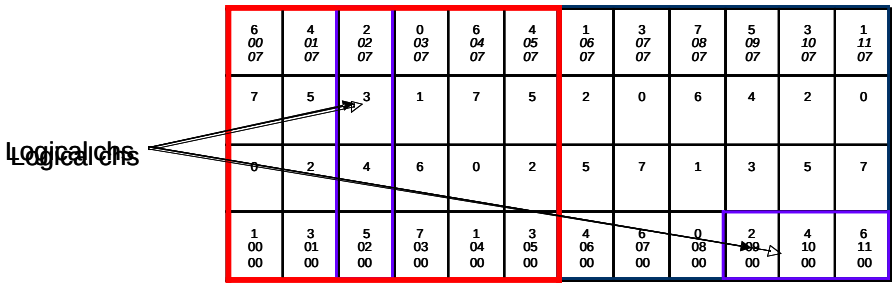

Figure 3: M4M5-R2 Optical Link structure

The Optical Link structure for region R2 of stations M4 and M5 is shown in red in fig. 3. It is made of 14 *logic channels* built starting from 24 DIALOG output channels. The DIALOG channels belong to the same chamber. Details are given in table 4.

Table 3: M4M5-R2 chamber readout channels

Number of Chambers	24 (M4) + 24 (M5)
Chamber type	12CP4
Phys chs (1 chamber)	48x2
DIALOG out chs (1 chamber)	48
Logic V chs (1 OL)	6
Logic H chs (1 OL)	8
Output signal modularity	8 differential (LVDS)
Number of connectors / FEE cards (1 chamber)	6
IB modularity	96 (48x2) in – 56 (14x2x2) out (2 Chamber/IB)
IB number	12 (M4) + 12 (M5)

3.1. M4/M5-R3

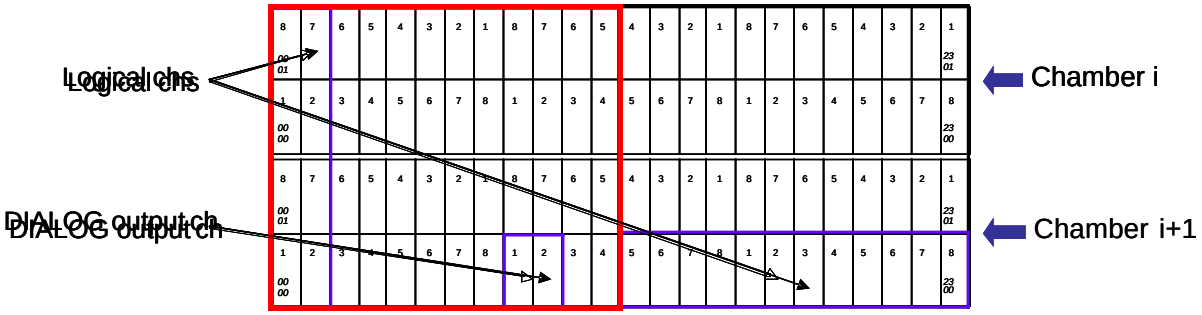

Figure 4: M4M5-R3 Optical Link structure

The Optical Link structure for region R3 of station M4 and M5 is shown in red in fig. 4. It is made of 10 *logic channels* built starting from 24 DIALOG output channels. The DIALOG channels come from two different chambers. A pre-OR of two neighboring channels is done to reduce the number of FEE outputs. Details are given in table 5.

Table 4: M4M5-R3 chamber readout channels

Number of Chambers	48 (M4) + 48 (M5)
Chamber type	24CP2
Phys chs (1 chamber)	48x2
DIALOG out chs (1 chamber)	24
Logic V chs (1OL)	6
Logic H chs (1 OL)	4
Output signal modularity	4 differential (LVDS)
Number of connectors / FEE cards (1 chamber)	3
IB modularity	144 (24x6) in – 60 (10x6) out (6 Chambers/IB)
IB number	8 (M4) + 8 (M5)

3.1. M4/M5-R4

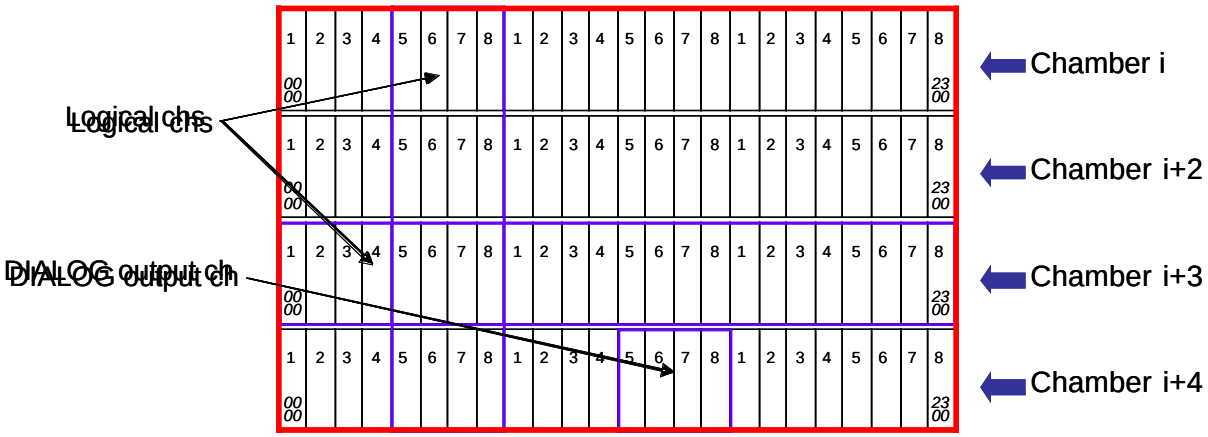

Figure 5: M4M5-R3 Optical Link structure

The Optical Link structure for region R4 of station M4 and M5 is shown in red in fig. 5. It is made of 10 *logic channels* built starting from 24 DIALOG output channels. The DIALOG channels come from four different chambers. A pre-OR of four neighboring channels is done to reduce the number of FEE outputs. Details are given in table 6.

Table 6: M4M5-R4 chamber readout channels

Number of Chambers	192 (M4) + 192 (M5)
Chamber type	24 CP1
Phys chs	24x2
DIALOG out chs (1 chamber)	6
Logic V chs (1 OL)	6
Logic H chs (1OL))	4
Output signal modularity	2 differential (LVDS)
Number of connectors / FEE boards (1chamber)	3
IB modularity	144 (24x6) in – 60 (10x6) out (24 Chambers/IB)
IB number	8 (M4) + 8 (M5)

3. The IB system

The Intermediate Board is the logic used to build up *logic channels.* This logic is located on both sides of the apparatus to minimize the length of the connection cables and it's made of two main parts, the Intermediate Boards itself and the Transition Board (fig. 6).

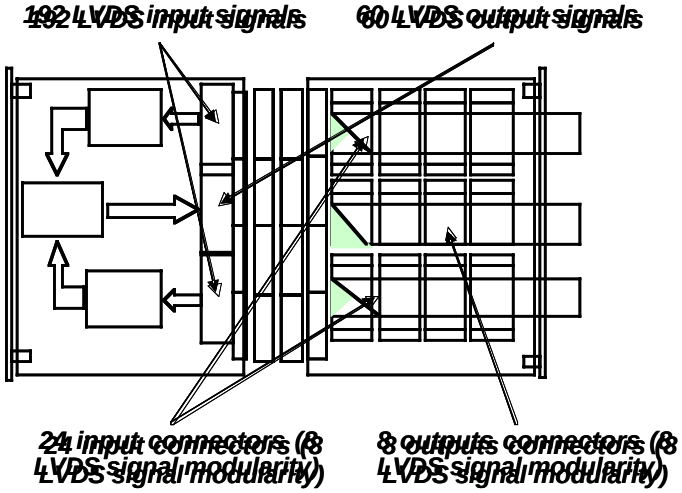

Figure 6: IB and TB block diagram

This two boards structure allows matching the chamber output connectors with the high density IB input connectors. Then a single layout of the IB board can be used to match the full muon detector topology if programmable components are used to generate *logic channels*.

3.1. The IB board

The main goals of the IB design were:

- Use a single board to match the full muon detector chamber geometry
- Maintain the outputs time skew within 3 ns
- Use components able to work with a (maximum) radiation integrated dose of ~ 2 krad.

While the first item can be easily archived using FPGA components to implement logic functions, the second goal requires an accurate layout of the board (path length must be almost the same for the 192 input signals). Then the IB has been designed with a symmetric structure both for component placement and for wires routing.

Anyway, the main source of time skew comes from the FPGA used to match the different chamber geometries. In fact, the routing architecture resources of the FPGA allows only a limited control on the signals transit time.

Because the requirements on the radiation dose an Actel device (54SX16A) based on antifuse technology has been chosen. The Actel 54SX16A has an internal architecture with two different types of cells, one with combinatorial logic (C-cells) and the other with flip-flop (R-cells), as shown in fig. 7.

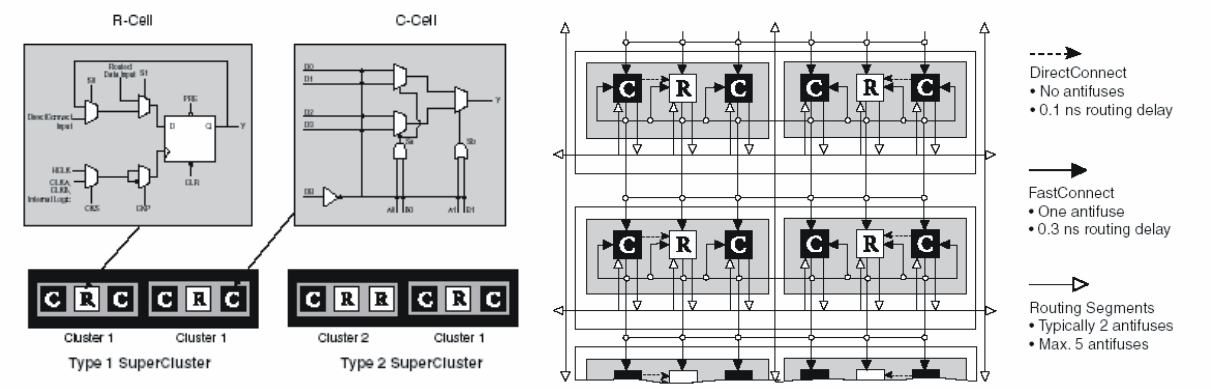

Figure 7: ACTEL 54SX-A type of cells and routing resources.

Three devices have been mounted on the IB board to optimize signals path. The first two (upper and lower) collect input signals and makes a pre-OR of them, while the third (the central one) receives the outputs of the previous FPGAs and builds-up the logic channels.(fig. 8).

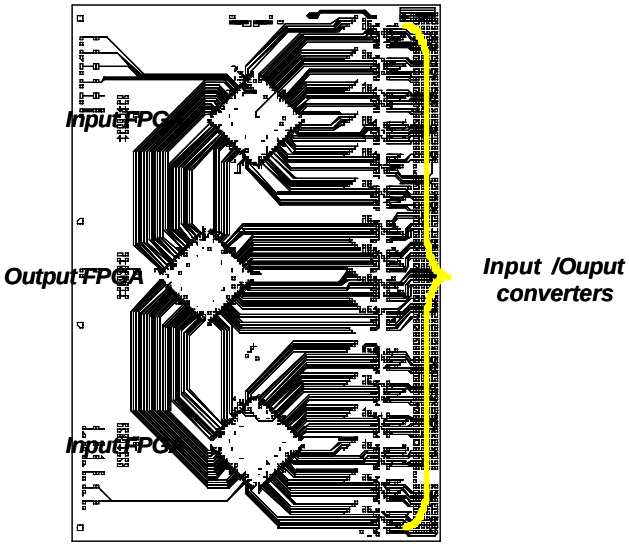

Figure 8: IB board layout

The circuit has been implemented as a tree structure that is spanned over all the FPGAs. Fig. 9 shows a part of the OR structure for the input FPGAs.

The inverted logic chosen to implement the OR function (as shown in fig 9) is due to the behaviour of the

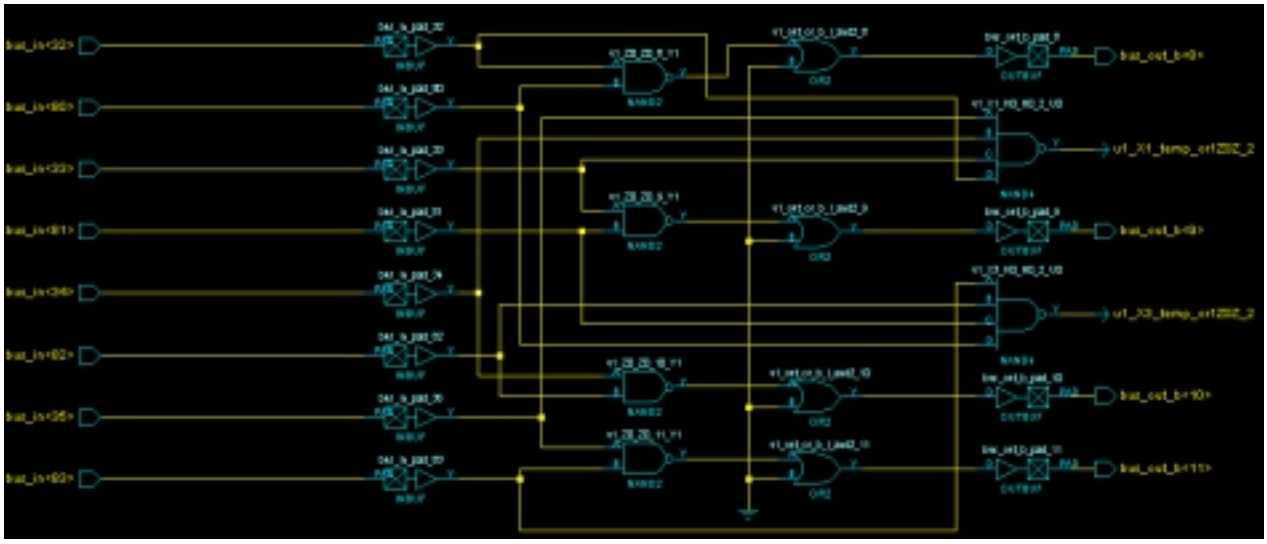

Figure 9: Input FPGA OR structure

74LVDT388 and 74LVDT389 TTL/LVDS converter used to translate (input/output) LVDS logic to the FPGA TTL logic. Actually the LVDS-TTL converters have a “high” output level when their inputs are open. Then using standard OR logic the IB output would be stuck to a “high” level in case of open input connection. The OR gates with a connection to ground are used as delay elements in the signal paths.

As the synthesis software automatically removes redundant logic to reduce resource occupancy, this optimization would destroy the symmetry of the circuit worsening the signal skew. Then particular directive have been set on the synthesis to avoid optimization. Finally timing constraints have been used to control propagation delay inside the FPGA.

An eight layer PCB has been used to route all signal. The IB first prototype is shown in Fig 10.

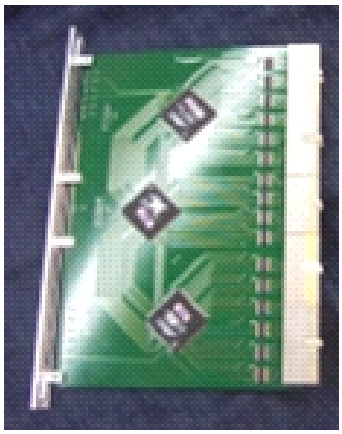

Figure 10: IB board (1st prototype)

3.2. The TB board

As already said, the transition board matches the chambers FEE modularity to the IB high density input connectors. The prototype of one of the two types of boards we need to fit all the chamber geometries is shown in Fig 11.

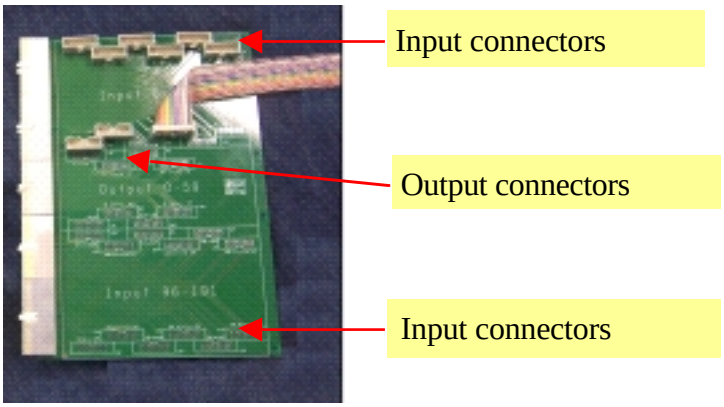

Figure 11: TB 1st prototype

It can manage up to 24 input and 8 output connectors and has been implemented using an eight layer PCB because the high number of input/output channels. Both input/output connectors have modularity equal to 8.

3.3. The IB crate

Both IB and TB board have been implemented according to the VME 6U mechanical standard. The 6U VME crate that hosts these boards uses a custom backplane. The backplane (fig. 12) allows to interconnect IB and TB board and to distribute low voltage (+ 3.3V and +2.5V) to the boards. The crate can host up to 16 IB boards. Fig. 13 shows the crate prototype we have used in our measurements.

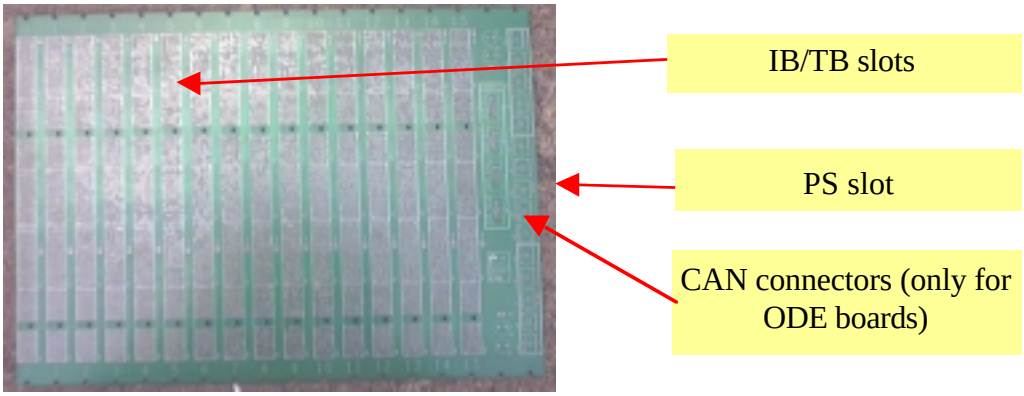

Figure 12: IB crate backplane

Figure 13: The 1st prototype of the IB crate

4. Simulation and test results

PCB traces delay is well known, than we concentrated our efforts on the simulation of ACTEL devices to minimize the output signal time skews. As M2/M3-R3 (fig. 1) is the worse case of chamber/OL topology (one DIALOG channel contribute both to vertical and horizontal *logic channels*; vertical *logic channels* are made of four channels coming from two different chambers, while horizontal *logic channels* are made from 24 channels belonging to the same chamber) we worked on this configuration. The fig. 14 shows the simulation results of time skew for 96 signals with time constraints set to control signal time delay (we show only 96 out of 192 because the M2/M3-R3 IB is made of two identical blocks).

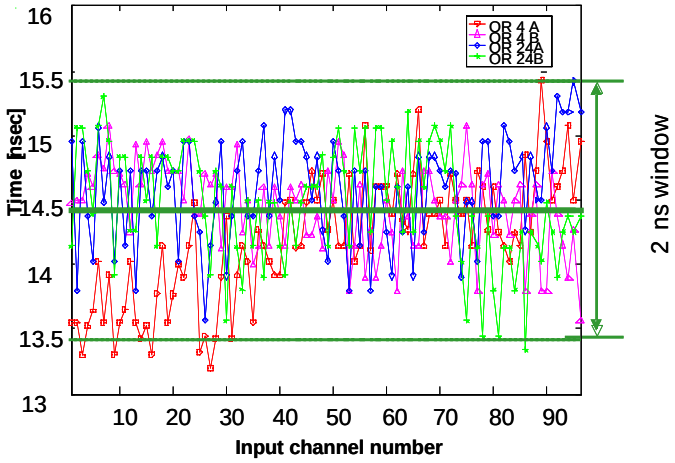

Figure 14: Output signal time skews (simulation)

FPGA were configured according to the results of simulation and the first IB prototype was assembled. The results of time delay measurements are shown in fig 15. The measurements show that only one channel is outside the 3 ns window required, while most of the channels are inside a two ns window. Looking for the problem of this “out of window” channel we found a failure in a LVDS receiver.

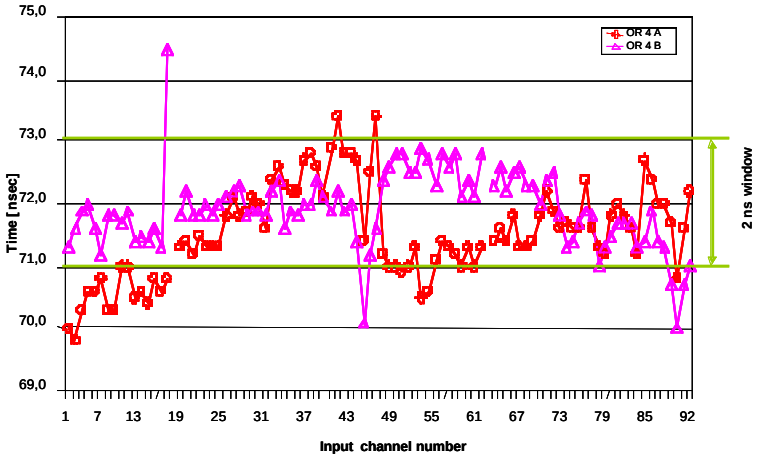

Figure 15: Output signal time skews (measurement)

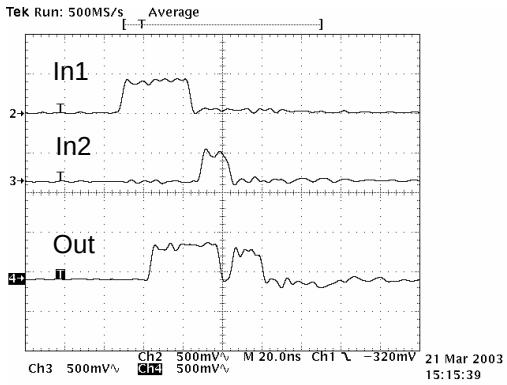

Figure 16: Input/output IB waveform

5. CONCLUSIONS

The IB system designed for the LHCb muon trigger has been presented. Optical Link geometries requiring the building of logic channels have been investigated and a solution to match detector topology readout with only one type of IB PCB and two types of TB PCB has been shown.

The results of the first prototype measurements show the system fulfils the project requirements. Anyway, though the components technology ensures a good behavior with respect to the total radiation (less than 2 krad) a test for radiation qualification must be foreseen.