



# LABORATORI NAZIONALI DI FRASCATI

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### **A low walk double threshold discriminator for gas tracking devices**

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#### **Abstract**

A 9U VME like double threshold discriminator has been designed and constructed at Frascati INFN laboratories. Its aim is to process the signals arising from gas drift chambers, introducing a very small time walk ( $\sim 650$  ps). Each discriminator board houses 32 channels. Each channel is located on an independent printed circuit mounted on socket. This solution is very convenient for replacing faulty channels without loosing operation of the full board.

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## 1 Introduction

To discriminate signals coming from gas drift detectors (i.e. drift chambers, straw tubes etc...), an original double threshold discriminating circuit has been designed and constructed at Frascati INFN laboratories. The main features of this circuit are:

- low time walk;
- high integration;
- analog signals splitting;
- majority capability.

These characteristics and the circuit performance are described in the following sections.

## 2 Circuit design

The design of any front-end circuit for particle physics detectors has to suit the characteristics of the input signals in order to obtain the desired performance. Nevertheless, the analog signals coming from gas drift chambers operated with argon based gas mixtures have similar characteristics: rise times  $t_r$  of about 10 ns; durations  $t_d \sim 100$  ns and amplitudes varying from a few mV up to some Volts. To achieve good spatial resolutions with such signals, it is necessary to measure drift times very precisely. This can be done only using discriminators that introduce a very small time walk.

The signals from a particle detector tracking system have a wide amplitude range. Therefore, it is impossible to have good timing performance simply by using leading-edge discriminators. On the other hand, although Constant Fraction Discriminators (CFD) introduce very small time uncertainties, they are quite expensive. A compromise can be found using Double Threshold Discriminators (DTD), which allow good timing resolution, but they are more simple and cheaper than CFDs.

The operating principle of a DTD circuit is very straightforward. The input signal is split in two parallel lines. On the first it is compared with a discriminating threshold; on the second, with a very low level threshold, slightly above the noise level, in order to have a trigger for the output stage that is fairly insensitive to the input amplitude variations.

Another requirement of particle physics detectors is to perform amplitude analysis of analog signals. To accomplish this task, a gain one amplifying circuit can be inserted directly into the discriminator board. On the front panel, it reproduces a copy of the analog input signal.

Finally, the signals of particle detectors can be used to implement trigger logics. For this purpose the discriminator board has been equipped with a current generator that gives an output level proportional to the number of fired channels. This output can be used to perform Majority operations.

The final layout of DTD circuit is shown in fig. 1. The input signal is split in two parallel lines: on the first one, it goes to an amplifying/adapting circuit that copies it for ADC analysis; on the second it enters

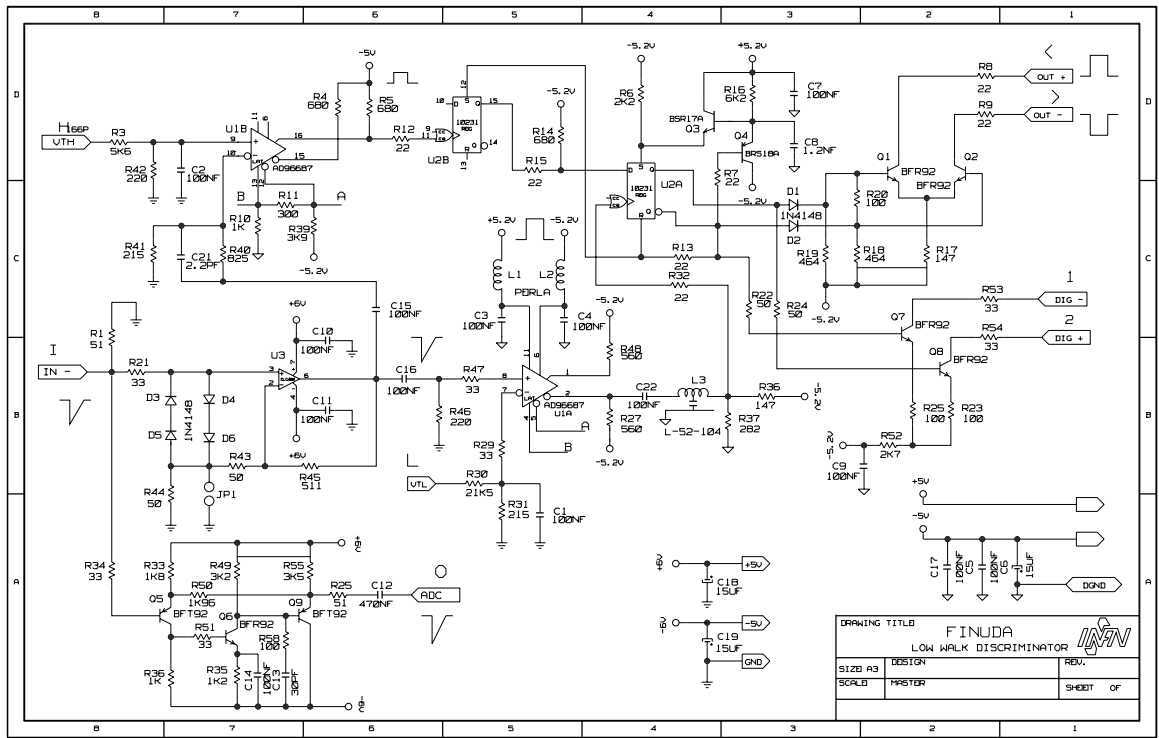


Figure 1: Layout of the Double Threshold Discriminator (DTD).

the discriminating logic. The first step of this logic is a limiting circuit that clamps signals with amplitudes greater than  $\sim 1.2$  V. This is necessary because sparks inside the chambers or other detector problems can produce signals with very high amplitudes. This signals can saturate the input stage of amplifier U3 (CLC404) producing a dead time of some  $\mu s$ . The purpose of this amplifier is to minimise the discriminator time walk. The AD 96687 ultrafast ECL comparator guarantees a propagation delay dispersion of 50 ps, only for signal amplitudes greater than 100 mV. Below this value, the intrinsic time walk increases, worsening the total circuit timing capability. The amplification of U3 has therefore been set to the value  $A = 5$  in order to make the Low Threshold Comparator (LTC) U1A work in the amplitude range where time uncertainty is minimum. Time dispersion minimisation is a very important goal for the LTC design because it has to give the trigger for output signal formation. On the other hand, this is not so important for the High Threshold Comparator (HTC) whose role is only to “validate” the delayed LTC signal. The output of the LTC U1A gives the clock pulse to the D-type flip-flop U2A (MC10231) after a 20 ns delay. This delay is to guarantees that the output signal starts after a fixed time with respect to the low threshold crossing, regardless of the HTC time walk due to the signal amplitude distribution and the HTC intrinsic time dispersion. If the high threshold is crossed, the HTC output signal sets the D input of U2A. When the delayed LTC signal reaches the U2A clock input, U2A datum is already set. Thus, the output signal is

produced and sent to the line-driver circuitry. The input signal to HTC is attenuated by a factor 5 by means of resistors R40 and R41. This is to compensate the amplification of U3 and restore the original signal amplitude.

The output stage of the discriminator circuit produces a differential current output that is sent to the following electronics. The solution of current drive differential outputs has been adopted to be able to drive very long cables ( $\sim 100$  m) to send discriminator output signals to the TDC modules. With differential current signals, it is possible to compensate pulses attenuation due to the line resistance, which can worsen timing resolution by slowing the signal leading edge.

In particle physics experiments, the number of analog signals to be discriminated can reach easily some thousand. Hence, it is necessary to have very compact circuits housing a great number of channels. For this reason, the 9U VME mechanics has been chosen. On one 9U board ( $360 \times 400$  mm) it is possible to house 32 DTDs. Nevertheless, high integration could result in a disadvantage when one channel breaks. In this case 32 channels have to be replaced. To solve this problem, each DTD is mounted on an individual printed circuit ( $75 \times 35$  mm) piggy-back on the “mother board”. To replace a fault channel, it suffices to change its circuit.

The “mother board” supplies to each DTD channel the voltages ( $\pm 5$  V;  $\pm 6$  V), and the threshold levels, and sums the analog current of each channel to produce a Majority linear output. It can also house interfaces for remote control the board. The first prototype of the “mother board” does not have any kind of VME interface.

### 3 Circuit performances

Figure 2 shows the circuit prototype constructed according to the design described in the previous section. This circuit was fully tested electronically using pulse generator signals to measure its timing response.

To evaluate the circuit time walk, a fast signal ( $t_r = 500$  ps) coming from a LeCroy [1] 9211 pulse generator was sent to the DTD. A global time walk of  $\sim 650$  ps was measured after setting the low DTD threshold to 3 mV and the high one to 40 mV and with input signal dynamics of  $40 \text{ mV} \div 250 \text{ mV}$ . The triangular points of fig. 3 show the results of these measurements. If the lower threshold is set to 10 mV, the total time walk increase a bit for signals of amplitude less than 60 mV (circular points). The same figure reports the results of the same test performed using a commercial (CAEN N96) leading edge discriminator (squared points). Here, the time walk is quite large when the input signal amplitudes are less than 70 mV.

A commercial version of the DTD circuit is presently used in the FINUDA experiment to process the signal from the straw tubes [6–8] and the drift chambers [4,5] detectors. FINUDA [2] is a  $\Lambda$ -hypernuclei experiment at the Frascati  $e^+e^- \phi$ -factory DAΦNE [3]. DTD design, with two threshold levels properly delayed, is very useful to reduce the time jitter arising from signals produced by particles crossing the drift cell near the anode wire. Since these signals show a “cluster train” shape which stretches the signal leading edge, it is necessary to properly choose the delay within the two thresholds. Wrong delay setting can produce efficiency reduction in the region around the wires [9].

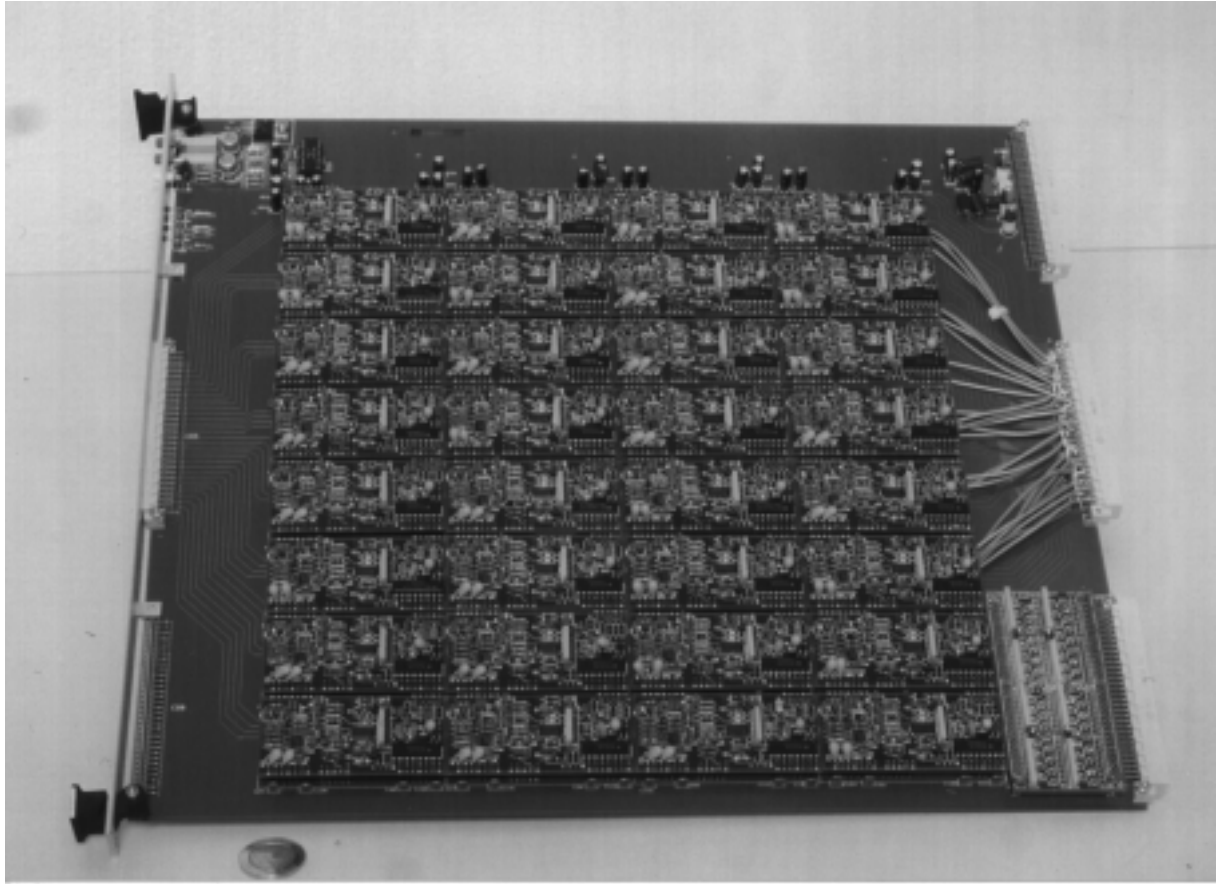


Figure 2: Layout of the board prototype housing DTD circuits.

Another test was performed on the circuit to evaluate how the current drive DTD outputs are dealt with the TDCs. The test consisted of two TDC measurements with and without a 70 m long cable connecting DTD and TDC. The results are shown in fig. 4. There are practically no differences in the TDC spectra with or without the long connecting cable.

#### 4 Conclusion

A new double threshold discriminator suitable for processing signals from gas drift detectors has been designed, constructed and tested at the Frascati INFN laboratories. Its main characteristics are: reduced time walk ( $\sim 650$  ps), high integration (32 channels on a 9U VME like board), easy repair of faulty channels and the possibility to drive long output cables thanks to differential current outputs. At present, a slightly modified version of this circuit commercially produced by CAEN Viareggio [10] is being used in the FINUDA experiment.

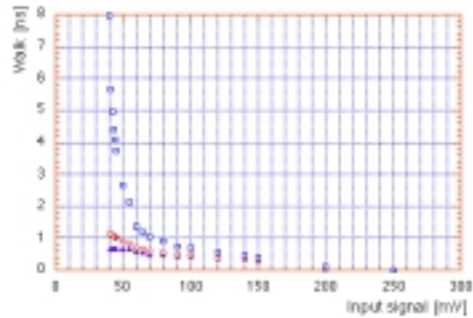


Figure 3: Measurement of the time walk of DTD with 2 different values of low threshold (triangles 3 mV) (circles 10 mV). The squares report the results of the same measurement done with a commercial discriminator, CAEN N96.

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