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MI.D.A.S.: a Forward Detector for the GDH Experiment at Mainz

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1 Introduction

MIDAS (MIcrostrip Detector Array System) is a compact telescope for charged particles in which the active layers consist of silicon detectors. It has been designed to extend the angular acceptance of the DAPHNE detector, previously used at MAMI to study photoreactions up to 800 MeV. The device will be used in the experimental program of the GDH collaboration to check the Gerasimov-Drell-Hearn sum rule.

MIDAS enables particle tracking and discrimination and energy measurement. The mechanics and the readout electronics have been realized by I.N.F.N. and University of Pavia. The software for acquisition tests, detector polarization and control has been developed using the Labview code. The detector resolution has been measured both by internal conversion electrons from a ^{137}Cs radioactive source and by m.i.p. from cosmic rays.

2 Detector Design

The DAPHNE detector [1] already meets most of the requirements for the experimental check of the GDH sum rule at Mainz [2]. However we considered important to extend the DAPHNE acceptance ($21° \leq \vartheta \leq 159°$; $0° \leq \varphi \leq 360°$) as close as possible to 4π sr in order to minimize the systematic errors in the cross section extrapolation.

Because of the severe constraints induced by the DAPHNE mechanical frame, two different devices have been realized. The MIDAS set-up [3] covers the intermediate forward region ($7.5° < \vartheta < 16.5°$), while a scintillator-lead device is placed externally to the DAPHNE frame covering the region $\vartheta < 5°$ [4].

Between the two devices a Čerenkov aerogel detector enables electron detection with a threshold of about 10 MeV and an efficiency >99%. Its signal is used as veto to suppress the electromagnetic background on-line.

The volume in front of the target and available for MIDAS is very limited. Therefore silicon detectors were chosen in order to obtain a compact device.

MIDAS includes two parts (fig. 1): a tracking section consisting of two double sided silicon detectors (V_1 and V_2) and a double silicon/lead sandwich (Q_1, Pb, Q_2, Pb, Q_3) for energy measurements.

The 5 detectors have a diameter of about 80 mm and a thickness of 1000 μm. A central hole let the primary γ beam go through.

The p-side of the tracking detectors is divided into 48 concentric rings, while the n-side is segmented into 16 radial sectors. The signals are carried out by a flexi-rigid cable consisting of 5 overlapping layers screened one to each other by a grounded wire-netting structure. The cable is terminated by 3 50-pins connectors and its measured capacitance is 222 pF/m.

The remaining detectors Q_1, Q_2 and Q_3 are single sided with the p-side segmented into 4 radial sectors (quadrants).

The silicon detectors were manufactured by Micron Semiconductor Ltd, UK. Their main geometrical parameters are listed in table 1.

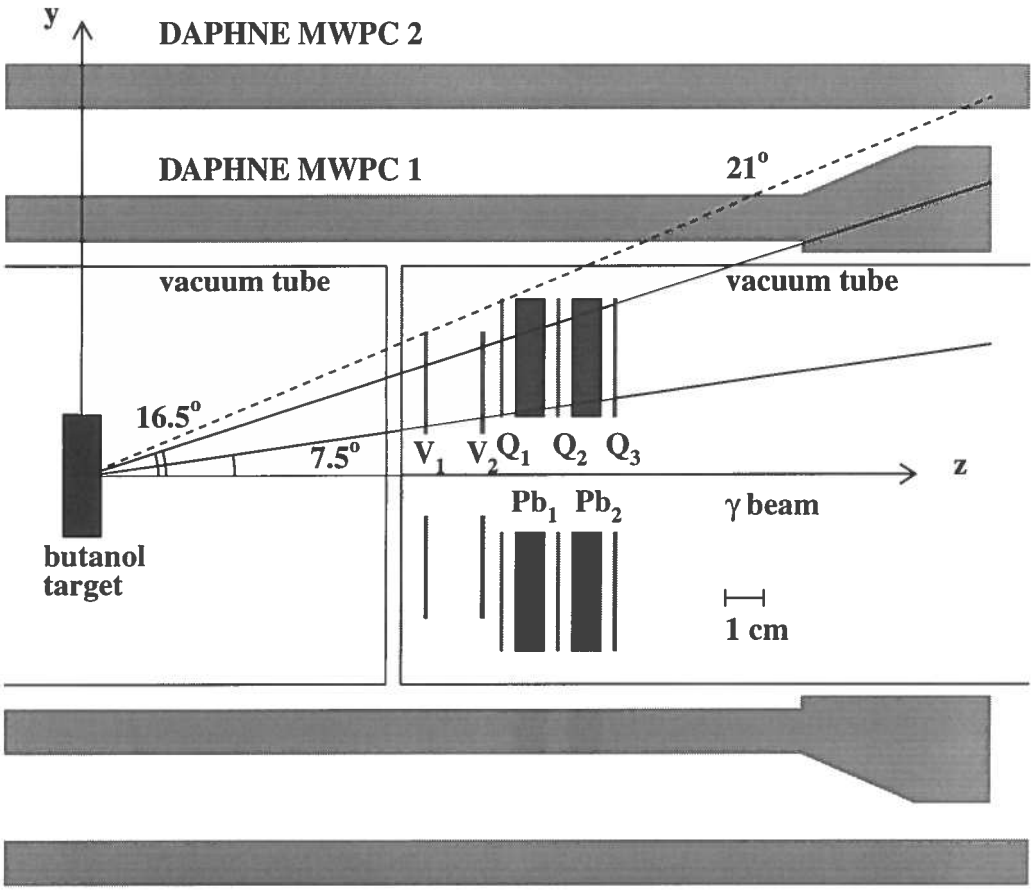

Figure 1: Side view of the device

The mechanics has been entirely designed and realized by the I.N.F.N. Pool of Pavia (fig. 2). The detectors and the lead absorbers are mounted inside an Aluminum tube fitting into the forward hole of the DAPHNE detector. The detector signal cables are distributed all around the inner surface of the tube. They are guided by a cylindrical basket and they exit from the back opening of the tube. Such a cable system lets the $\vartheta < 5°$ region free for the particle transmission towards the other forward devices.

The tube is closed at both ends by two Aluminum windows, $25\mu m$ thick. It is also provided with a gas inlet and a gas outlet to supply an Argon flow of few ℓ/hour. In such a way the detectors current is very stable and does not depend on the atmosphere

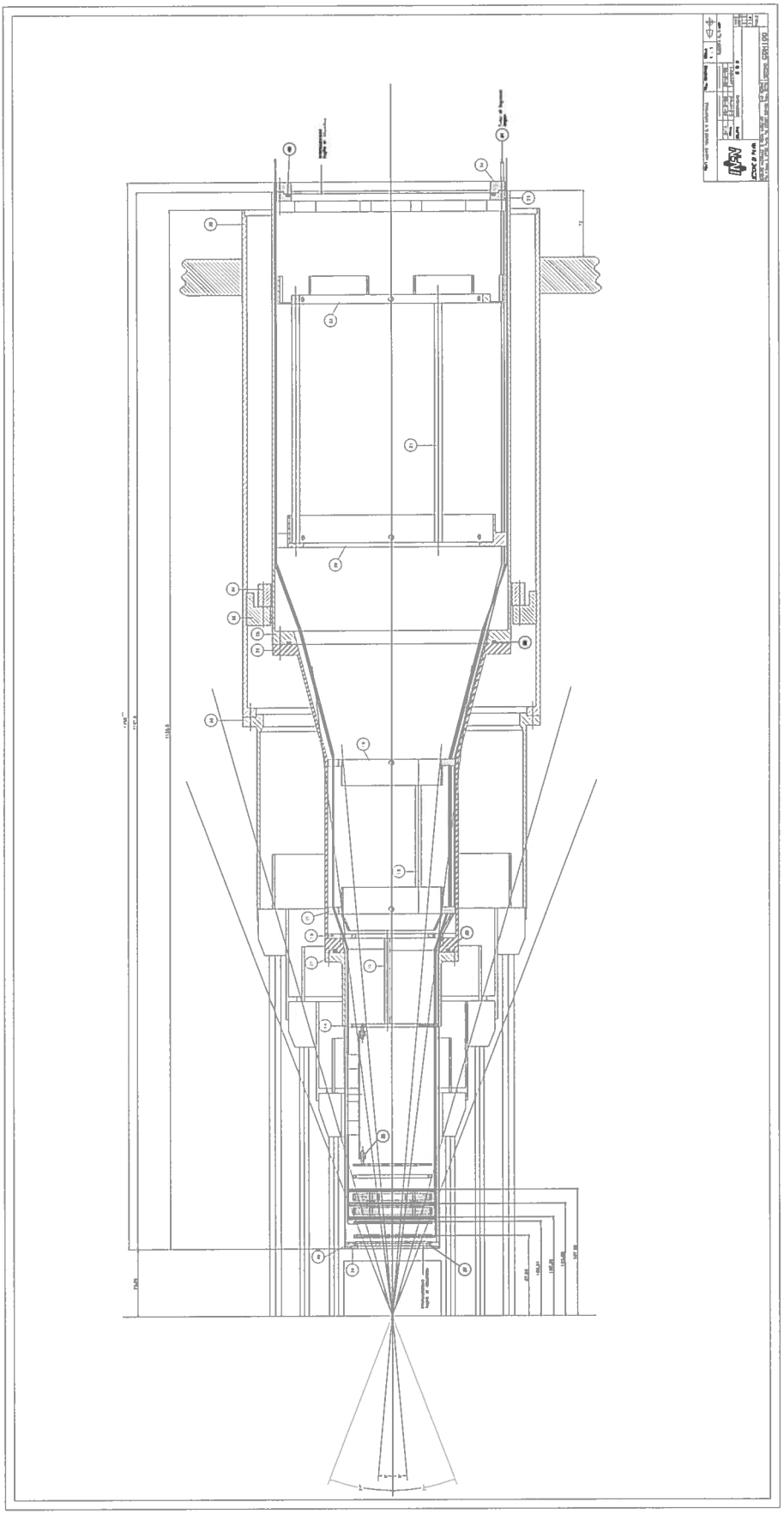

Figure 2: Layout of the MIDAS set-up

Table 1: Detector characteristics

	Tracking Detectors	**Quadrant Detectors**
Thickness	1000 μm	1000 μm
Geometry	Annular Ring	Annular Ring
inner radius	11 mm	14 mm
outer radius	35 mm	43 mm
Type	Double sided	Single sided
p side	48 rings	4 sectors
n side	16 sectors	-

impurities or humidity.

A rail system allows to insert the device into DAPHNE.

3 Principle of operations

The MIDAS device provides:

1. a trigger for charged hadrons;
2. the discrimination among e, $\pi^{\pm}$, and p;
3. the tracking for charged particles.

GEANT simulations were used to optimize the geometrical set-up by taking into account the experimental conditions at MAMI energy.

3.1 Triggering hadrons

Two trigger conditions have been realized to detect protons and pions, assuring the minimum background contamination.

According to simulation the most important source of background is due to electrons coming from pair production and Compton scattering processes occurring in the experimental target.

Therefore the double lead sandwich, whose total thickness corresponds to $\simeq$3 radiation lengths, has been designed to absorb most of the background.

On the contrary, almost all the pions and high energy protons are completely transmitted, giving a signal from all detectors. Therefore a good trigger for high energy hadrons has been obtained by the coincidence of the 3 quadrants detectors Q_1, Q_2, Q_3.

The low energy protons stopped inside MIDAS are triggered by the Q_1-Q_2 coincidence. These particles have a large energy loss rate, so the detection threshold can be set high enough to cut most of the electromagnetic background.

Simulations show that the above triggers allow to detect protons and pions with energy T>70 MeV and T>50 MeV respectively, while the electron background is suppressed with an efficiency of about 99%.

The remaining background mainly comes from pair production processes. In most of the cases only one of the two electrons enters MIDAS, while the other is emitted at a very low angle and then detected by the Čerenkov counter. Therefore this background can be eliminated requiring an anticoincidence between the Čerenkov signal and the MIDAS trigger.

With the previous configuration the experimental trigger rate due to background is estimated to be only $\simeq$0.5 times the pion count rate and mainly associated to Compton electrons.

These events can be discriminated off-line by the pulse height analysis.

3.2 Particle identification

At MAMI energy, the greatest part of photoproduced protons and pions are far from the relativistic regime and they can be discriminated using the dE/dx technique. Their energy loss rate can be measured by recording the pulse height of the detector signals.

The energy resolution of the silicon detectors has been measured by the internal conversion electrons from a collimated ^{137}Cs radioac-

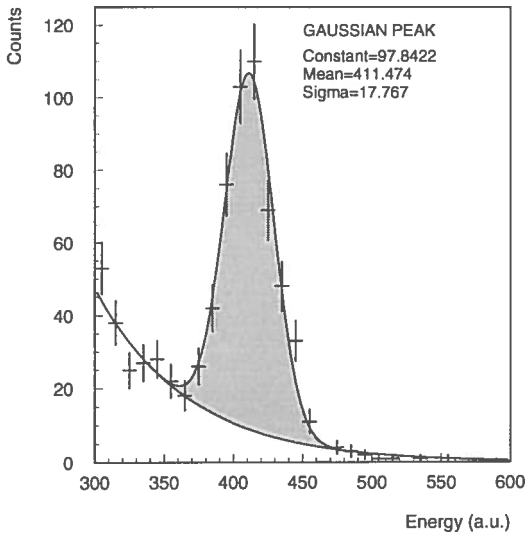

Figure 3: Detector resolution measured with the conversion peak of a ^{137}Cs source

tive source [3]. These electrons, having an energy of 661 KeV, are completely absorbed by a single 1000 μm thick detector, thus the detector response clearly shows the monoenergetic conversion peak (fig. 3). The energy resolution has been deduced from the width of the conversion peak. It is about 10% (FWHM), which is expected to give a good particle discrimination over most of the photon energy range.

3.3 Tracking

The particle tracking is performed by the V_1 and V_2 detectors. A charged particle passing through one of these detectors produces a signal from a single ring and a single sector.

The intersection between the hit ring and the hit sector determines the impact point of the particle on the detector. Then two detectors allow the complete reconstruction of the particle trajectory.

The polar and azimuthal emission angles resolution depends on the ring pitch and on the sector opening angle respectively.

Thus the detector geometrical parameters were chosen to have

the required resolutions which are expected to be $\sigma(\vartheta) \simeq 1°$ and $\sigma(\varphi) \simeq 10°$ according to simulation.

4 The Electronic Chain

The readout electronics is based on preamplifiers and Fastbus modules described in ref. [5] and ref. [6]. These modules receive the differential signals from preamplifiers and provide the shaping, the track & hold, the multiplexing and the 12-bit digitization of the signals.

The original design of these modules (FEMC) was modified by the Electronic Pool of INFN Pavia [7]. A trigger section with a double threshold discriminator was added and the original optical transmitter for the readout was replaced by a Latch circuit.

Data are sent to an interface which contains the control logic and is directly fed to the VME CPU DSP56 that is used for acquisition.

In fig. 4 the block diagram of the readout electronics is shown.

4.1 Preamplifiers

The hybrid preamplifiers are mounted on boards carrying 27 channels at maximum.

These boards provide for the detectors voltage supply. They are referred to a positive voltage for cathodes (n side) and to ground for anodes (p side).

In fig. 5 the schematics of a single preamplifier channel is shown. The original design was slightly modified in order to increase the input capacitance and the linear range. The input stage consists of a FET with capacitance C_{in}=35 pF. The differential output has a dynamic range of ±400 mV and a gain of 1 mV/fC. The equivalent noise charge (ENC) is 230 e^- measured with no input capacitance.

In fig. 6 the output signals of the preamplifier are shown.

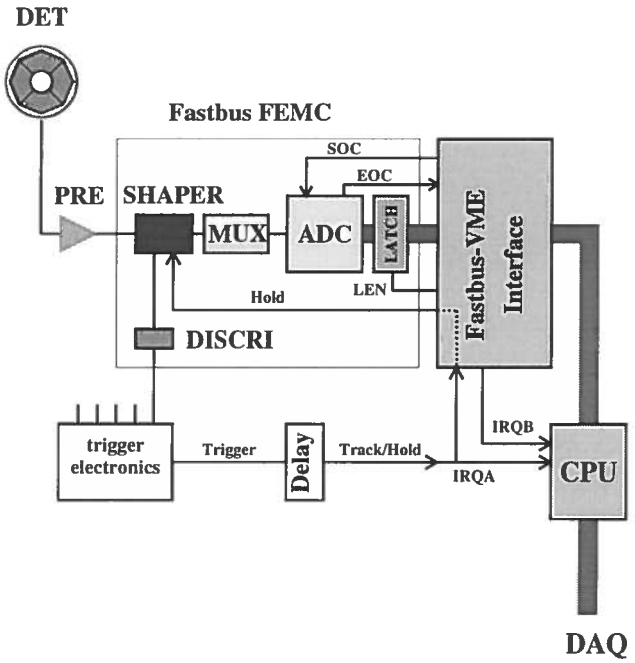

Figure 4: Electronic chain

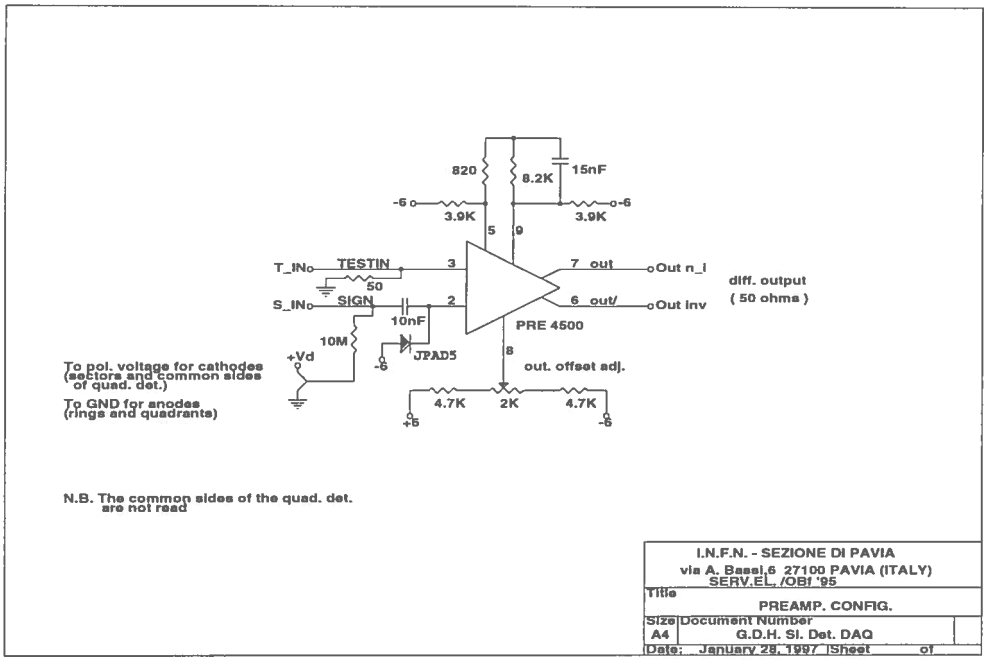

Figure 5: Preamplifier scheme

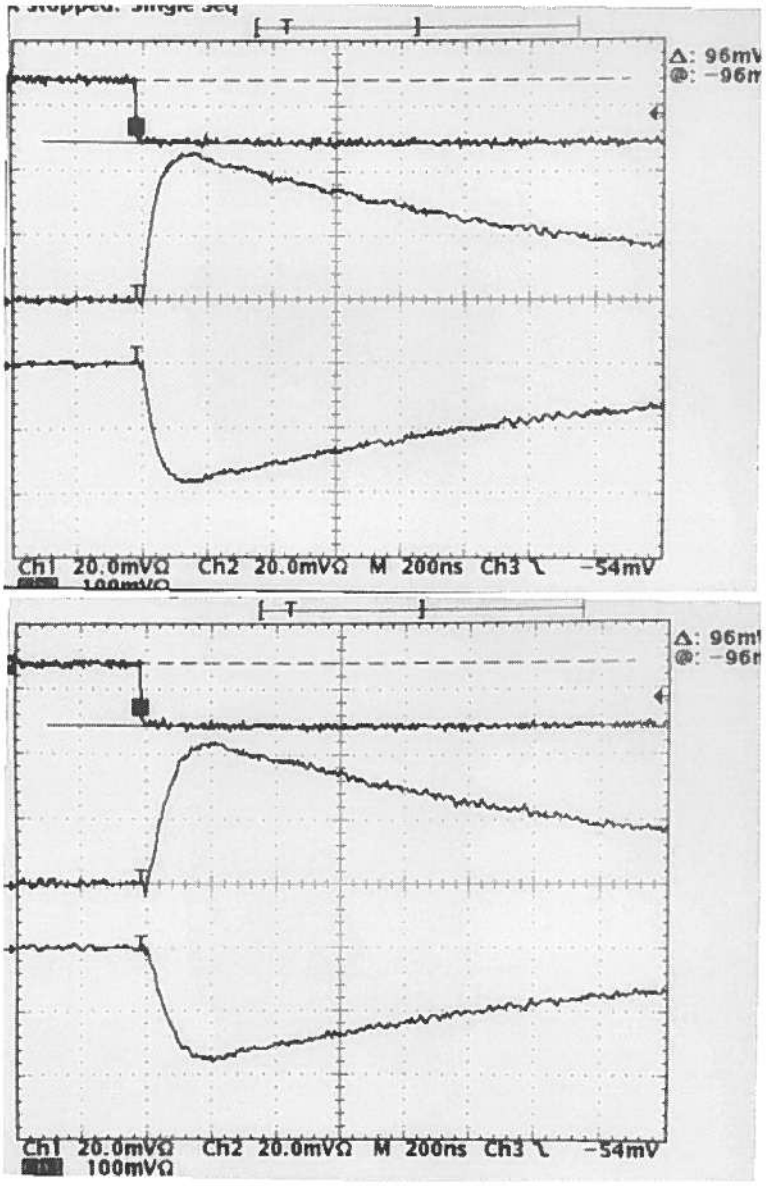

Figure 6: Preamplifier differential output. A step pulse is injected into the test input of the preamplifier. The output of the preamplifier is shown without (up) and with (down) the detector capacitance.

4.2 FEMC modules

There are four FEMC Fastbus modules used in the electronics set-up. Each module implements 80 channels divided into 5 groups (rows). Each channel is equipped with a hybrid shaper, consisting of a $(RC)^2CR$ filter. It is followed by a hold circuit allowing the 80 signals to be multiplexed and serially digitized by a single 12-bit ADC DATEL 810 with 2 μs conversion time. In fig. 7 the block diagram of the shaper is shown.

An auto-trigger line has been obtained by taking out the signal from the first stage of each shaper (pin #5). This signal is sent to an on-board discriminator (fig. 8) with a double circuit allowing to set two different threshold levels: a High Level Threshold (HLT) and a Low Level Threshold (LLT).

The output signals of each row of shapers (16 channels) are OR-ed to generate a HLT trigger and a LLT trigger. The delay of the auto-trigger with respect to a signal injected into the test line of the preamplifier is 160 ns.

The auto-trigger signals are combined into external modules to provide two experimental triggers, one for low energy protons and one for pions and high energy protons. These triggers also generate the track & hold signal.

Fig. 9 shows the output of the first stage of the shaper (up) which is differentiated (down) and sent to the discriminator.

The output signal of the shaper is bipolar (fig. 10) with the following characteristics:

- peak at 1.4 μs;
- total amplification $\times$ 16;
- total time 20μs.

The arrival of an experimental trigger makes the hold active and the signal is stored for conversion (fig. 11).

The hold must start in correspondence to the signal maximum amplitude, so a Timing Unit is used to generate the proper delay to the experimental trigger.

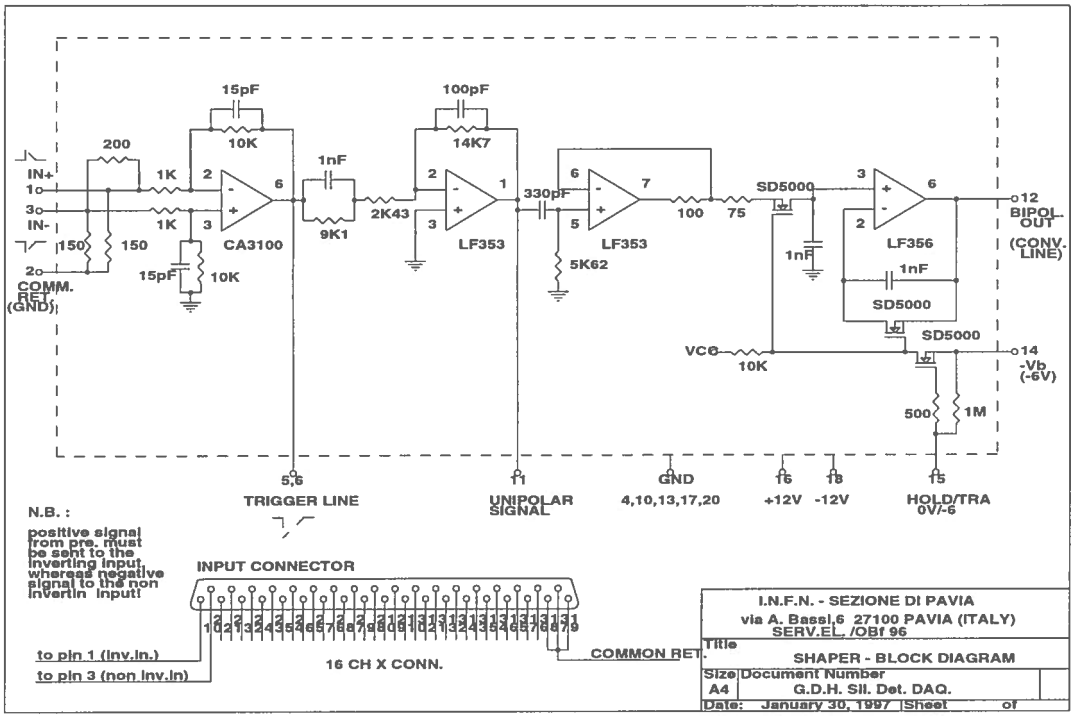

Figure 7: Block diagram of the shaper

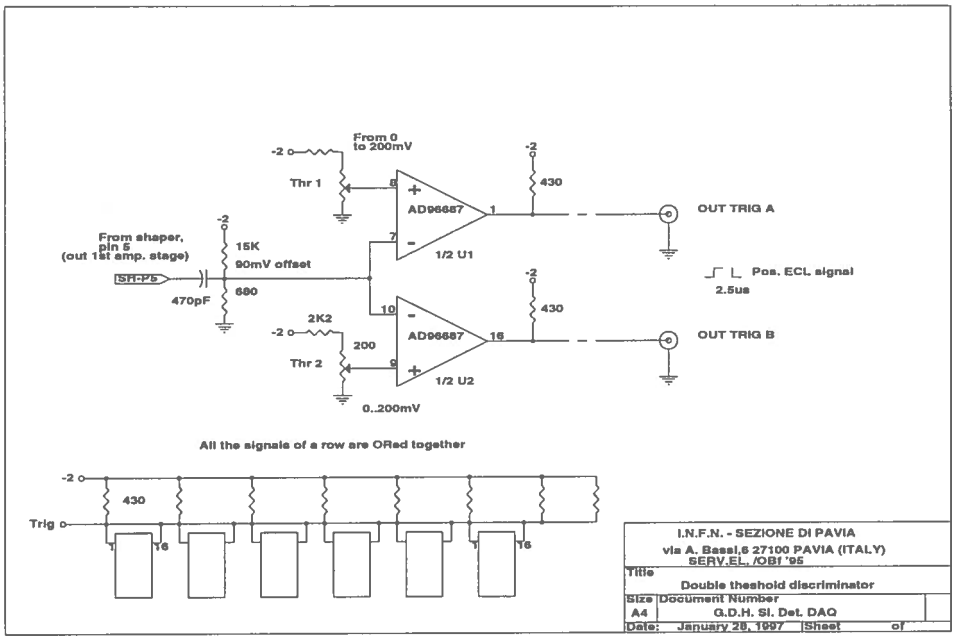

Figure 8: Double threshold discriminator

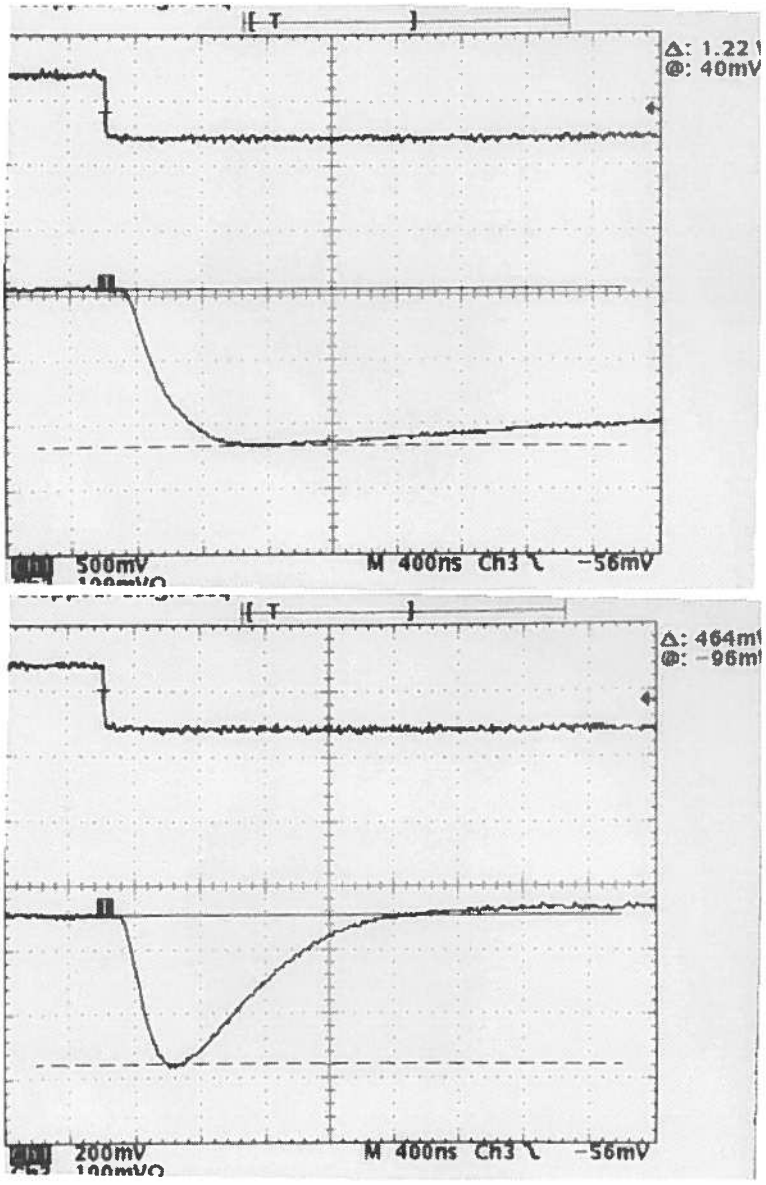

Figure 9: A step pulse is injected directly into the shaper input. Up: output signal from the pin #5 of the shaper. Down: output signal after the differential CR stage of the discriminator.

4.3 The Latch

The Latch circuit [7] replaces the optical transmitter of the FEMC module allowing the VME acquisition.

It consists of two 74FCT533 latches. The Fastbus modules are equipped with a 12-bit ADC, thus the readout is made for a pair of modules at a time, in such a way that all the 24 bits/word of the CPU DSP56 are filled: the 12-bit data of the first module fill the low significant bits (LSB) and the 12-bit data of the second module fill the most significant bits (MSB). This is obtained by doubling the latch system.

4.4 The Trigger Electronics

The signals from the detectors are arranged in the FEMC input to obtain separate auto-triggers for the 3 quadrant detectors. In total there are 6 auto-trigger signals, 2 for each detector, one obtained with LLT and the other with HLT.

The LLT is set to the minimum value compatible with the electronic noise and it allows to trigger m.i.p. signals. The HLT is about 2 times the mean m.i.p. signal amplitude, which corresponds to the minimum energy released by protons going at least through the Q_2 detector.

The auto-trigger outputs from the FEMC modules are combined into external VME modules to provide the experimental triggers. The VME modules receive as input the ECL signals from the auto-trigger section of the FEMC module, providing NIM translation and the required logical coincidences.

Two triggers have been implemented: one for pions and high energy protons (T_1); the other for low energy protons (T_2).

The pion T_1 trigger is realized by the triple LLT coincidence between the 3 quadrant detectors Q_1, Q_2 and Q_3. The T_2 trigger is obtained by the double coincidence between the quadrant detectors Q_1 and Q_2, using the HLT.

The readout and acquisition is started by one of the two experimental triggers (ORed).

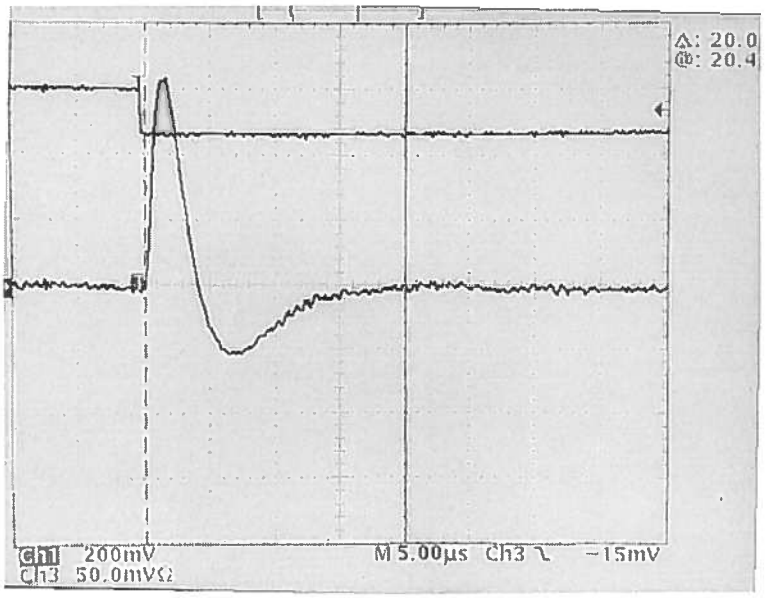

Figure 10: The output signal obtained from the hybrid shaper (pin #12).

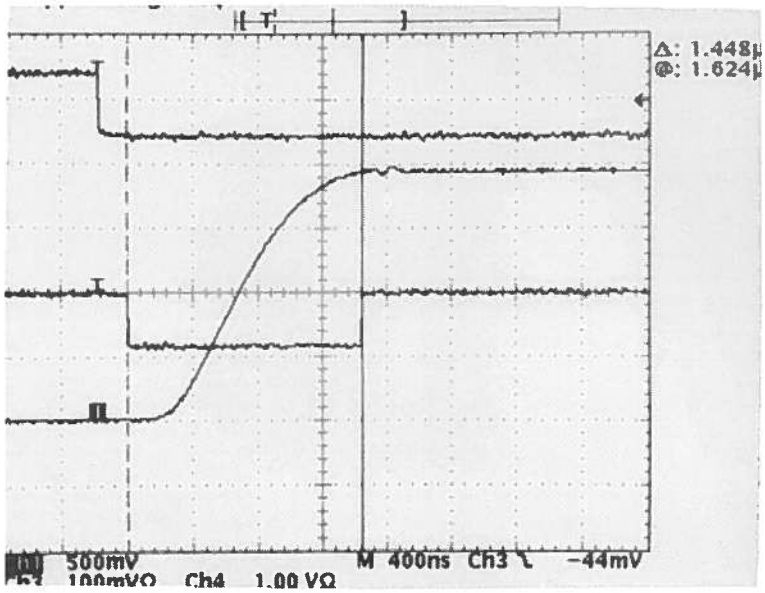

Figure 11: The signal stored by the hold circuit. Signals can be stored up to 3 ms with negligible attenuation

4.5 The Fastbus interface

The digitization/acquisition cycle starts when the interface receives a trigger. The same trigger is sent to the IRQA interrupt of the CPU. Therefore the acquisition program generates a clock signal which allows to select the channel to be converted and to start the conversion.

When the ADC conversion is finished, an End-Of-Conversion signal is sent to the second CPU interrupt (IRQB) and the acquisition program generates the clock signal for the following selection.

The initialization of all multiplexers requires 5.5 μs; the selection of the channel 2.14 μs; the conversion readout 3.18 μs.

The channels to be converted are selected in a given order which does not follow their natural numbering.

5 Data Acquisition

The acquisition is performed with a CPU DSP56001 [8]-[9]. The DSP56 runs a data acquisition program to read and decode the Fastbus ADC's. These data are stored by the DSP in a circular buffer and they have to be transferred to the host computer for the storage.

5.1 The CPU DSP56

The DSP has a 24-bit data bus with 3×64KW memory zones: one for the programs (P) and two for the data (X and Y).

The interface between the CPU and the VME is made by means of a VIC068 (Cypress).

The DSP has a RS232 port and a Host 8-bit parallel port. The Host Port is directly interfaced to VME through memory mapping. It consists of two banks of registers: one bank accessible to the host computer and a second bank accessible to the DSP CPU. All the registers are 8-bits wide.

The acquisition program for the DSP is written in macro-assembly 56000. It allows the readout with pedestal suppression. The peak

and the width of each pedestal distribution have to be previously determined and loaded in memory. Only channels having an amplitude greater than the specified values are stored into the DSP memory.

The acquisition program can be loaded through the RS232 port. Users can interact with the DSP by means of a monitor program (DSPbug) [8].

5.2 Event Transfer

Data transfer from the DSP memory to the host computer can be performed in two different ways: via the VME bus and via the Host Port of the DSP.

The first method is the fastest one and it is used in the experimental data taking. There is a master VME CPU performing the readout of different sections of the GDH experimental apparatus [2]. This CPU directly accesses the DSP memory. The VME addresses of the DSP memory are obtained by multiplying by 4 the DSP internal addresses.

The second method requires a handshake protocol using the Host Port registers [9]. It has been adopted to test the MIDAS device independently from the rest of the experimental apparatus.

The data transfer software has been realized using the Labview code [10] installed on a QUADRA 900 computer. The data transfer loop is only controlled by two flags, HF2 and RXDF (Receive Data Register Full). When the DSP is ready for data transfer (HF2), the host tests the RXDF flag which is set to 1 when the DSP has filled the 3 8-bits Receive Data Registers.

A control of the number of word to be read is not implemented: the event transfer ends when both HF2 and RXDF are set to 0. A final test on RXDF is performed to ensure that the last word of the event has been transferred.

The program disables the IRQA interrupt during all the acquisition cycle. In such a way the program does not accept new triggers arriving while the data transfer of the previous event is in progress.

6 Detector Polarization

The silicon detectors are polarized by a CAEN SY527 system. It consists of a 19" wide crate, fitting several kind of low and high voltage boards. The same system also provides the low voltage for the preamplifiers.

The SY527 is remotely controlled via VME. The software to control the detector polarization has been realized using the Labview code. It is able to detect current overloads; in this case it reacts decreasing the polarization voltage to protect the silicon detectors against breakdown.

The software also provides the current and voltage monitor.

Acknoledgements

We acknowledge the careful work of the INFN workshop in the realization and assembling of the MIDAS set-up. In particular we are indebted with V. Arena, G. Bestiani, E.G. Bonaschi, D. Calabrò, A. Freddi, G. Iuvino, P. Ventura, F. Vercellati.

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