ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Napoli

INFN/TC-97/09
21 Marzo 1997

F. Fabozzi, P. Parascandolo:

DESIGN OF A HIGH THROUGHPUT FIFO BOARD

SIS-Pubblicazioni
dei Laboratori Nazionali di Frascati

INFN – Istituto Nazionale di Fisica Nucleare
Sezione di Napoli

INFN/TC–97/06
21 Marzo 1997

DESIGN OF A HIGH THROUGHPUT FIFO BOARD

F. Fabozzi, P. Parascandolo
INFN – Sezione di Napoli, Mostra d'Oltremare, Pad. 20, I – 80125 Napoli, Italy

Abstract

The design of a 60 MHz pattern decoder and a 64 bit wide FIFO data bank poses some unusual challenges to the digital designer since analog effects become of paramount importance to assure signal integrity.

1. INTRODUCTION

The IFR subdetector of the BaBar experiment [1–2] is based on Resistive Plate Chamber (RPC) [3] planes employing a large number of strips (about 50 K) which must be extensively buffered while making trigger decision. A front end card (FEC) [4–5], acting both as discriminator and buffer of data, mounted on the detector and serving 16 channels has been produced (more than 3K cards). From this point the Data, on the occurrence of a trigger, will be first loaded into a parallel in serial out shift register and then transmitted to 52 FIFO boards (IFB) located into 8 crates close to the apparatus which will provide for data buffering. The IFB module is necessary since, although the average acquisition frequency foreseen at BaBar is of just 2 KHz, maximum frequency peaks of 0.4 MHz could be possible.

Data acquired by IFBs will be transmitted to the central Data Acquisition system (DAQ).

The BaBar collaboration has chosen to multiplex a whole crate readout section into a single high speed transmission line going to standard DAQ Read Out Modules (ROM) common for all the sub–detectors and located in the Electronic House (EH). The approved solution for the transmission line consists of a fiber optic transmission system at a speed of 1.2 GHz (CLINK & DLINK). The fiber optic system serves both to acquire data from the detector to the DAQ (DLINK) and to transmit clock (59.5 MHz), trigger and control signals to the IFR sub–system crates

(CLINK). Commands (12 bit) and test data (64 bit) reach the IFB module via Din line; Data are output serially via Dout line.

A block diagram of the IFR electronics is depicted in Fig. 1.

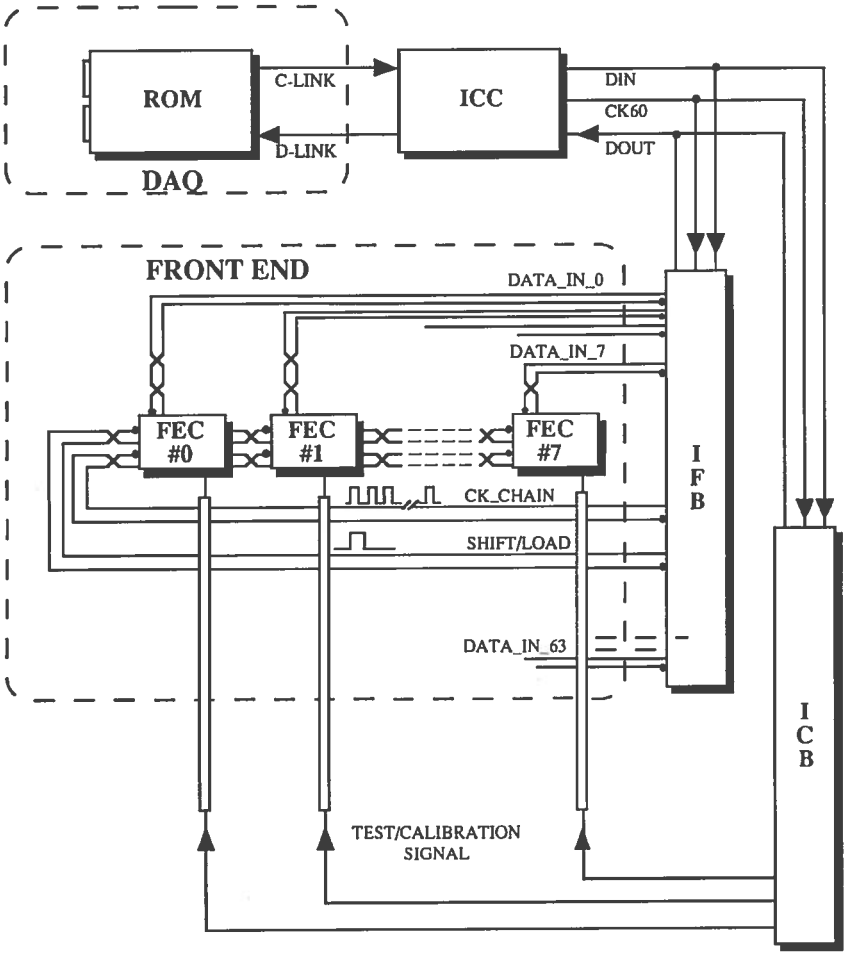

Fig. 1 – Overview of IFR electronics

2. IFB BLOCK DIAGRAM

Each IFB serves 64 FEC channels acting as an acquisition master. In the occurrence of a trigger (L1 Trigger Accept) strip status (hit or not), properly stretched by the front end electronics, is first loaded into a pipeline register bank and then transferred into the IFB's FIFO bank (Fig. 2). To perform this function IFB produces a 16 pulse train CK_CHAIN plus a SHIFT/LOAD signal to the FECs, and synchronously stores incoming data. The first CK_CHAIN pulse loads strip status onto the FEC parallel in serial out shift register, furnishing at the serial output strip No. 15, while the following CK_CHAIN pulses – with the SHIFT/LOAD signal set to low – transmit strip No. 14 and so on until strip No. 0.

As the clock frequency for BaBar subdetectors electronics is fixed at 59.5 MHz, we have derived the CK_CHAIN clock frequency by this one dividing it by four, so that data transmission frequency from FEC to IFB is fixed at about 15 Mhz.

In addition to the sixteen 64 bit words indicating the strips content, for each L1 Trigger Accept a Header and a Trailer are added for a total of 18 words (Fig. 3).

Only 32 bit of the Header are significant, the other being just zeroes (Fig. 4).

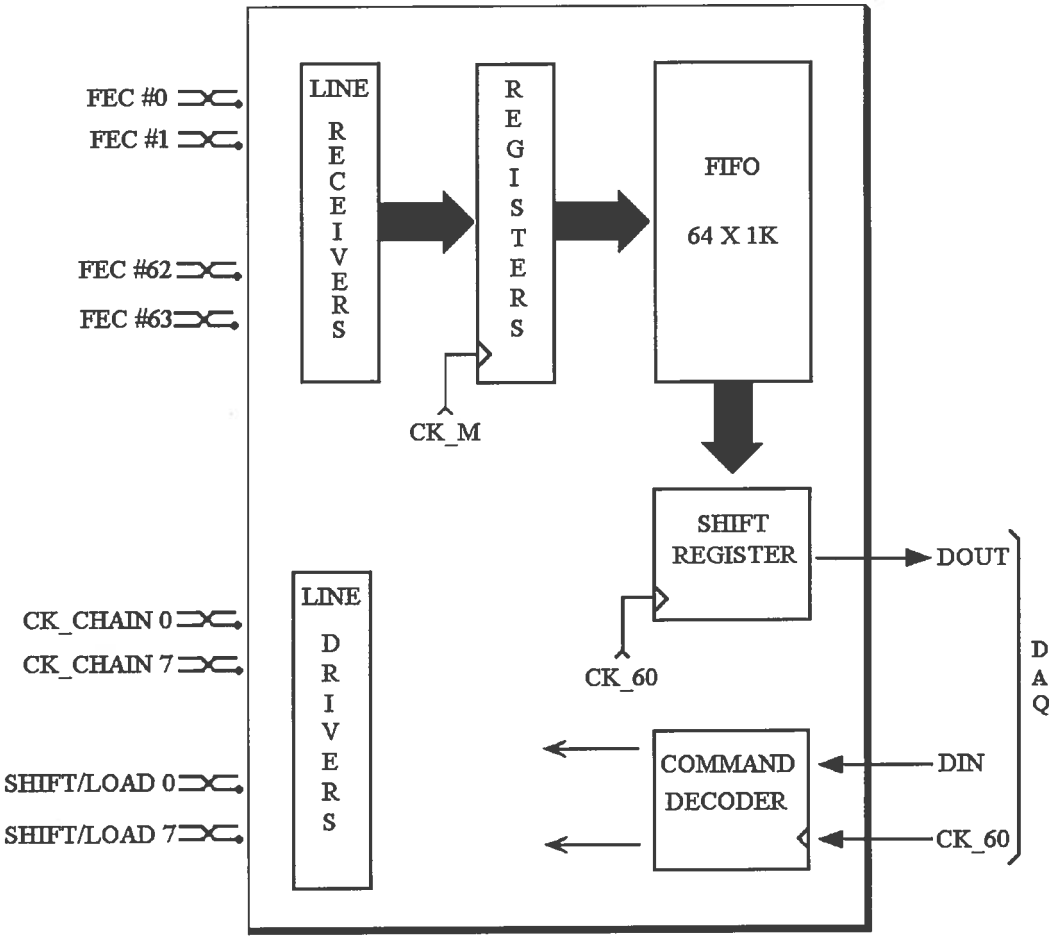

Fig. 2 – IFB block diagram.

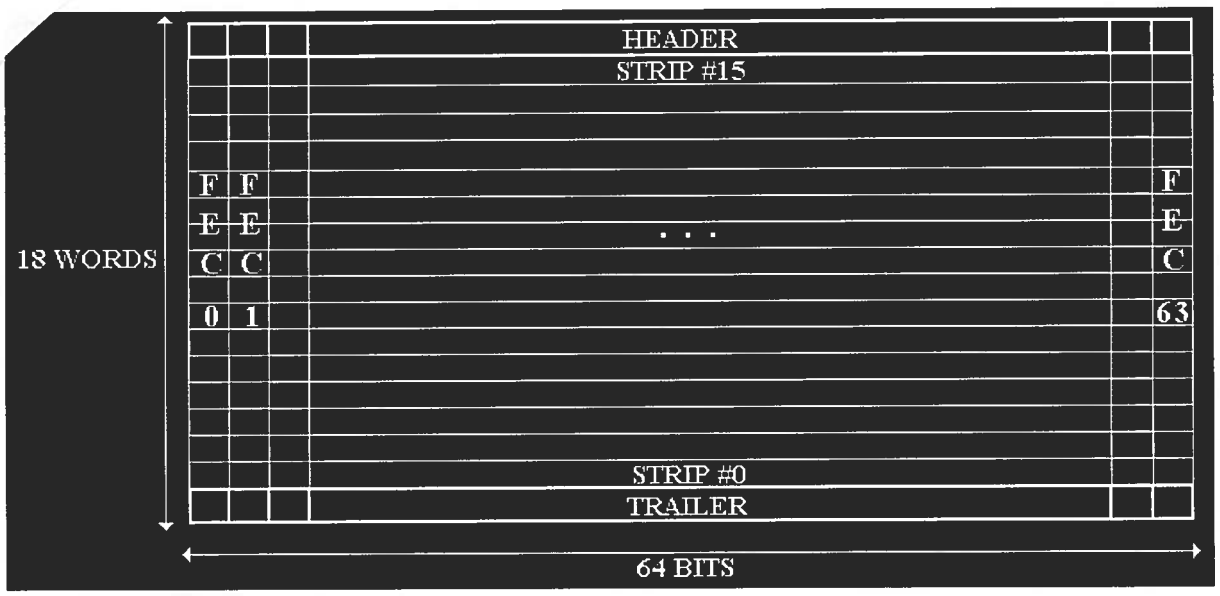

Fig. 3 – Data frame associated to an L1 Trigger Accept.

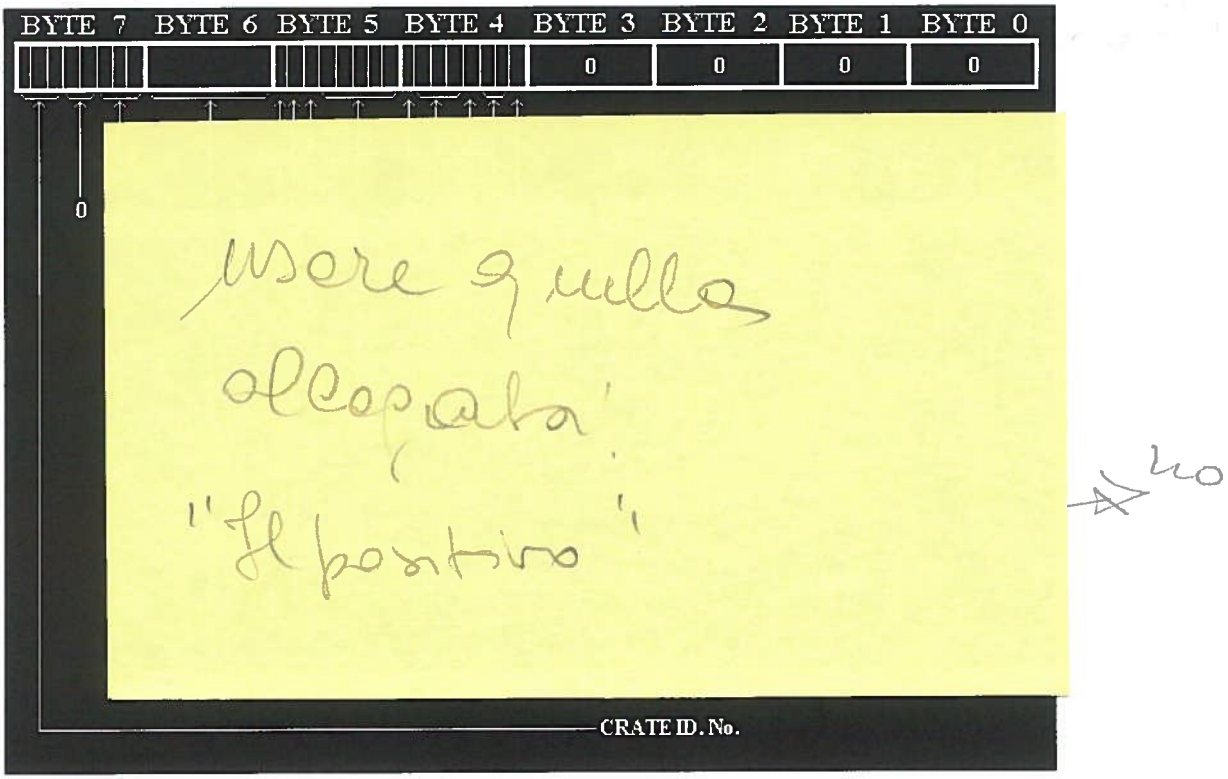

Fig. 4 – Header format

The "Trigger Tag" is a label that DAQ attaches to every L1 Trigger Accept and is sent together with the command itself. The 8 "Time Stamp" bits refer to a counter which is present on each IFB module and provides the time occurrence of the trigger. The time stamp counter is clocked by the 59.5 MHz clock common for the whole experiment. In the idle state the Data bit of the GLINK is stuck at zero while the 59.5 MHz clock continues to run. That way the "Time Stamp" counters present on the IFB and on each sub–detector keep up counting so that stay synchronous each other also when the GLINK is idle.

A Trailer, made up by 32 "ones", closes the event.

Commands and data are fed to the IFB via DIN input. The only output of the module is the DOUT line. The format of the Run–time commands is the following:

z s c c c c c d d d d d
z ==> 0
s ==> 1
c ==> command bits, LSB first
d ==> data bits, LSB first

Non–run time commands have the format indicated below:

z s c c c c c a a a a a d d d
z ==> 0
s ==> 1
c ==> command bits, LSB first
a ==> sub–address bits, LSB first
d ==> data bits, LSB first

For a detailed description of the commands format and requirements imposed on the receiving and on the transmitting section of the IFB refer to the BaBar internal note No. 281 [6].

On each module a fixed pattern detector (Cmddec PLD) compares the serial bit stream against a predetermined pattern producing different check signals for each allowed pattern. Cmddec produces the following commands: NOP, Clear Readout, Sync, L1 Trigger Accept, FC, Read Event, WRF, RDF.

NOP – code 0 – is a no–operation code. No operation is required onto the module but the command has to be decoded and a flag to be written onto the FIFO with the next header must be set.

Clear Readout – code 1 – performs a reset operation of the FIFOs pointers. That way the FIFO empty flag becomes active. This command is issued at the very beginning of the Data Acquisition or it is sent to restart acquisition after a catastrophic event.

Sync – code 2 – is used to reset the time counters of the module (for the IFB the "Time Stamp" counter referred to above).

L1 Trigger Accept – code 3 – starts Data Acquisition from the front end. Each time this command is issued, the strips status present on the detector 12 microseconds before is latched onto the front end cards (FECs) and is transferred serially to the IFB. In order to distinguish between successive triggers a Header (32 bit) and a Trailer (32 bit) must be added, so that, for each L1 Trigger Accept a total of eighteen write operations into the FIFO are requested. Since a FEC serves 16 channels, the DAQ, for each trigger issued, must read a total of 1152 bits from each IFB module. The data bits of the L1 Trigger Accept command constitute the "Trigger Tag" which is just a label to enable the DAQ system to distinguish between trigger frames. Once an L1 command is detected, data from FECs are acquired by sending CK_CHAIN to the front end and pipelining the data into the pipeline register bank (8×74F374) whose clock is CK_M. This clock is produced with a "built in" delay of 128 nsec. from CK_CHAIN, to take into account the cable length which will be fixed at about 8 meters. Data are written onto the FIFO by the CK_WR_F signal, which is produced not only to load data from FECs (16 + 2 pulses) but also to store a test pattern word into the FIFO (just one pulse in this case). The test pattern is loaded into Wrf0 & Wrf1 PLDs by a WRF command.

Read Event – code 4 – is used to start transmission of data held into the FIFO buffer to the DAQ. Data from the FIFO are first loaded into a shift register and then they are shifted out serially at 59.5 MHz with the LSB first. This action is controlled by the Rdctr PLD which provides both the right Read FIFO signals and the load signal to the Shift PLD, which performs the necessary parallel to serial conversion.

False Command – code XX –. Each time there is no match between the serial input and the internal fixed pattern, the IFB sets a flag of False Command indicating a reception of a wrong pattern or a failure in the command decoding process. This flag is stored and written onto the FIFO with the next header.

As outlined before, to test proper operation of the IFB card, the DAQ can send a WRF command – code 1A – to write a 64 bit pattern onto the FIFO and read back it via an RDF command (code 17).

We have chosen to implement the logical functions required by the IFB design into more MACH210A–7 PLDs, manufactured by AMD [7]. Seven chips are employed either to decode the commands (Cmddec), to assure diagnostic operation on the board (Wrf0 & Wrf1), to implement the time stamp counter (Ts_wrf), to assure reading from FIFO and data transmission to DAQ (Rdctr & Shift) and to manage the interface versus the front end (Fec_fif).

For the IFB module faithful operations up to a clock period of 14 nsec. are requested.

This requirement can be achieved since a close look at the MACH210 PLD's manufacturer catalog reveals that this component is specified to have a set up time t_s from input, IO or feedback to

clock of 5.5 nsec., whenever the input register is D_type, while the clock to output delay t_{co} is 5 nsec. With regard to the clock distribution network, we have opted for a point to point architecture using a CDC391 clock driver [8].

At present a first prototypes series is under test and preliminary results are satisfying as the board is operating up to a 12 nsec. clock period, well beyond the 14 nsec. requested period.

3. FEC – IFB INTERFACE

The choice of the interface standard between the FECs and IFB requires a close analysis of the various factors which influence data transmission. The utmost item regards the line length versus data rate trade–off while noise immunity and radiated noise are also to be analyzed carefully. A single ended transmission presents some obvious advantages, being simple to implement and requiring just one wire per signal, but its bandwidth is limited to the tenth of KHz., whereas a differential transmission allows a transmission frequency in the order of the tenth of MHz, much longer line length and, as twisted pairs are used with currents flowing in opposite directions, produces less noise. Further, since the receiver is differential, data transmission is much less sensible to ground shifts.

We have opted for a differential ECL standard (Fig. 5).

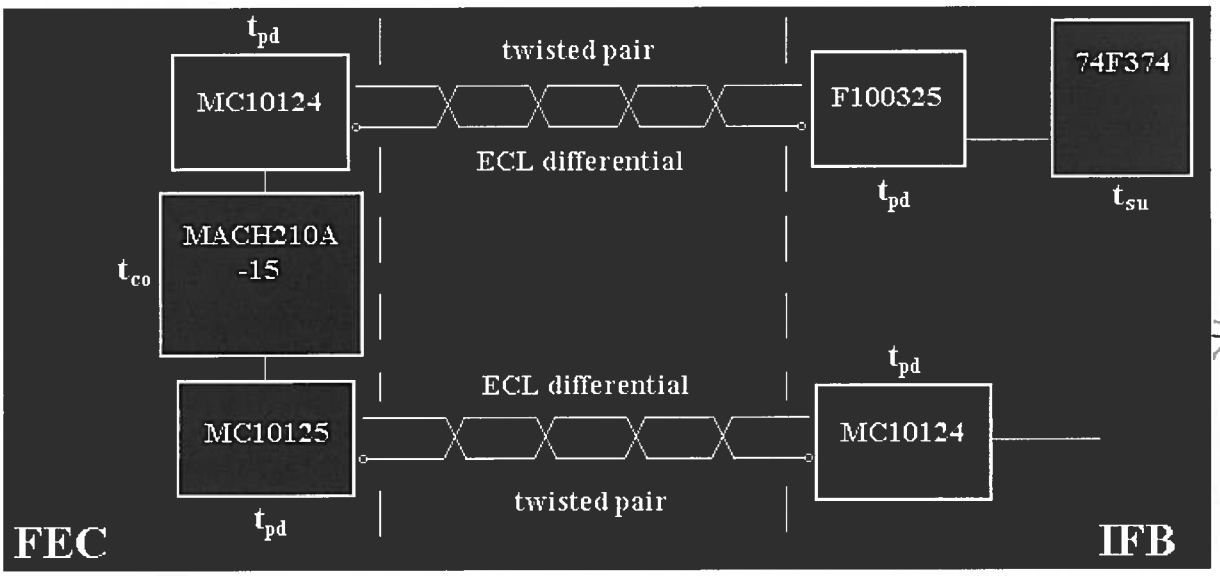

Fig. 5 – FEC–IFB interface standard.

To work safely at a frequency of 15 MHz – whatever cable length may be – the following relation must hold true:

$$4 \times t_{pd} + t_{co} + t_s < 64 \text{ nsec.}$$

With ECL line drivers and receivers 13 nsec. are left for safety margins – since for MC10124/125 t_{pd} = 6 nsec., while t_{co} = 15 nsec. for the MACH210, and t_s = 2 nsec. for the 74F374. Using TTL components for line drivers/receivers, such as ALS192/ALS193, we could not achieve this frequency of operation since the propagation time of TTL parts is 14 nsec. worst case. As an added benefit of ECL, since the voltage swing is of just 0.8 V, radiated noise is very low. In fact the noise measured at 10 cm from the twisted pair goes down and so there is no need to shield cables.

In the IFB design we have opted for the F100325 line receiver, which is pin compatible with the F100125 but features a power dissipation of a roughly half value. As an added benefit versus MC10125 line receivers, we gain two receivers more into the same package. Interface with the MC10124 present onto the FEC – being done differentially – causes no problem.

4. THE DYNAMIC PATTERN DETECTOR (Cmddec)

The design of the dynamic pattern detector has been described in great detail elsewhere [9]. Besides the commands, two time critical signals lasting just one cycle are also produced: LDS and NSYNC. The former is produced at the end of an L1 command both to load the "Trigger Tag" into an internal pipeline register and to latch the external "Time Stamp" counter into an 8 bit pipeline register; the latter is produced likewise at the end of a SYNC command to reset the "Time Stamp" counter.

Transfer takes place synchronously whenever LDS signal is low. LDS generation is therefore time critical and the relative equation cannot be combinatorial. To assure reliable operation the time t_{co} (delay clock to output) plus t_s (set up time from input, IO or feedback to clock) plus PCB delay (in case of "time stamp") must be well under our design goal (14 nsec).

For the NSYNC output (active low) the same rules as outlined for LDS signal are applicable.

To assure good timing performance only D–type registers are to be employed in this PLD as they have just a 5.5 nsec. setup time from input, IO or feedback to clock. Obviously this minimum setup time must be assured in the relative timing between the DIN input and the 59.5 MHz clock (CK60).

In the following graphs we show how, with a 5.5 nsec. setup time of DIN vs. CK60, the PLD works with a 12 nsec. period for some consecutive commands (L1–L1, RDF–RDF).

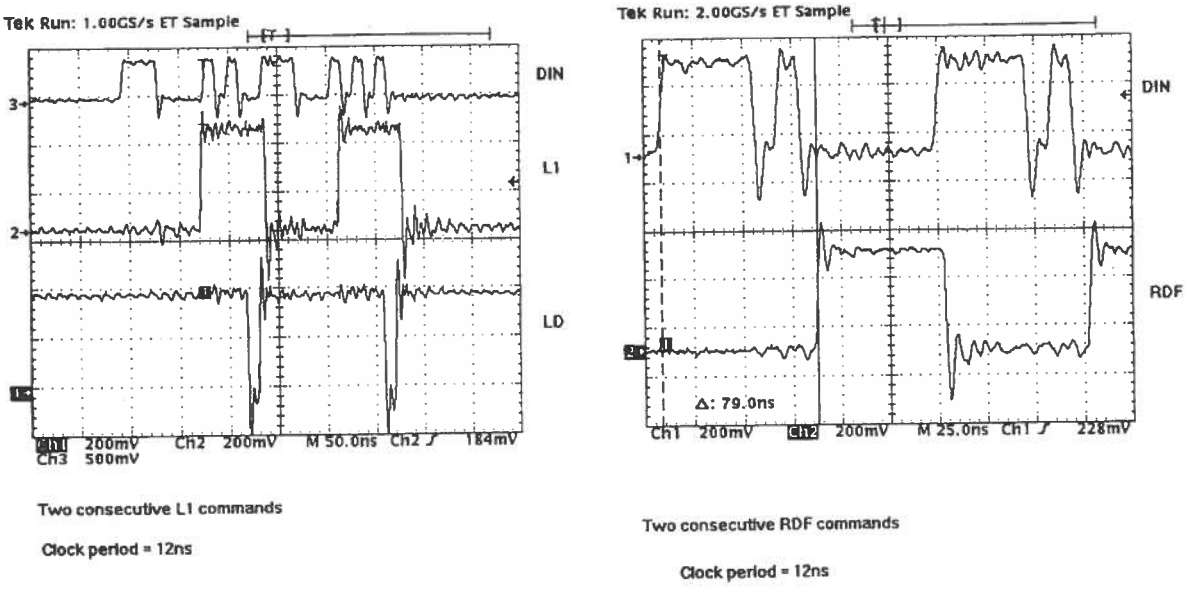

Fig. 6 – Decoding action of Cmddec PLD.

5. FRONT END INTERFACE MANAGER (Fec_fif)

Next to an L1 command, the Fec_fif PLD produces the necessary signals to assure correct writing of the strips data into the FIFO. In addition to SHIFT/LOAD and CK_CHAIN pulse train described previously, this PLD produces CK_M, CK_WR_F, EnH, EnR, EnTR to manage writing into the FIFO.

CK_M is a pulse train of 16 pulses delayed by 128 nsec. with respect to CK_CHAIN to take into account the fixed cable length between the FECs and the IFB. It is used to clock strips data into the 74F374 register bank.

CK_WR_F is the write signal to the FIFO bank. It consists either of a train of eighteen pulses, each time the board is acquiring FECs data (16 pulses for strips data, other two pulses for Header and Trailer), or it consists of just one pulse in case the board is working in diagnostic mode next to a write test pattern command WRF.

EnH, EnR and EnTR are the enable signals to write the Header, the register bank or the Trailer into the FIFO.

In Fig. 7 timing relation between above signals are shown.

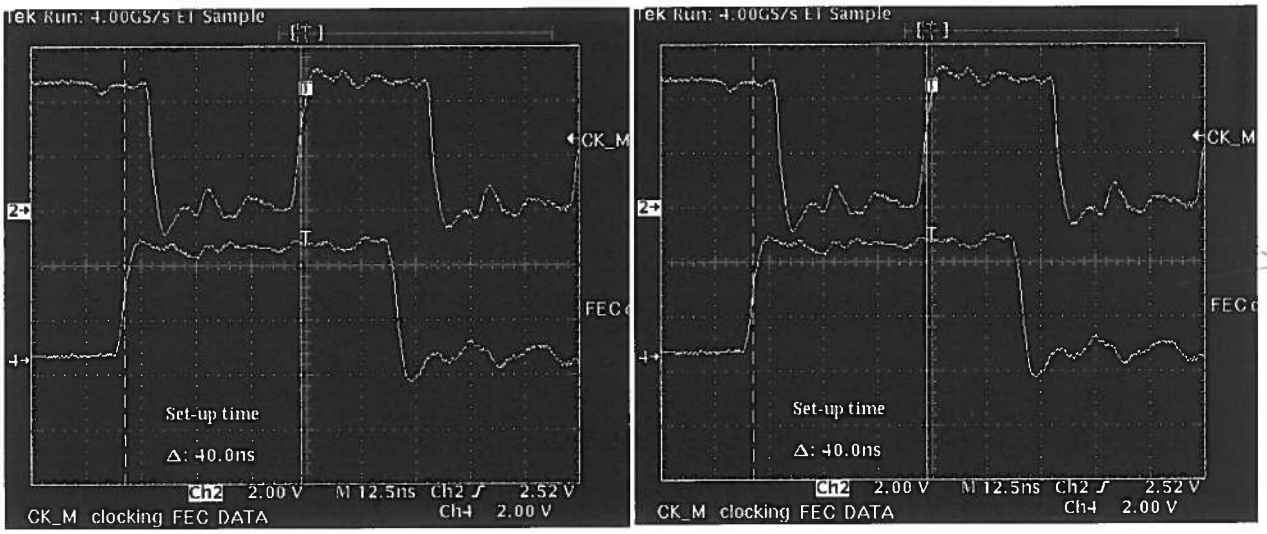

Fig. 7 – Signals managing acquisition from FECs.

Besides above functions Fec_fif produces the logical OR of empty flags and full flags of the eight FIFOs for further writing onto the header.

6. INTERFACE TO DAQ AND READER FIFO CONTROLLER

Once data are stored into the FIFO they can be read out either by an RDE command, which reads a whole frame (i.e. eighteen locations), or by an RDF command, which reads out just one location of the FIFO (RDF is used only in diagnostic mode).

Data are read out serially in any case at the frequency of 59.5 MHz. To accomplish this function two PLDs are used: Rdctr and Shift.

Rdctr generates the read signals to the FIFO bank. To simplify the PCB, instead of implementing a long 64 bit shift register, we have opted for a 16 bit bus at the output of the FIFO bussing together four chips. That way Rdctr PLD has become a little bit more complicated since four properly timed Read signals (RD_0 through RD_3) are to be produced, but routing has been

much improved allowing us to gain board area for other time critical signals. Furthermore, through a careful design of Rdctr, we have allowed much time (four cycles) for settling to the FIFO outputs before to produce the enable to load data to the output shift register (LDSR signal). That way much time is left to FIFO outputs to settle properly in spite of the slightly bigger parasitic capacitor coming from bussing.

Operations performed by Rdctr and Shift are similar both for RDE and RDF command.

In Fig. 8 timing for RD_0 is shown. This PLD, like the others, works faithfully up to a 12 nsec. clock period.

The Shift PLD behaves as a shift register parallel in (16 bit) serial out. To load the pattern into the Shift PLD the LDSR signal must be low and loading – being synchronous – occurs on the low to high transition of the 59.5 MHz clock. That way there is no idle state between data transmitted to DAQ. In fact after the transmission of the last bit of a sixteen bit word a parallel load occurs, and the first bit of the new word loaded is sent to DAQ. The serial input of the Shift PLD is stuck at zero so that the idle state of the DOUT line is set correspondingly.

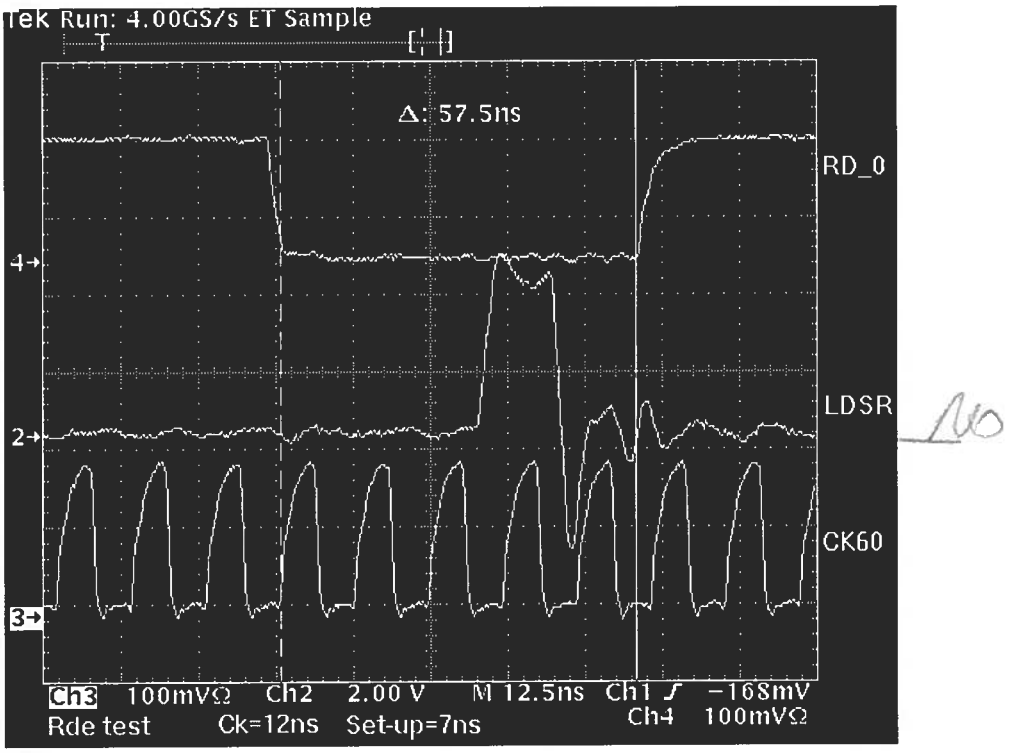

Fig. 8 – Signals managing reading from FIFO.

In Fig. 9 we show operation of Shift PLD up to a 12 nsec. clock period.

Beside the operation outlined above, the Shift PLD acts as a pipeline register both for two command signals (NOP and FALSE) and for two FIFO flag signals (EF and FF outputs of the Fec_fif PLD) for further writing onto the Header.

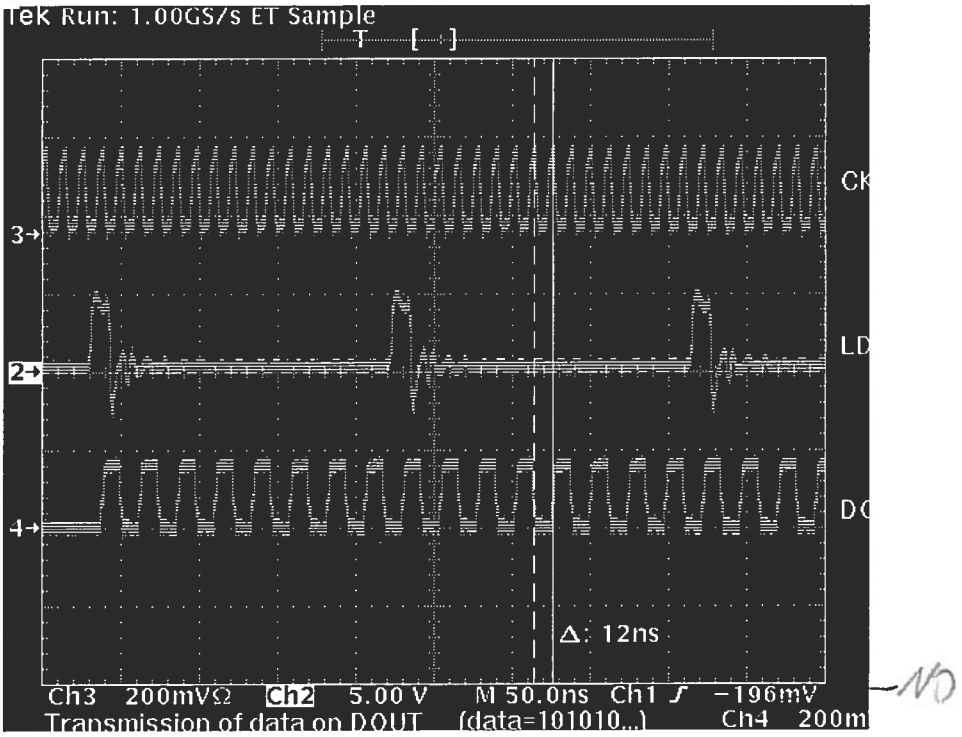

Fig. 9 – Serial transmission of data on Dout line.

7. THE TIME STAMP COUNTER PLD: TS_WRF

This PLD incorporates the eight bit "Time Stamp" counter which is reset by the NSYNC signal produced on the last cycle of a SYNC command. One bit of the counter CK15 implements a divide by four function and is used as a clock by Fec_fif, the manager of data acquisition from FECs. CK15 signal is always active as an output pin differently by the "Time Stamp" counter which is used internally. In fact the "Time Stamp" is latched synchronously into a pipeline register internal to this PLD by the LDS signal produced in the Cmddec. This pipeline register is then written onto the next header (EnH low).

In Fig. 10 we show the behavior of this PLD.

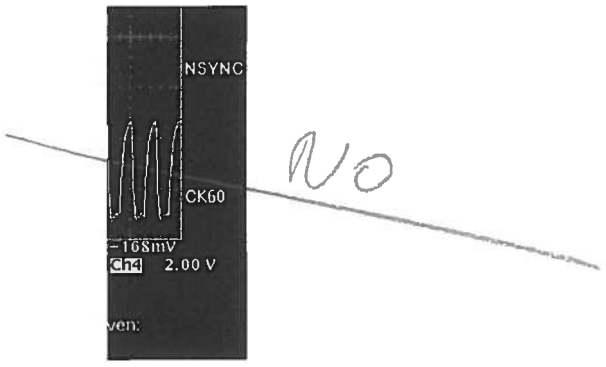

Fig. 10 – Writing of Time stamp and behavior of CK15 clock produced by Ts_wrf.

Beside above operations, the Ts_wrf PLD produces the enable signals for Header and Trailer generation and acts also as master for the diagnostic mode operation.

In fact next to an L1 command this PLD produces the enables (ET_0 and ET_1) and resets (RST_0 and RST_1) to Wrf0 and Wrf1 PLDs, so that a pattern of 32 zeroes can precede sending of the start bit – in case of the Header – and a pattern of 31 "ones" can precede a pattern of 32 "zeroes" – in case of Trailer generation.

Furthermore, next to a WRF command, this PLD produces the SCRST signal after 64 cycles to the Cmddec resetting its shift register so that this PLD can accept further commands, and an enable to load signal (ENST) to Wrf0 and Wrf1 PLDs.

ENST, like SCRST, is time critical and its equation cannot be combinatorial.

In the next figure we show the behavior of this PLD at 12 nsec. clock period.

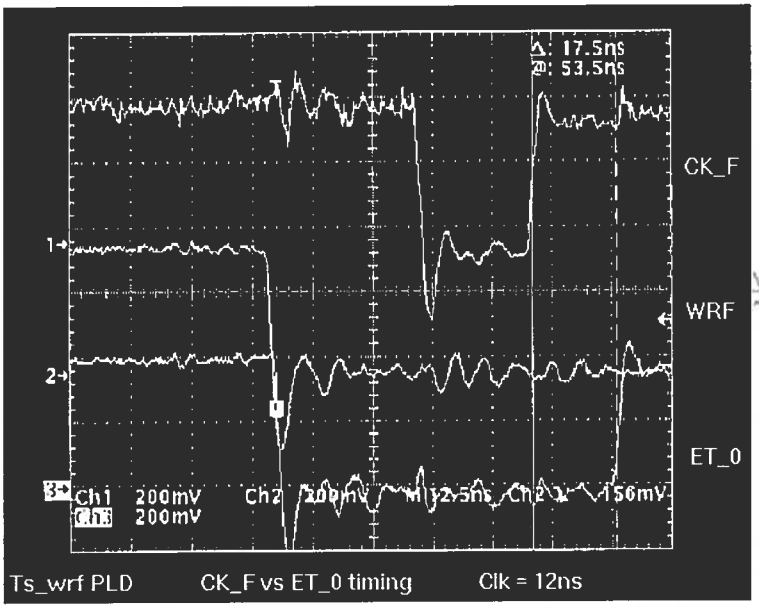

Fig. 11 – Signals managing test pattern writing into the FIFO.

8. THE IFB IN DIAGNOSTIC MODE: WRF0 AND WRF1

Each time the IFB operates in diagnostic mode and a WRF command is issued, a serial stream pattern is loaded into Wrf0 and Wrf1. After the whole pattern is loaded, Ts_wrf provides for a proper enable signal and for a write signal to the FIFO.

In Fig. 12 we show the behavior of this shift register next to a WRF command.

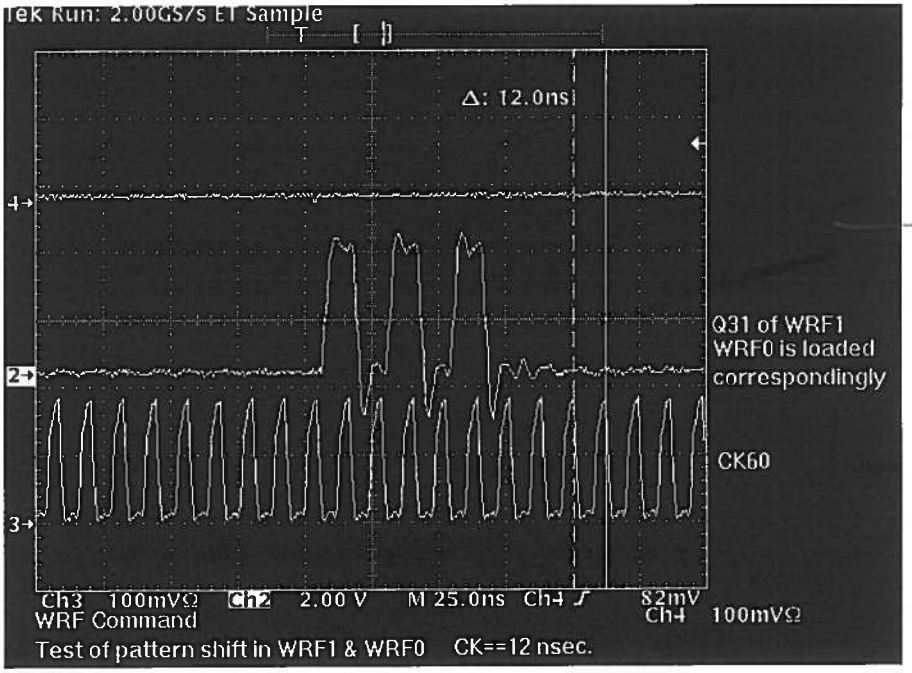

Fig. 12 – Shift registers WRF0 and WRF1.

9. SUMMARY

In this note we have described the functions and the design of a FIFO board for the IFR subdetector of the BaBar experiment. In particular we have shown in detail the logic blocks, implemented in seven MACH210–7 PLDs necessary to the correct operation of the board, and the proper generation of signals.

The tests on the PLDs have shown that all ones work correctly up to a 12 nsec. clock period.

REFERENCES

[1] Letter of Intent for the Study of CP Violation and Heavy Flavour Physics at PEPII, BaBar collaboration, SLAC Report SLAC–433, June 1994.
[2] BaBar Technical Design Report, BaBar Collaboration, SLAC Report SLAC–R–95 457, March 1995.
[3] R. Santonico and R. Cardarelli, Nucl. Instr. and Meth. **187**, 337 (1987).
[4] N. Cavallo et al., " A possible front–end readout scheme for the resistive plate chamber detector at BaBar", INFN/TC – 95/07.
[5] N. Cavallo et al., "Front–end card design for the RPC detector at BaBar", INFN/TC – 96/22.
[6] BaBar Note 281, BaBar DAQ Group, Draft 4/15/96.
[7] "MACH 1, 2, 3, and 4 Family Data Book", AMD, 1995.
[8] F. Fabozzi, P. Parascandolo, "Design of a high speed clock distribution network", INFN/TC (to be published).
[9] F. Fabozzi, P. Parascandolo, "Operation and performances of a high speed dynamic pattern detector", INFN/TC (to be published).