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DETECTOR ARRAY CONTROL AND TRIGGERING

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Detector Array Control and Triggering

Chimera Collaboration
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I. INTRODUCTION

To probe the properties of nuclei under extreme temperature and density conditions, experiments can be performed in Nuclear Physics at intermediate energies, using a multidetector system for charged particles. With this purpose in mind, we have designed and are constructing CHIMERA [1] a detecting apparatus capable of covering a solid angle of $4\pi*0.94$ using 1192 detection cells arranged in a cylindrical geometry around the beam axis in 35 rings, for a total length of ~ 4 m. Each cell consists of two detectors: a silicon detector (300 μm thickness) [2] is followed by a CsI(Tl) scintillator [3] (thickness ranging from 2 cm at backward angles up to 12 cm at forward angles). The forward 18 rings cover polar angles from 1° to 30°, using 688 cells. The remaining 504 cells (i.e. the backward 17 rings from 31° to 176°) are disposed in a sphere with a radius of 40 cm.

Mass and charge identifications are performed using both the Time of Flight technique and the ΔE-E matrix method. The signals coming from the CsI(Tl) detectors are also used for the identification of light particles of high energy, employing the shape discrimination method [3]. So, there are more than two thousand chains and more than five thousand signals to collect and to control, because each detector has its own electronic chain, consisting in power supply, preamplifier, amplifier, logic modules, analog-to-digital converter and each cell generates four analog signals (energy and time for Si, fast and slow components for CsI(Tl)).

In the present paper the tests of a prototype based on a Digital Signal Processor (DSP) are described. It is capable of real-time computing special algorithms in time intervals short enough to establish triggering conditions on-line. These tests were performed in order to choose the most suitable architecture with a view to developing a system based on one or more DSP-boards for the control and second level triggering.

As a benchmark algorithm has been employed the power-law formula for charged particle identification [4,5] already used by some of us for testing custom on-line computational systems [6]. Section II gives the general constraints for the present work. In section III the hardware and the software of the prototype are described, together with the module interfacing the DSP-board both to ADCs and to the data acquisition system (ACQ). This module is also used to test timing performances of a decisional unit for a 1st level trigger. Section IV shows the results achieved and the conclusions.

II. GENERAL CONSTRAINTS

The primary objective for the controlling of a complex system is to obtain its stable behaviour in all the operating conditions. The stability of the whole apparatus depends not only on the collected control parameters, but also on the timely executions of all the periodic control tasks. In order to guarantee a periodic activation of all the cyclical activities, it is necessary to foresee specific kernel mechanisms to handle timely critical processes. In real-time applications, many tasks are characterized by a deadline, which is the maximum time disposable for the completion of the tasks hard and soft.

Using detector arrays, as in our case, tasks must be devoted to solve some problems that can affect the data acquisition. In fact because of the very high number of detection cells, the data rate may be high also if the event rate is low, because the number of parameters to be collected is high and the interval between two events may be very small, due to the randomness of nuclear events.

These problems may concern the control of the different detector parameters, the whole apparatus calibration and the velocity of the data storage system.

With a view to satisfying these objectives it is necessary to carry-out real-time, on-line calculations of special algorithms. In all the three cases special algorithms have to be computed by means of dedicated kernels. Each kernel must perform the computation in a maximum time, smaller than the dead time characteristic of the data acquisition system.

The schematic of the data acquisition system of CHIMERA [7] is shown in Figure 1.

The most important timing constraints for an on-line computational system, allocated in a data acquisition system, are due both to the complexity of the algorithm to be computed and to the high data rate, as a consequence of the high number of collected parameters.

Each analog signal is usually converted from the ADC in a few tens of μs. Moreover, at the present state of the hardware, the Fast Data Link (FDL), used in the data acquisition system for the hardware readout, needs of about 300 μs for reading and transferring the data in the memory of a destination crate. So the aim is to compute, for the whole detector, the required algorithms in a comparable time.

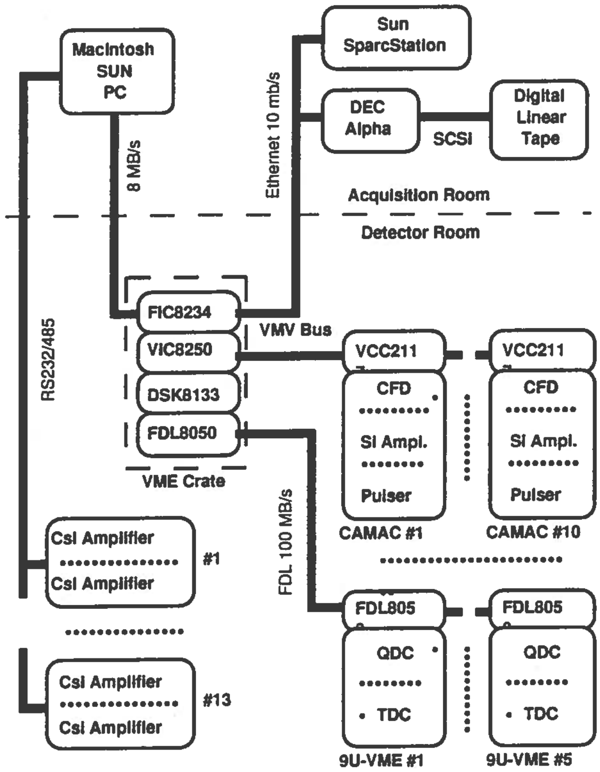

Figure 1: Schematic of Chimera Data Acquisition System

We have investigated [8] the fact that it is more convenient to use DSPs rather than other hardware solutions, because of lower hardware and software development costs, easier external environment interfacing and better computational perform-ances.

In order to complete the tests on the DSP-based system, we have decided to perform the on-line particle identification of the reaction products using the power-law formula [4] derived from the Bethe-Bloch relationship for the stopping power of ions.

In order to compute the power-law formula it is necessary to collect parameters by means of a telescope of two detectors. The first of them is the transparent detector (crossed by all the interesting particles). The reaction products lose in it only a part of their energy (ΔE) while the remaining energy (E) is lost in the second detector. The power-law algorithm is given by the Charge Identification Function CIF = $(E+\Delta E)^{X}-E^{X}$, where x is a real number depending on the kind of the reaction and of the produced ions (generally $1.5<x<1.8$). CIF is proportional to $M^{X-1}Z^{2}$ [9], and it is a function with a frequency distribution curve characterized by separate frequency peaks, each corresponding to a differently charged reaction product.

To perform also the mass identification of the reaction products it is necessary to measure the Time of Flight Δt. So in the case of non relativistic kinematics, it is possible to compute the Mass Identification Function ($MIF = E\,\Delta t^{2}$), that is proportional to the mass of the products. MIF also has a frequency distribution curve characterized by separate frequency peaks, each corresponding to a different mass of the reaction products.

From a computational point of view, CIF is more suitable to be used as a benchmark algorithm than MIF.

In the final release the DSP-board for the control and triggering systems, can be put either in the VME crate of the data acquisition system, in order to share the data coming from the FDL, or in the PCI-bus of a host computer, in order to receive the data from the FIC8243 through the network, using the broadcasting technique.

III. PROTOTYPE DESCRIPTION

As a minimal condition to be satisfied for prototyping, we have used only an elementary detection cell, consisting of one telescope of two silicon surface barrier detectors. For this telescope we have used CIF as a function to trigger the event collection, i.e. to reconstruct the energy-spectra of charge identified ions.

For fast real-time computing of CIF, we have chosen Texas TMS320C30 DSP [10] (33.3 MFLOPS and 16.7 MIPS) and the TMS320C30 EValuation Module (EVM) [11], installed in the ISA bus of a host PC. To evaluate the performances of the board before the on-beam tests, we have used an evaluation system, ad hoc realized [12]. CIF computation and discretization are carried-out by EVM, while I/O streams are simulated by using two PCs.

For connecting ADCs, DSP and ACQ an interface (IADA) consisting of two different symmetric parts, one for ADCs and the other for ACQ has been realized.

To implement IADA, Programmable Logic Devices (PLD), [Lattice (isp)LSI-1016] [13] have been used. This module has been connected to DSP, using the 5 Mbit/s serial port.

A pair of ΔE and E analog signals coming from the telescope electronic chains is converted by two ADCs. The two digital 12-bit words are read by IADA, using the needed protocol and controlling the time delay between the two words. IADA sends the acquired pair to the DSP serial-port, performing a parallel-to-serial conversion. At this moment the two data are read by the DSP and the required computations are carried-out.

The calculated, discretized CIF value is now presented, performing a serial-to-parallel conversion, on the output section of the DSP serial port together with the identified energy value, to be read by the output section of the interface.

Subsequently, with the proper handshaking the CIF value is read by the data acquisition system and visualized on the video-terminal of the host computer.

For calculating CIF, we have to compute trascendental functions. Generally we do not have at disposal a specialized processor for their calculations. So to solve this problem in assembly code we may use series expansion.

With this approach we can increase performances also by modifying the algorithm: series kind, expansion coefficient numbers and floating point format. We have chosen [14] to use Chebychev polynomial series expansion [6,12]. For more calculation details on CIF expansion in series of Chebychev polynomials, see ref. [6,15].

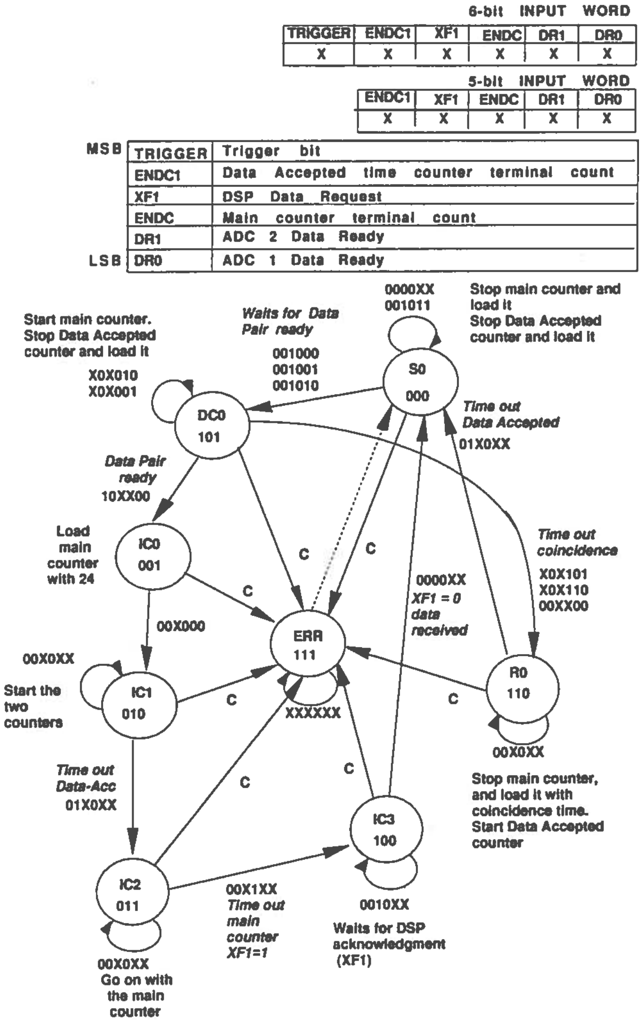

Figure 2: IADA State Transition Diagram

The easy programmability of PLDs together with a relatively fast response enable their use also in a flexible and more complex programmable system. So it is possible to use them as central decisional unit for a first level trigger of a detector array. IADA working period is 120 ns, corresponding to the external clock period given by DSP, i.e. twice its internal clock period. To speed up the working mode of the interface, the front edge of the external clock period from DSP is used for timing the state-machine, while the falling edge is employed for the slave devices.

In fact, from an ideal point of view IADA can be subdivided in the state-machine, and in slave auxiliary circuitry (like counters, shifters...). So IADA can be considered as working with a clock period of 60 ns.

IADA state-machine uses in this first release 5-bit input words. To use the interface module also for testing the timing performance of the decisional part of a first level trigger, the state-machine has been modified, using 6-bit input words. Each coincident ADC-word in input is compared with its own 12-bit mask-word used to simulate a pattern of discriminator signals, in order to accept or reject the event.

In Figure 2 is shown the state transition diagram for the two solutions. At rest IADA is in the S0 state. In this state the two counters (main and data accepted time) are stopped and set to proper values.

IC0 is reached (through DC0) only when a pair of data (ΔE, E) arrives in the coincidence time (and for the trigger when the trigger conditions are satisfied -trigger flag set-). Otherwise the system resets to S0 through R0. In IC0 the main counter is reset and loaded with the value 24, in order to serialize the two 12-bit data words. From IC0, through IC1 and IC2, IC3 is reached and IADA waits for the acknowledgment from the DSP. Every wrong combination of the input signal in every state causes IADA to fall in the error state (ERR).

The comparison is carried-out in less than a half clock period (60 ns) as previously said, independently of the length of the pattern word used, allowing to avoid the necessity of wait-states. The limitation to one fixed pattern per input word, is due to the lacking of internal memory of the used PLDs. In any case the extension to a number of patterns, as large as required, will need of an additional time, corresponding only to a memory access (few tens of ns, at maximum).

The software environment is structured in different levels : a single assembly program for the DSP, that performs all the operations connected to CIF calculation and identified-ion energy-spectra reconstruction, an User Interface Program (UIP), written in C language and running on the host PC that allows to easily control and monitor the experiment phases.

These different layers are interfaced by a C library, obtained by customizing the TEXAS EVM320C30 C library. The single assembly program implemented and driven by UIP allows four different operations to be performed (Figure 3):

1) Calibration, separately for each electronic chain;
2) Computation of maximum and minimum values for the Identification Functions (IF), in charge (CIF) and in mass (MIF);
3) IF spectrum discretization, using the maximum and minimum computed values;
4) Energy spectra reconstruction of the identified reaction products.

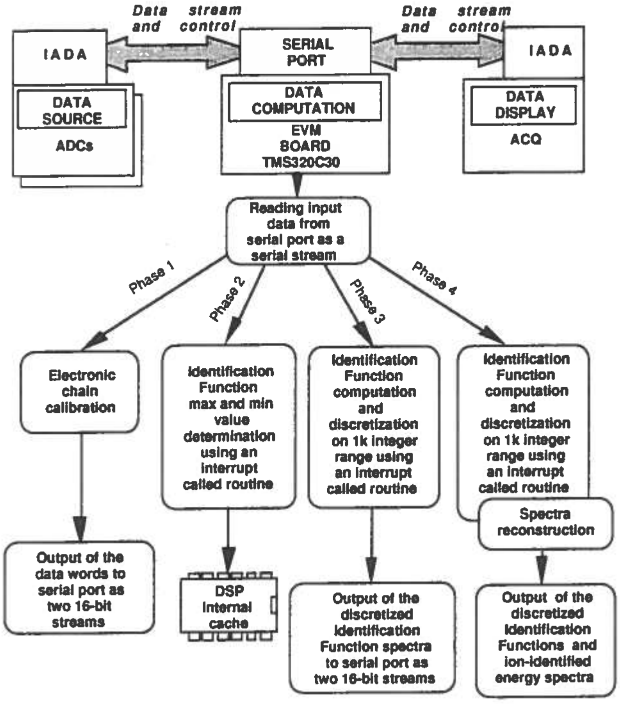

Figure 3: Program Flow Chart

In the on-beam test only the charge identification was performed. Both charge and mass identifications were performed using the energy and time digital data collected in a previous experiment [16], stored in the memory of the host computer.

IV.PERFORMANCES AND CONCLUSIONS

The on-beam test has been done, at the Laboratorio Nazionale del Sud, with the SMP Tandem and the C-2000 Scattering chamber. A carbon beam of 94 MeV has been used to bombard a 30 $\mu g/cm^2$ ^{12}C target.

A silicon detector telescope with a 50 μm thick transparent detector, a 1500 μm thick detector to stop heavier reaction products, and a 500 μm veto counter to avoid to collect particles with Z=1 has been used. The obtained results are reported in Figure 4, showing at $\theta_{lab}=30^o$ the identification spectrum of the emitted light ions ($2<Z<7$) for the ^{12}C $+^{12}C$ reactions.

In this paper we have described a new approach to solve the triggering problems that arise using a detector arrays. In fact the use of the DSP permits fast on-line computation of the real-time algorithms used for the 2nd level trigger. The test done on the 1st level trigger makes clear the opportunity to realize decisional units with PLDs because of the offered possibility to reconfigure the state-machine to follow evolving necessities, without doing any hardware modification, and also because they allow to carry-out simple operations, like pattern recognition, practically with no spending of additional time.

In fact we have taken into account the possibility to use DSP also as 1st level trigger decisional unit [17]. As test, we have used the same pattern recognition as for PLDs, obtaining, as result, a total time of 7 clk, corresponding to 420 ns, using TMS320C30 DSP. Anyhow, also with newer and faster DSPs, 7 clk is a time greater than that obtained with PLDs (60 ns).

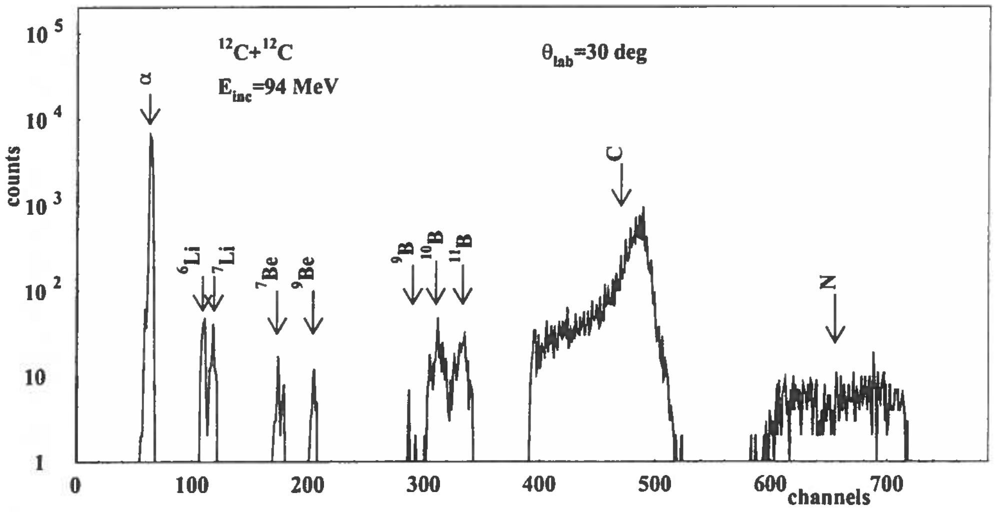

Figure 4: CIF Spectrum

We can conclude that the results achieved using old generation DSPs: 13.26 μs for event identification, of which 6.72 μs for CIF computation, 120ns for MIF computation are in any case good quality time results. They can better indicate the goodness of the approach if are read in terms of clock-cycle: 206, 112 and 2 clk respectively. In fact if we consider the new generation DSPs (120MFLOPs to be compared to 33MFLOPs of the one used in the present work) and to the new PLDs, with built-in memory up to 10 Kbits, we may easily extrapolate a significant time reduction.

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