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CRYOGENIC FRONT-END ELECTRONICS FOR FAST NOBLE-LIQUID CALORIMETRY

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ABSTRACT

We present results obtained after evaluating a few hundred monolithic preamplifiers designed to readout, at cold, the signal of the middle and back segments of the barrel LAr calorimeter of ATLAS. Those chips have been produced in GaAs MESFET technology using a foundry service.

1.- INTRODUCTION

The signal generated in a noble-liquid calorimeter cell can be read-out either by a cold hybrid or monolithic circuit or by a warm readout. Several thousands cryogenic preamplifiers have already been used in calorimetry starting with the HELIOS (NA34) experiment followed by RD3, P44 and NA48 prototypes. Good results and still better expectations in terms of noise, speed, sensitivity to pick-up noise, and cross-talk justified long term efforts to develop preamplifiers optimized for these applications[1,2]. In the case of ATLAS, inaccessibility imposes severe requirements to the reliability of all the components inside the cryostat. Reliability of cold electronics is mainly compromised by thermal stress, possible charge trapping, and high voltage discharges and not for the mere operation at low temperatures. On the contrary, operation at very low temperatures suppresses thermal activated processes (i.e. electromigration) responsible of most failures in electronic devices at room-temperature. Warm preamplifiers are connected to the detector via transmission lines of a few meters long. They have the advantage of not dissipating power inside the cryostat and that can be accessed at least once a year, but at the expense of higher electronic noise, cross-talk and pick-up noise sensitivity. In fact, when using cold preamplifiers the detector signal is amplified right at the cell's end before sending it out the cryostat where the risk of corruption by radiofrequency interference (RFI) or various origins is high. A warm readout circuit, instead, receives the current signal with no amplification at the outside of the cryostat. To reduce the impact of RFI, which could translate into higher coherent noise in the detector, single or double shielding technics should be used. A cold readout circuit provides input impedance of sufficiently low value, a few ohms, to reduce cross-talk effects. This can not be done in warm preamplifiers which should match the characteristic impedance of the transmission line.

To date, thousands of channels have been readout with cold preamplifiers since the very beginning of the RD3 collaboration. We have been pursuing development of monolithic preamplifiers for noble-liquid calorimetry based on GaAs MESFETs as those devices present high speed of response and low noise in a wide low-temperature range including that of LAr and LKr[3].

Recently, monolithic circuits specially designed to readout the middle and back segments of the ATLAS electromagnetic calorimeter have been fabricated. The main purpose of this fabrication run was to evaluate the feasibility of producing in the near future a large number of highly reliable chips to equip the whole detector (~50000 channels). We wanted to evaluate the uniformity of noise, gain and speed of the chips fabricated in the different wafers of a single foundry run. Also, we wanted to evaluate the circuit stability and its dynamic range for the nominal working conditions of the middle and back compartments of the detector which comprise a cell capacitance of 1 nF to 2 nF and a maximum detector current of 4 mA to 8 mA.

Finally, considering the severe environmental conditions imposed by the envisaged long term operation of ATLAS, about 10 years without access to the cryostat, we checked for thermal stress in passive devices and in the chips and charge trapping in the latter. Protection networks designed to limit the damage of accidental high voltage discharges have also been designed and tested.

In section 2 we describe "C4", the cryogenic monolithic chip designed for ATLAS LAr barrel calorimeter. In Section 3 we give details of the fabrication of a series of about 500 C4 chips, and in Section 4 we report the results of the independent evaluation made at BNL and INFN/Milano. In section 5 we briefly describe reliability issues and present recent results of thermal shock tests.

2. - "C4": A MONOLITHIC DUAL-CHANNEL COLD PREAMPLIFIER.

The building block of the cold readout circuit is a monolithic dominant-pole amplifier (DPA) fedback as a current-to-voltage converter. The feedback network consists of a resistor R_F in parallel with a capacitor C_F, both elements external to the chip, with values optimized for each compartment and for the whole range of pseudorapidity η covered by the barrel detector. The time constant $C_F \times R_F$ is set to ~20 ns and R_F is dimensioned to handle the large input current. Its value ranges from 430 Ω to 1.5 kΩ[4].

The chip was designed following previous experience[2]: a large MESFET, 3 x 24000 μm^2 at the input followed by a cascode loaded by a current source constitutes the gain stage; it is loaded by an intermediate buffer in turn followed by the output stage. The input transistor receives its bias current from a separate power supply. In this way power dissipation is kept low despite the dynamic range is high. The design was discussed with the BNL team with whom we agreed sharing the burden of characterizing a large number of chips in a very short time.

Although simulation of the chip performance at cryogenic temperatures can be done with high accuracy, an uncertainty always exists in a new design, in particular in what concerns very high frequency effects which could affect circuit stability. To reduce this risk C4 was designed initially in two "flavours": SC incorporating a single transistor in the cascode stage and DC having instead two devices in that stage. Simulations have shown that DC flavour had higher open-loop gain but lower phase margin. As enough space was available in the wafer "tile", a third flavour, LV, consisting of an SC with the output stage "shifted down" to lower voltage was also incorporated. We anticipate now that all flavours worked well but DC gave the best performance. Therefore, for space reasons, we will mostly report in this paper the evaluation results of C4-DC chip whose circuit diagram is presented in Fig. 1.

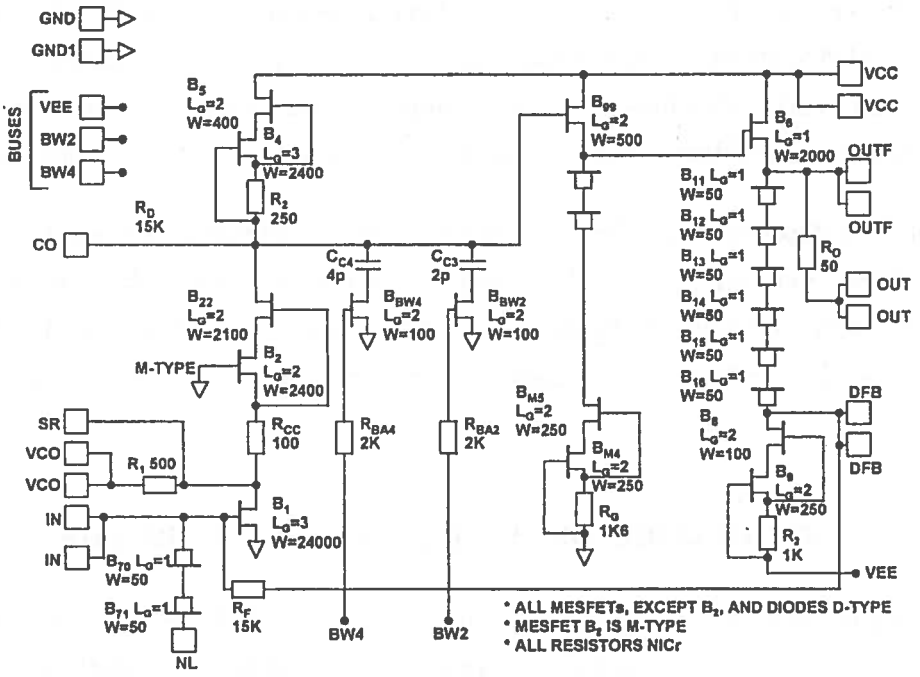

Fig. 1. Schematic diagram of the monolithic cryogenic preamplifier C4 - DC.

3. - FABRICATION OF A SMALL PRODUCTION SERIES

Four 4" wafers carrying C4 dice, as well as other projects, have been fabricated using TriQuint's QED/A GaAs MESFET process. Each wafer contained 30 tiles of 15 x 13 mm^2. In each tile a set of dice (1 SC, 1 DC and 1 LV) plus one extra LV die was accomodated. Each die measures 1.5 x 2.5 mm^2 and contains two identical circuits. As explained above, the purpose of this fabrication run was to establish the uniformity of chip performance at cryogenic temperatures within a wafer and along the four wafers. In order to follow possible disuniformities within a wafer, we have received and evaluated 15 sets of chips from the first wafer (#39). Each set was identified according to their original position in the wafer. After assembly, half of those sets have been sent to BNL for independent evaluation. Fig. 2 shows how the wafer is subdivided in 30 tiles tagged with their position, and the 15 tiles that have been evaluated to identify the best flavour.

Chips have been assembled into dual-in-line (DIL) 18 pin ceramic packages using silvered epoxy for die attach and 25 μm gold wire for ball-bonding. Two wires per contact have been used in almost all connections to further improve reliability. Fig. 3 shows a photograph of the assembled chip taken with a scanning electron microscope. Fig. 4 shows in a larger scale a detail of the die surface.

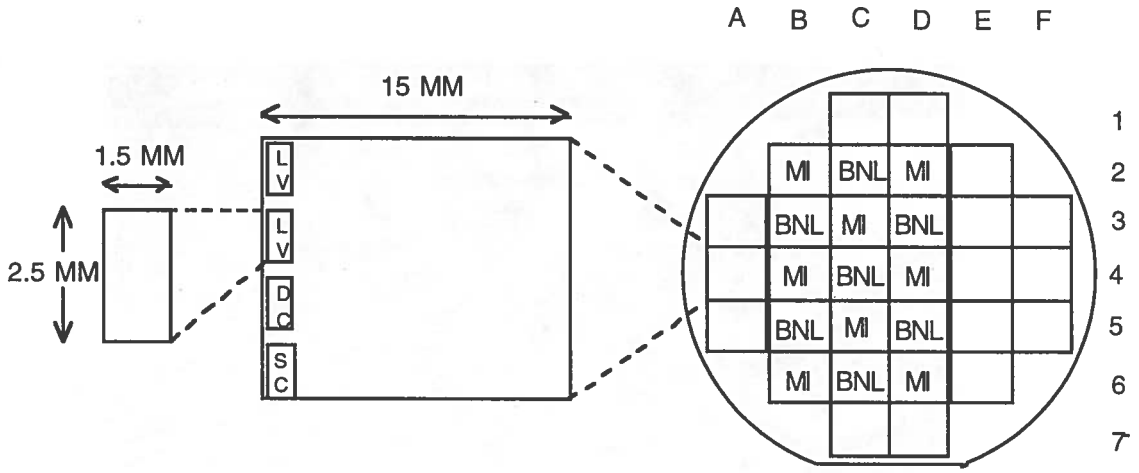

Fig. 2. A wafer is subdivided in 30 tiles each one containing four dice.

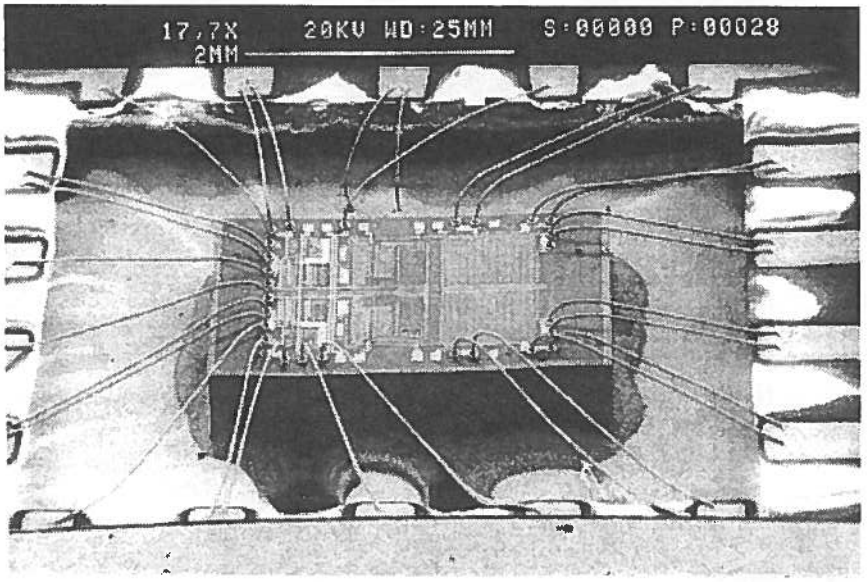

Fig. 3. Chips have been assembled into 18 pin DIL ceramic package. The chip dimensions are 2.5 x 1.5 mm^2 and it contains two channels. Two bonding wires per pad have been used in almost all contacts.

4. - EVALUATION OF CHIPS PERFORMANCE

For evaluation, tests PCB's have been prepared simulating the readout of two cells of the calorimeter. The PCB contains the feedback components, the capacitance simulating the detector and a DIL socket in which the chips under test are plugged in. One of the two channels of the chip, channel A, "sees" an external capacitance C_D = 1 nF and its feedbak network consists of R_F = 820 Ω in parallel with C_F = 22 pF. The second channel, B, sees C_D = 2.2 nF and has R_F = 430 Ω and C_F = 56 pF. A CR-RC^2 shaper followed the preamplifier.

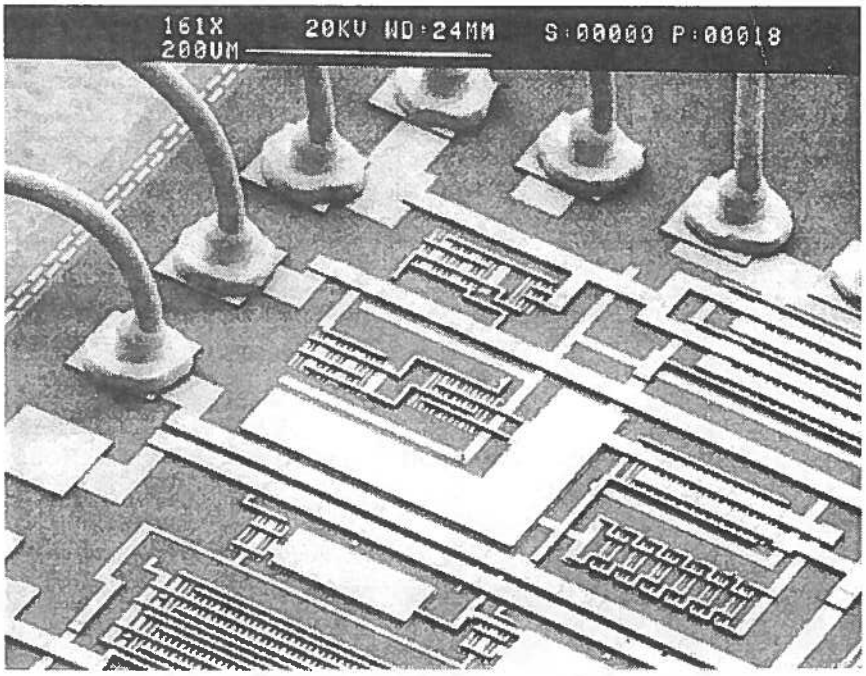

Fig. 4. A closer view of the C4 - DC surface.

An exponential current pulse with a time constant of 400 ns was applied as a test signal by using a step voltage generator and a series of a capacitor C_T and a resistor R_T. C_T-R_T values were 47 pF and 8.2 kΩ respectively during noise measurements and 470 pF 820 Ω during linearity measurements.

Results of evaluation are summarized in Table I. Amplitude and peaking time have been evaluated at shaper output.

Table 1: Results of evaluation at 87 K of the three different C4 flavours.

	Peaking Time tp [ns]		ENI at tp [nA]		Amplitude [mV]	
	C_D = 1nF	C_D = 2.2 nF	C_D = 1nF	C_D = 2.2 nF	C_D = 1nF	C_D = 2.2 nF
SC	37.7±0.80	41.3±0.73	161±20	363±35	205±4.0	94.5±1.7
DC	35±0.50	35±0.60	154±15	335±32	228±3.0	113±1.4
LV	39.3±0.60	39.9±0.59	154±8.0	327±31	200±9.8	97.9±5.7

As can be observed, DC flavour has the lowest noise (at the same tp), is the fastest and has the smallest dispersion of gain. Double cascode allows better open loop gain, and it is free from triggered oscillations that appeared in previous designs. Good agreement was obtained between the measurements done at both Labs. Table 3 summarizes the main parameters of the selected chip flavour C4 - DC.

Table 3: Main parameters of the monolithic C4-DC chip at 87 K

GBW Product (compensated)	1.7 GHz
Series White Noise	0.33 ± 0.015 to ±0.045 nV/√Hz
Corner Frequency of 1/f Noise	0.8 MHz
Dynamic Range	3 V with 0.6% INL
Power Dissipation	70 mW

Following determination of the best C4 flavour, we looked at all the other DC's fabricated in the four wafers and visually inspected. Also additional LV's, determined to be the second best, have been analized in order to complete a total number of 200 chips that added-up to the initial 50 units from the first wafer. A total number of 250 chips (500 channels) have then been evaluated of which 120 DC's. The production yield was very high: ~86%. In fact, we could verify that only 17 DC chips out of 120 fabricated in the four wafers presented defects; actually, 15 have been screened by visual inspection while 2 units have been found faulty only when performing the first electrical tests. Similar result was verified with the LV's, although we could not precisely determine the yield as we do not now how many units were screened by visual inspection.

Another interesting result was to found that series noise density varies as the channel bias current I_D to the power -0.25, which demonstrates that noise in contributed only by the input FET. In fact, noise density is inversely proportional to the square root of the FET transconductance which in turn is proportional to the square root of I_D. Second-stage noise contribution, noticeable in a previous monolithic circuit realized for LAr calorimetry[2] was this time strongly suppressed. Direct measurements of noise spectral density of the input FET were in agreement with the values extracted from ENI.

In Fig. 5 we present a plot of ENI vs tp for two different detector capacitances. It can be noted that the plot follows nicely the $tp^{-1.5}$ law as expected[5]. Noise dispersion was evaluated at t_{ptr} = 40 ns, either at C_D = 1 nF and at C_D = 2.2 nF.

While making noise measurements, the peaking time and amplitude at the shaper output was

monitored to also evaluate gain and speed dispersion. The results are indicated in Fig. 6,7 and 8.

Regarding large signal response, measurements have been done in the following conditions: C_D = 1nF; Imax = 4 mA and C_D = 2.2 nF; Imax = 8 mA. Integral nonlinearity was determined to be less that 0.6%, Fig. 9.

Coming back to noise, the value of series noise density e_n was extracted from ENI measurements and plotted as a function of the channel resistivity RSD, as in Fig. 10. The results for this foundry run, NOV 95, are in good agreement with previous runs and confirms that, at cold, noise density of MESFETs and its dependence with temperature are smaller for lower channel resistivity (higher doping).

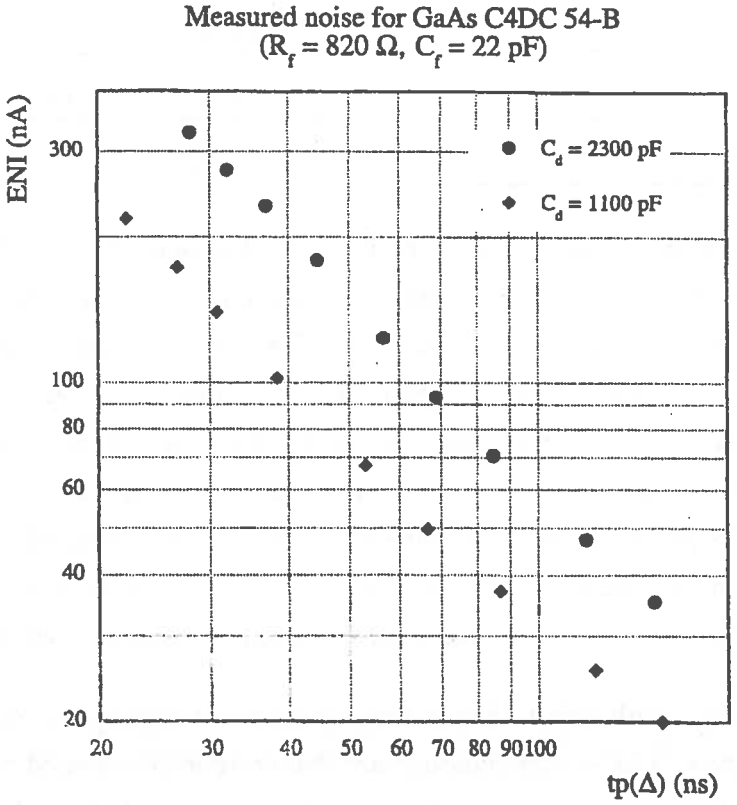

Fig. 5. Equivalent Noise Current (ENI) versus peaking time for two different detector capacitances as determined by the BNL team on chip 54-B (wafer #41).

5. - RELIABILITY ISSUES

Having no access to the detector components inside the cryostat for a long time, put severe requirements to system reliability. Connectors, mother boards, resistors and capacitors will be subjected to mechanical stress during thermal cycling (filling and emptying the cryostat with LAr). Active devices must withstand thermal and also electrical stresses that may provoke charge

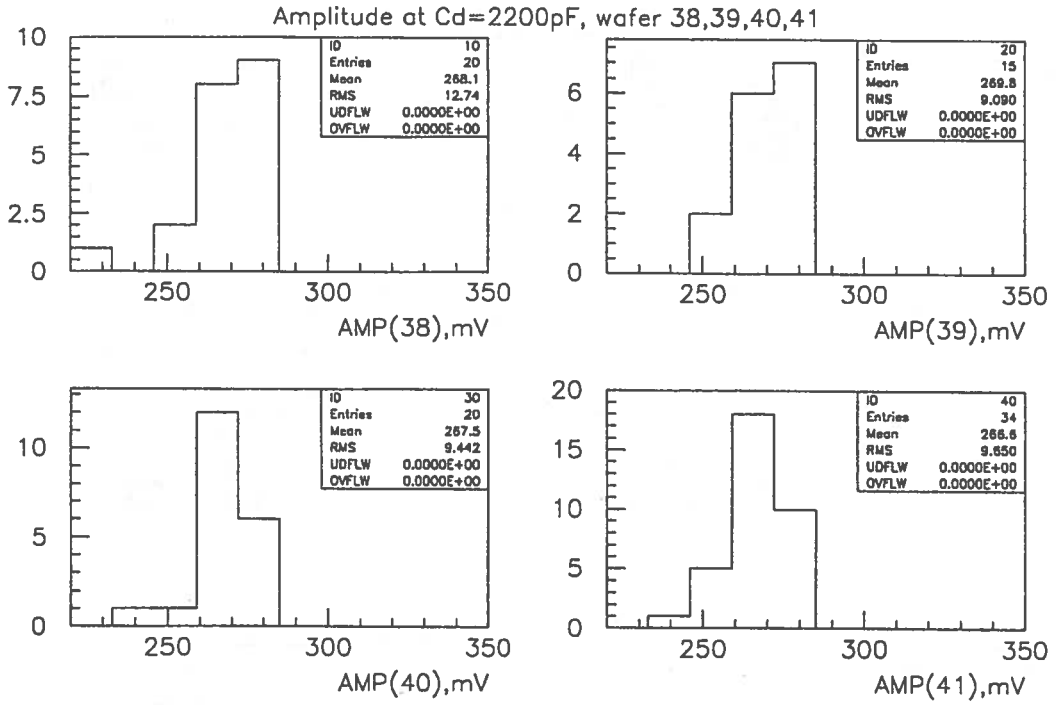

Fig. 6. Amplitude distribution in the wafers #38 to #41. Dispersions are 4.8%, 3.4%, 3.5% and 3.6% respectively.

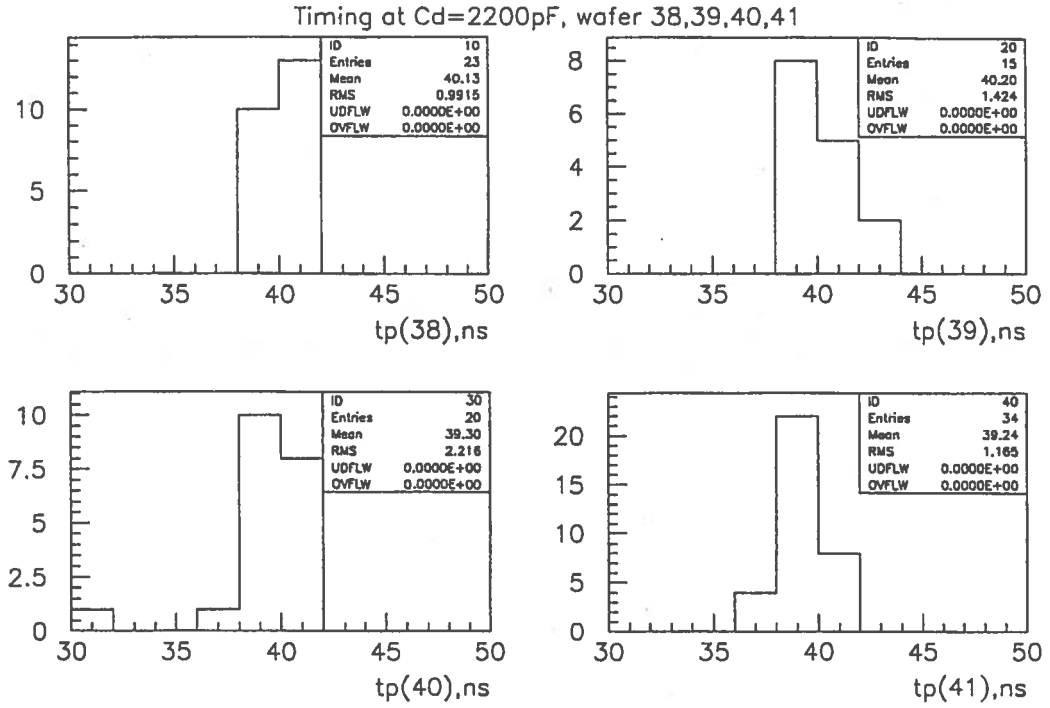

Fig. 7. Peaking time distributions in wafers #38 to #41. Dispersions are 2.5%, 3.5%, 5.6% and 3.0% respectively.

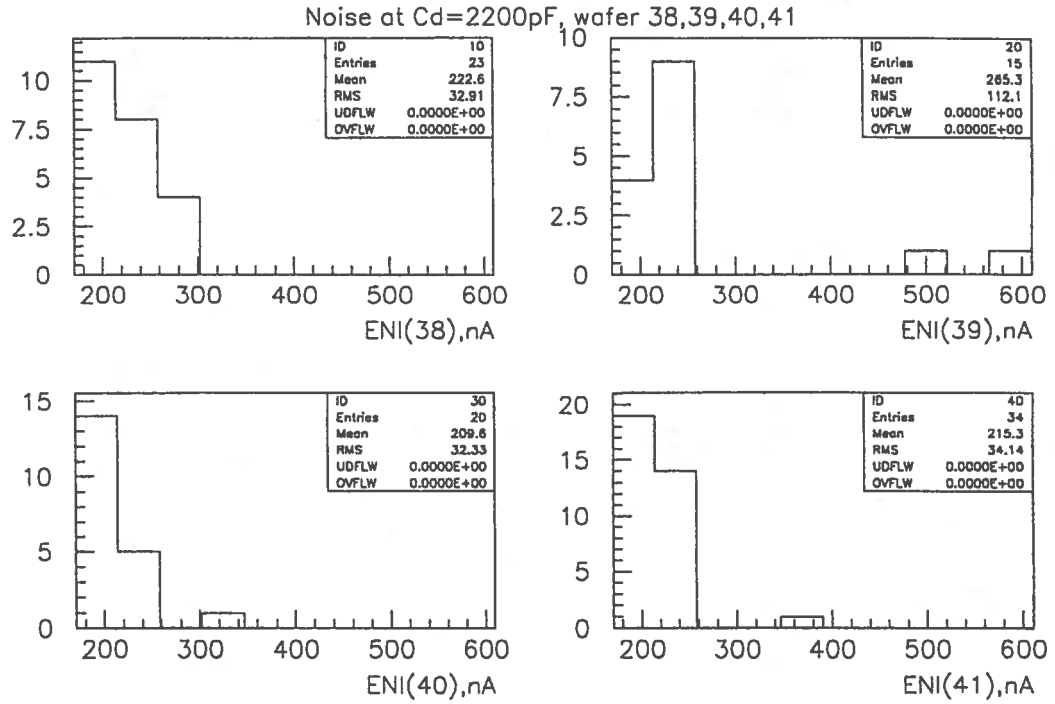

Fig. 8. Equivalent Noise Current distributions in wafers #38 to #41. Dispersions are 15%, 4.5%, 8.8% and 9.5% respectively. The four channels with higher noise have not been included in the statistics.

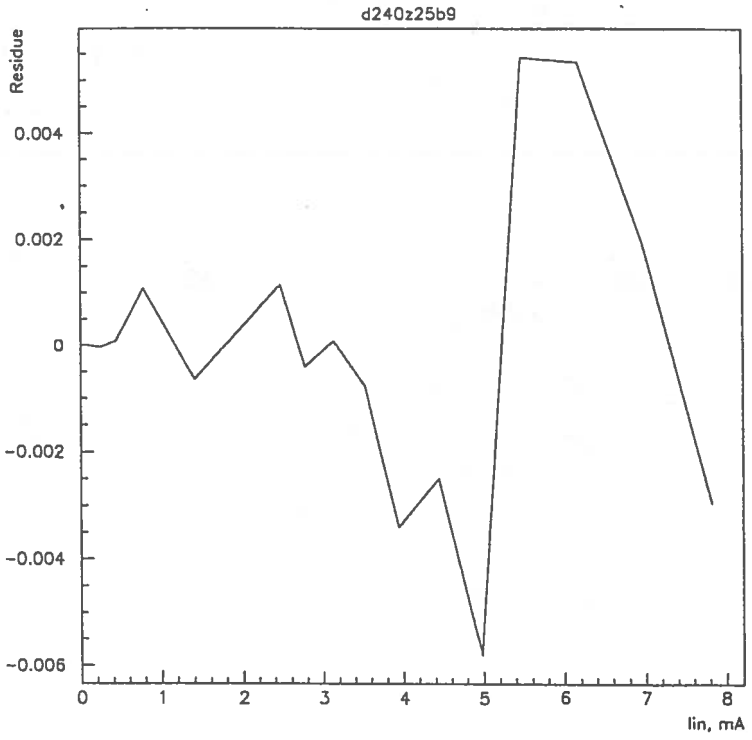

Fig. 9. Residues to a linear fit, normalized to 8 mA, as a function of maximun detector current. Vcc= 9 V. Integral non-linearity is 0.6%.

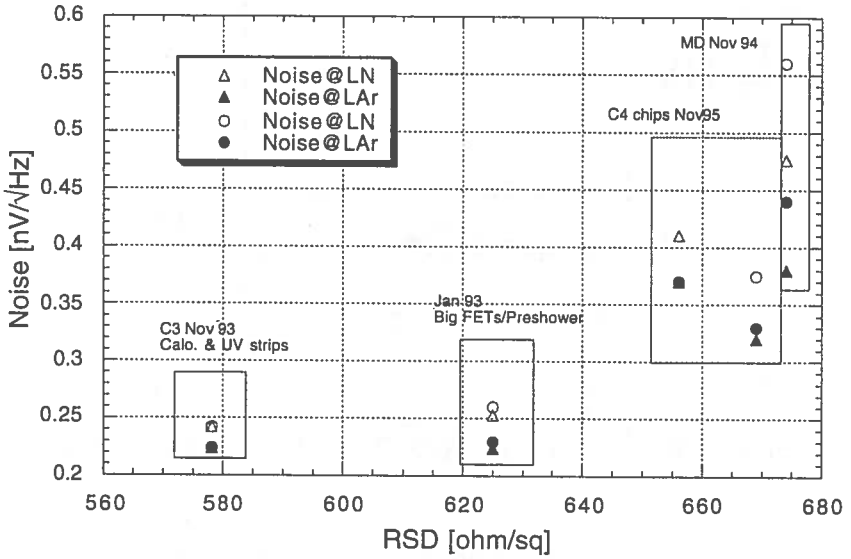

Fig.10. Noise density of MESFETs made in various foundry runs, at 77 K and 87 K as a function of channel resistivity.

trapping (which evidences as a change in the device characteristics). High voltage discharges could destroy the device if it is not protected with an adequate network. All these aspects have been given due attention.

Charge trapping was not observed in TriQuint's FET's neither in Vitesse FETs(6) which are also ion-implanted devices of similar characteristics to TriQuint's.

Mechanical stress have been checked by subjecting 7 chips and a set of passive components to ~700 thermal shock cycles from + 50 ^{o}C to 77 K, every 50 sec. No failures have been detected in the chips. In a few cases, at the end of the test, a tiny crack was noticed in the ceramic lid, which suggested use of metallic lid as a better solution. Most noticeable was the damage in the cables used in the test jig.

As for high voltage discharges, a protection network was designed and evaluated. Its schematic circuit is indicated in Fig. 11. Tests have been performed confirming that the network is effective to protect the chips against energy absorption of 6 mJ. In fact, ~25000 discharges of a 2.2 nF (blocking) capacitor charged to 2.3 kV did not provoke degradation in chips performance.

Another aspect related to reliability is radiation damage. It was already demonstrated that cold preamplifiers are radiation hard to the levels envisaged for 10 years operation of LHC at the barrel region(7)

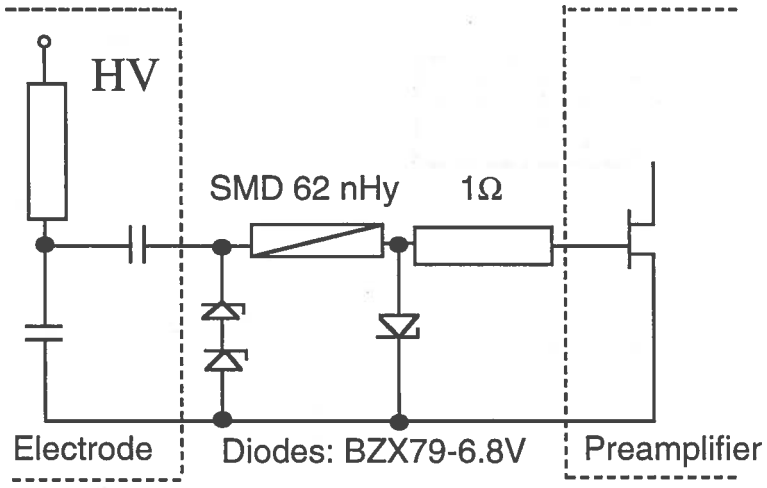

Fig. 11. High voltage protection network for C4 chips.

6. - CONCLUDING REMARKS

Recent experience of fabricating almost 500 monolithic preamplifiers using a GaAs MESFET foundry process gave positive results. More that 200 chips have been evaluated. The fabrication yield was very high: ~86%. In the four wafers fabricated amplitude and timing dispersion was below 5%. Integral-nonlinearity for the full signal excursion (8 mA, 3 V at the output) was 0.6%. Series noise was 0.33 nV/√Hz with ± 5 to ± 15% dispersion. The noise level agrees with the expected value according to the resistivity of the wafers.

Test to evaluate thermal stress damage showed that chips can at least survive 5000 chips x cycles. Also passive components, including electrolytic capacitors, suitable for cryogenic operation have been identified and tested for thermal stress.

We believe that the excellent performance of cold preamplifiers in terms of noise, speed, cross-talk and pick-up noise sensitivity could be safely used in noble-liquid calorimetry providing that the electrodes are designed to limit the energy delivered in case of an accidental HV discharge and/or suitable protection networks are used.

7. - ACKNOWLEDGEMENTS

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evaluation measurements in a very short time.

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