

ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Trieste

INFN/TC-97/25
8 Settembre 1997

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SIMULATING INTRINSICALLY AC-COUPLED HYBRID PIREX DETECTORS

SIS-Pubblicazioni
dei Laboratori Nazionali di Frascati

Simulating intrinsically AC-coupled hybrid pixel detectors

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Abstract

A bonding technique allowing AC-coupling of large hybrid pixel detectors in a simple and economic way is proposed. It consists in using a screen printing method to deposit *non-conductive* glue drops to interconnect diodes and VLSI cells. The AC-coupling can thus be achieved through the capacitance defined by the non-conductive glue drop realising the bonding itself. The feasibility of the proposed technique, together with its limitations, has been investigated by calculations and PSPICE simulations on a 5x5 pixel array.

Submitted to Nuclear Instr. and Meth. in Phys. Res. A

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1. Introduction

In the last years, a large amount of conceptual and experimental studies on silicon pixel detectors has been carried out, leading to several applications in High Energy Physics [1-6]. Hybrid pixel detectors are going to be extensively used as vertex detectors in the LHC experiments currently under development [7-9].

In this experimental environment, radiation damage effects are expected to be a crucial item for both detectors and electronics [10]. Different VLSI technologies are being studied to realise rad-hard front end electronics [11]. As far as the detector diode is concerned, one of the main effects related to radiation damage is leakage current increase. This effect can be extremely important because it scales linearly with particle fluence [12]. At the very short shaping times foreseen at LHC ($\tau_M \approx 10\text{-}30$ ns), this does not seem to constitute a major problem from the noise point of view, because the total ENC is expected to be dominated by the amplifier series noise, which scales as $(1/\tau_M)^{1/2}$. Nevertheless, dynamic range reduction due to preamplifier saturation may easily occur in case of dramatic increase of leakage current. Even if different solutions can be envisaged to reduce it (e.g. operating detectors close to 0 °C and/or annealing cycles), the problem could obviously be avoided by AC-coupling the detector diode to the preamplifier input. This can be naturally done using a properly modified screen printing interconnection technique.

In the next Section, a brief description of the bonding technique is given and the proposed method is described. In Section 3, a 5x5 pixel array model is introduced, together with a simplified small signal equivalent circuit of a charge sensitive preamplifier connected to each diode. According to this model, the validity of the method is then discussed in Section 4, through PSPICE (version 6.2.J, © MicroSim Corp.) simulations reproducing the detector operation. Conclusions are then drawn in Section 5.

2. The hybridisation technique and the AC-coupling method

Screen printing can be effectively used to deposit small glue drops, matching the geometry defined by a mask, on contact pads having diameters larger than ≈ 120 μm . A VLSI chip flipping, alignment and deposition procedure on the screen printed substrate, followed by a proper glue polymerisation thermal cycle, completes the detector assembly [13, 14].

This method, using conductive glues, proved to be cheap and to have an acceptable missing contact rate (less than $1/10^4$, [14]); moreover, it is reliable as far as thermal stresses, radiation damage and electromigration effects are concerned [14, 15]. A proper pad metallization is required to prevent contact problems related to the naturally grown aluminium oxide and to ensure long term bond reliability. An improvement in mask realisation and low viscosity glues is necessary to fit smaller contact pads. Nevertheless, the technique can be easily used in the

case of macropixels (a few hundreds of μm side) leading to a fast, cheap, wholly in-lab controlled hybrid pixel detector assembly procedure.

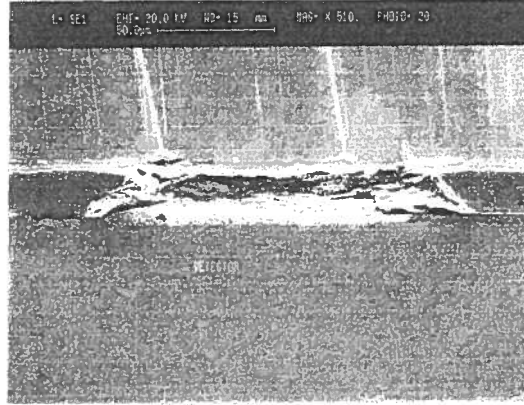


Fig. 1 SEM photograph of a typical contact obtained with a screen printing hybridisation technique. The contact can be approximated to a cylinder with a height of $\approx 20 \mu\text{m}$ and a radius of $75 \mu\text{m}$.

Up to now, only *conductive* glue has been used for pixel detector realisation, but a large class of thermally conductive yet electrically insulating screen-printable glues are available. This suggests the possibility of using a non-conductive glue drop to realise a decoupling capacitor intrinsically contained within the bond assuring the mechanical stiffening of the detector. The capacitor is made by the two metal pads (on the diode and VLSI cell respectively) having the polymerised glue drop as the insulator between them. The decoupling capacitance C_{dec} is thus the bonding capacitance itself (C_{bond}). The bonding capacitance can be easily evaluated knowing the shape of the bonds and the dielectric constant of the glue; typically, the bond can be assumed to be cylindrical, having a height h (distance between the two substrates) of about $20 \mu\text{m}$ and a base radius R of about $75 \mu\text{m}$ ([14], see Fig. 1). The typical dielectric constants of the non conductive glues for screen printing range between 3.0 and 5.6 [16]; in the following, an average value of 4.3 will be considered in the calculations. The capacitance of a parallel round plate capacitor is given by the Kirchhoff formula [17]:

$$C_{\text{bond}} = C_0 + \epsilon_0 \epsilon_{\text{glue}} R \left[\ln \left(\frac{16\pi R}{h} \right) - 1 \right] \quad (1)$$

where $C_0 = \epsilon_0 \epsilon_{\text{glue}} \pi R^2 / h$ is the first order capacitance, evaluated by considering a standard parallel plate capacitor.

Using the semi-empirical formulas contained in [18] and Eq. (1), it is possible to evaluate, for a given geometry of the detector diode and the VLSI cell (and once that the contact pad

dimension, given by the radius R , has been chosen), all the capacitances involved: the junction capacitance C_j , the inter diode capacitance C_{ip} and the decoupling capacitance $C_{dec} = C_{bond}$. The ratio C_{bond}/C_{ip} is given by:

$$\frac{C_{bond}}{C_{ip}} = \frac{\epsilon_{glue}R}{\epsilon_{Si}L} \ln\left(\frac{2g}{d}\right) \left[\frac{R}{h} + \frac{1}{\pi} \left(\ln \frac{16\pi R}{h} - 1 \right) \right] \quad (2)$$

where d is the p^+ implantation depth, L is the pixel side (with the obvious *a priori* condition $L > 2R$) and g is the gap between adjacent diodes. In Table 1, typical geometry sets, together with the corresponding capacitances, are listed. In this Table (and throughout the whole paper) the pixel side L has been taken to be $(2R+150) \mu\text{m}$: this is because the contact pad must be obviously fully contained inside the square pixel and some room (depending on the process technology used and on the cell architecture and complexity) must be left to realise the circuit. In fact, on the VLSI substrate, the contact pad size is a trade-off between the needed diode size and the required cell performances. If a certain design technology is chosen to realise a specific circuit, its dimensions are frozen, thus leaving all the remaining space available for the contact pad. We have chosen $150 \mu\text{m}$ as a reasonable value (to be added to $2R$) for digital readout cells developed with a standard technology [19].

$L (\mu\text{m})$	$R (\mu\text{m})$	$C_j (\text{fF})$	$C_{ip} (\text{fF})$	$C_{bond} (\text{fF})$	C_{bond}/C_{ip}
300	75	30	19	45	2.4
350	100	45	22	77	3.5
450	150	70	28	162	5.8
550	200	105	34	277	8.1
650	250	150	40	423	10.6

Table 1 Typical geometry sets and corresponding values of the various capacitances. The pixel side L has been taken to be $(2R+150) \mu\text{m}$, where R is contact pad radius (see text).

It can be clearly seen that C_{dec} can be made significantly larger than C_{ip} , thus showing, in principle, the possibility of an effective AC-coupling without an excessive charge loss to the neighbouring pixels [20]. It should be also noted that the "minimum" pixel size must be close to $500 \mu\text{m}^2$ to allow a sufficiently high C_{bond}/C_{ip} ratio. In fact, the gain in the ratio C_{bond}/C_{ip} when increasing the pixel side, is due to the fact that C_{bond} scales, in a first order approximation, as R^2 (and R is proportional to L), while C_{ip} scales only linearly with L [18]. Therefore, in the following, the critical case of about $500 \mu\text{m}^2$ pixels will be considered as first.

column of Table 2 reports the ratios between the Hit Pixel Amplifier output (HPA_{AC}) and the corresponding *ideal* preamplifier output in case of DC-coupling (HPA_{DC} , given by Q/C_f). Even if, with this geometry, it is not possible to collect the full released charge (too low C_{bond}/C_{ip} ratios), the signals are sufficiently high to be detected above typical digital VLSI noise thresholds [25].

C_{bond} (fF)	R (μm)	$2R/L$	C_{bond}/C_{ip}	HPA_{AC}/HPA_{DC}
50	92	0.41	1.8	21%
100	130	0.58	3.6	34%
150	159	0.71	5.4	44%
200	184	0.82	7.1	50%

Table 2 Summary of the parameters used for the simulations in the case $L = 450 \mu\text{m}$ described in Subsection 4.1. The bonding capacitance has been varied from 50 fF to 200 fF by varying the bond dimension (i.e. the radius R , see second column). The glue dielectric constant was kept fixed at the average value 4.3 discussed in Section 2.

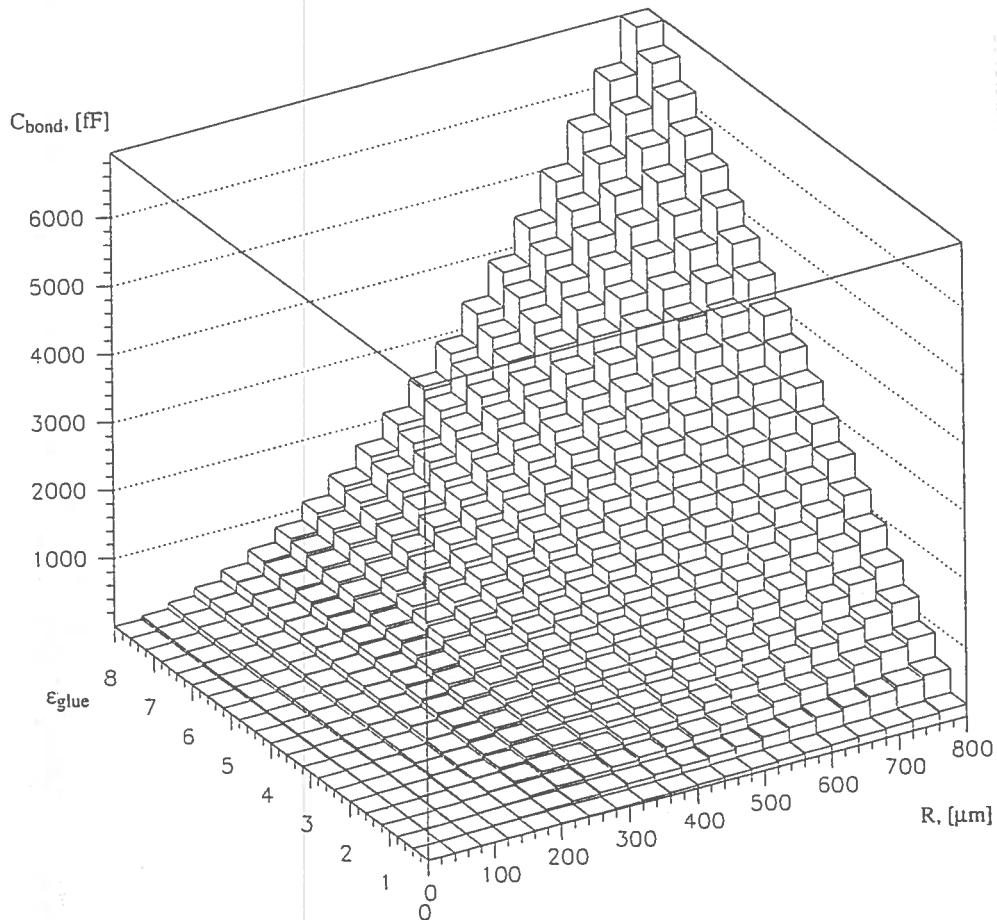


Fig. 6 Plot illustrating the dependence of the bonding-decoupling capacitance on the value of the glue dielectric constant and on the bonding area radius.

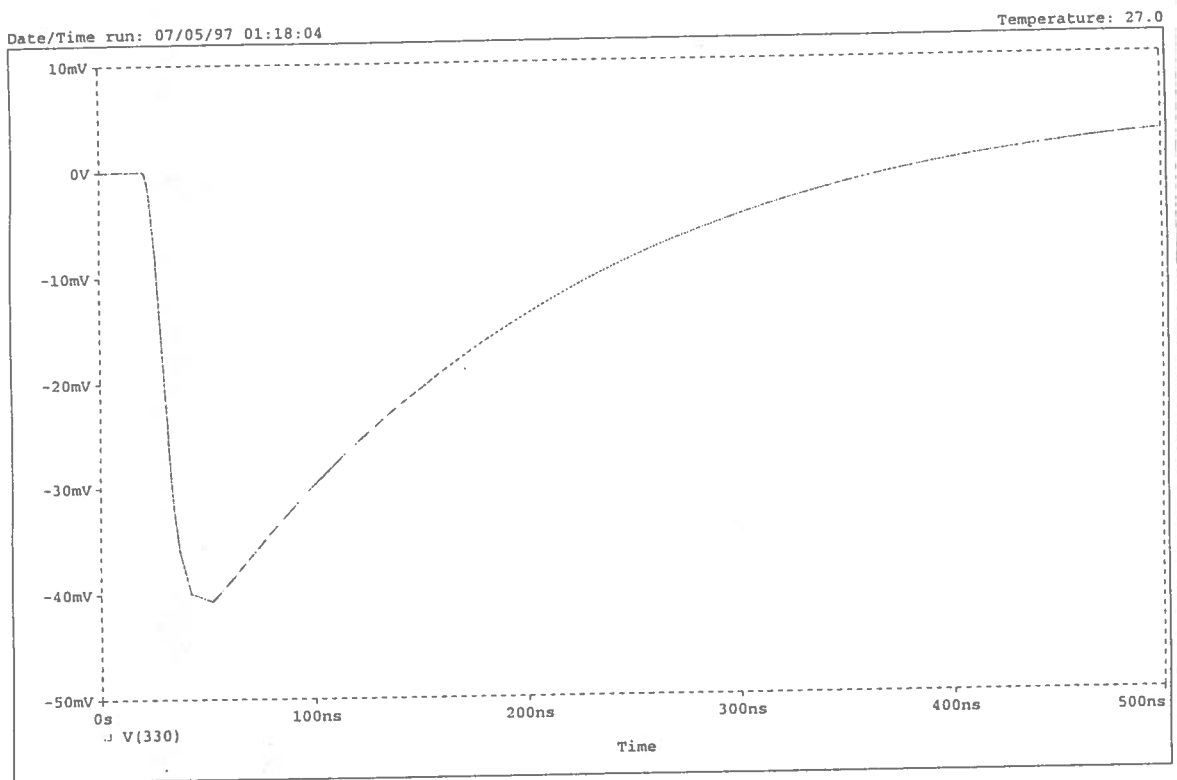


Fig. 7a Hit Pixel Amplifier (HPA) output for $L = 450 \mu\text{m}$ and $C_{\text{bond}} = 50 \text{ fF}$ (see Table 2).

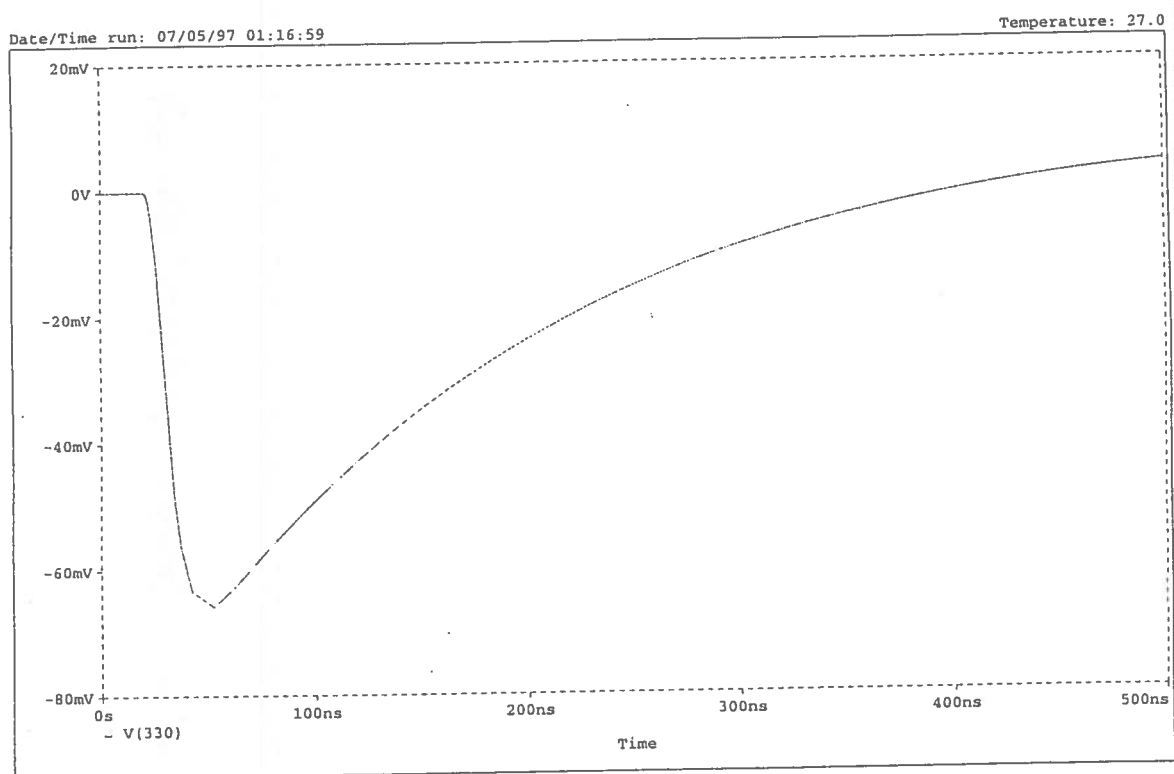


Fig. 7b HPA output for $L = 450 \mu\text{m}$ and $C_{\text{bond}} = 100 \text{ fF}$ (see Table 2).

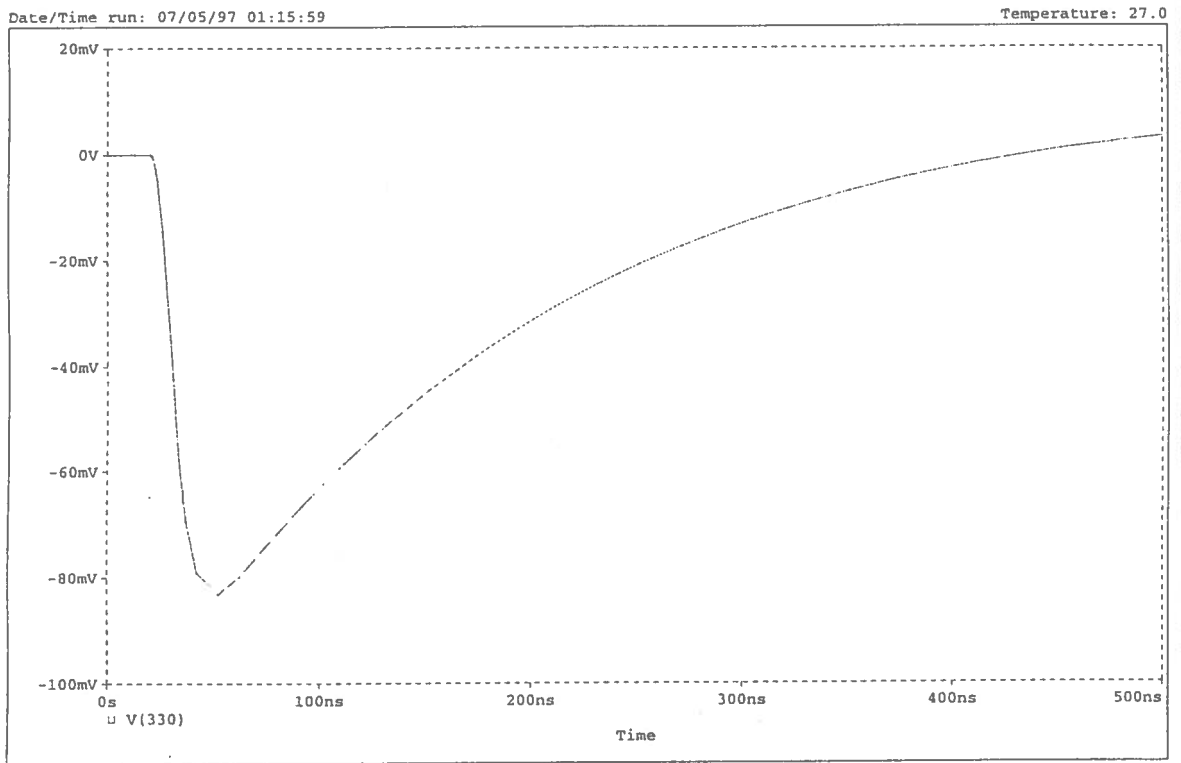


Fig. 7c HPA output for $L = 450 \mu\text{m}$ and $C_{\text{bond}} = 150 \text{ fF}$ (see Table 2).

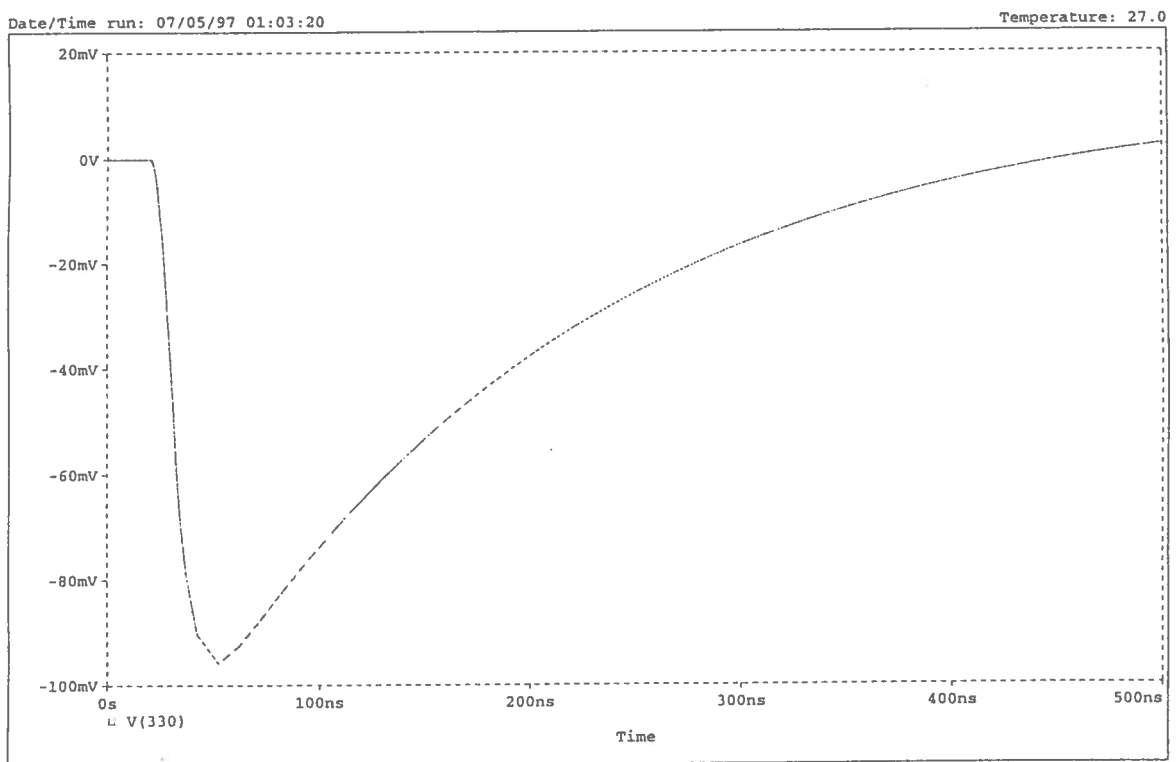


Fig. 7d HPA output for $L = 450 \mu\text{m}$ and $C_{\text{bond}} = 200 \text{ fF}$ (see Table 2).

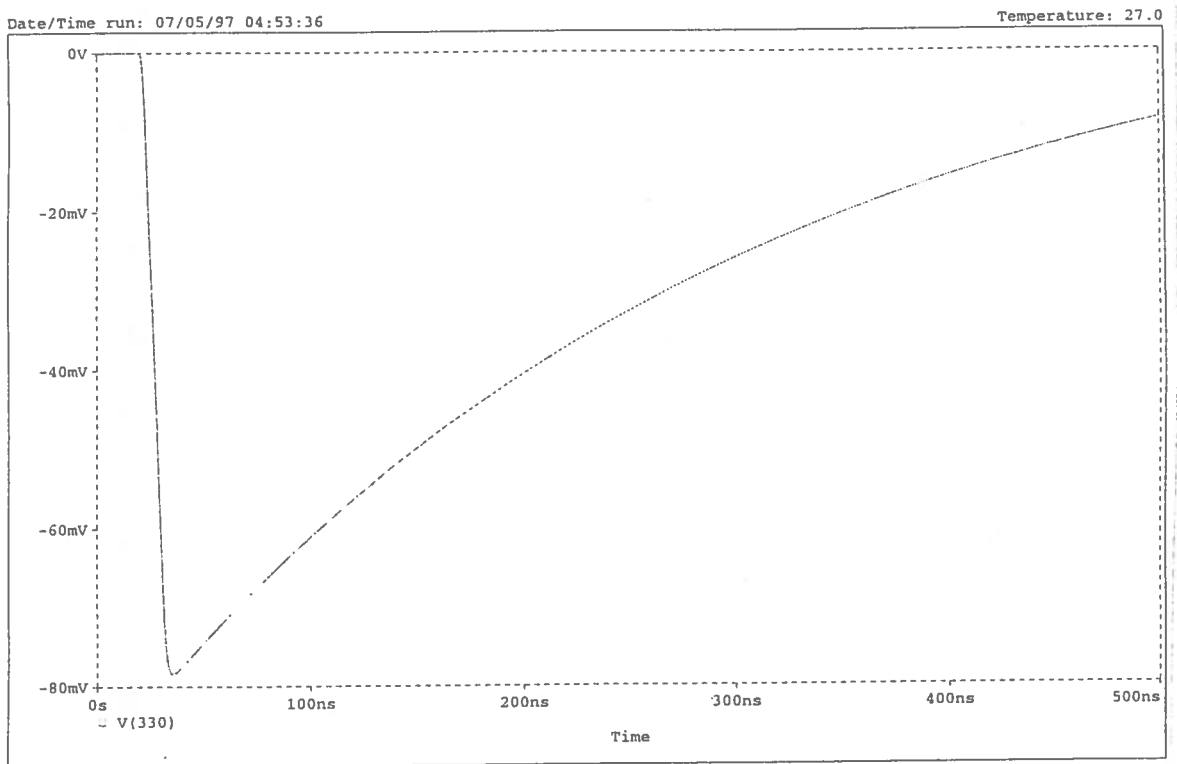


Fig. 8a HPA output for the first of the five cases described in Table 3, $L = 650 \mu\text{m}$.

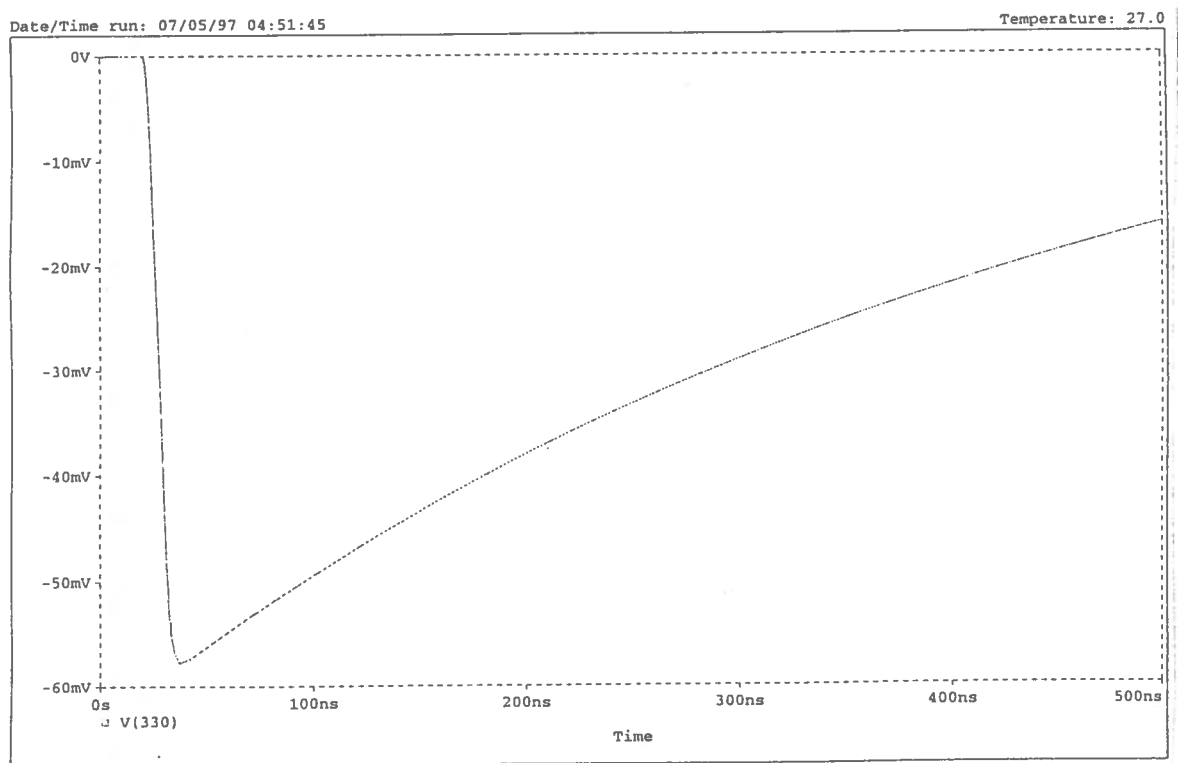


Fig. 8b HPA output for the case $L = 850 \mu\text{m}$ (see Table 3).

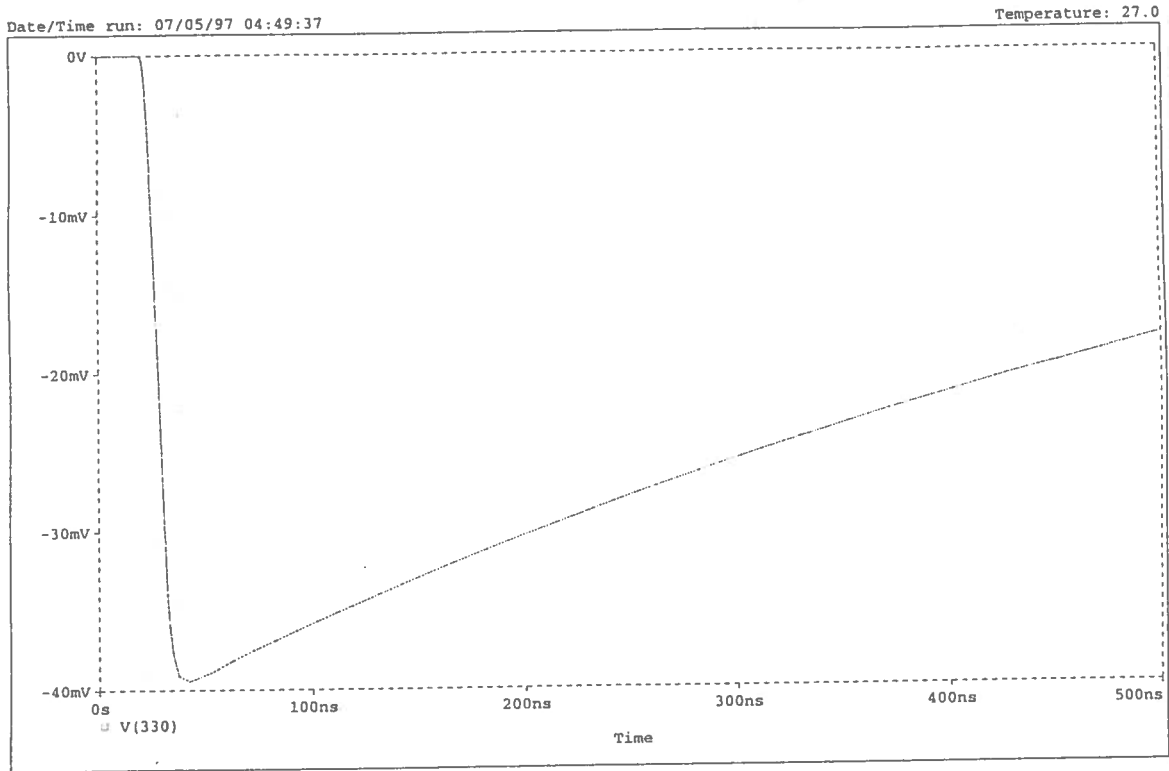


Fig. 8c HPA output for the case $L = 1050 \mu\text{m}$ (see Table 3).

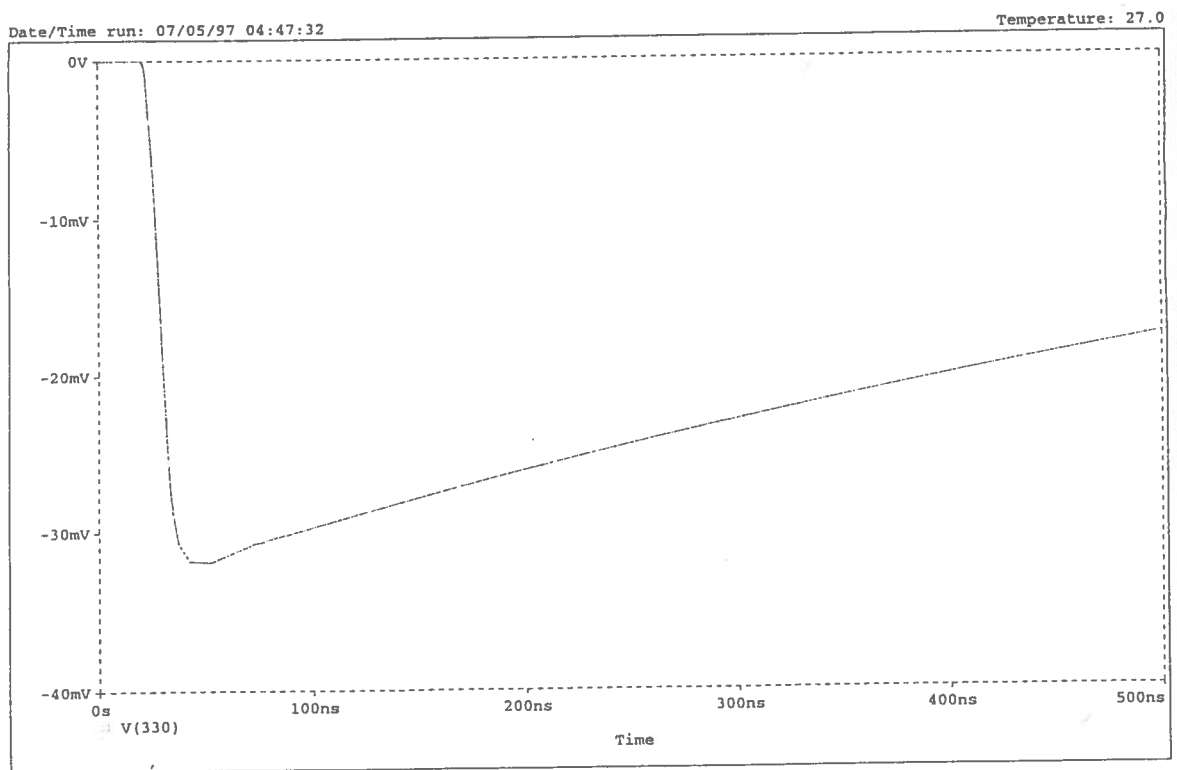


Fig. 8d HPA output for the case $L = 1250 \mu\text{m}$ (see Table 3).

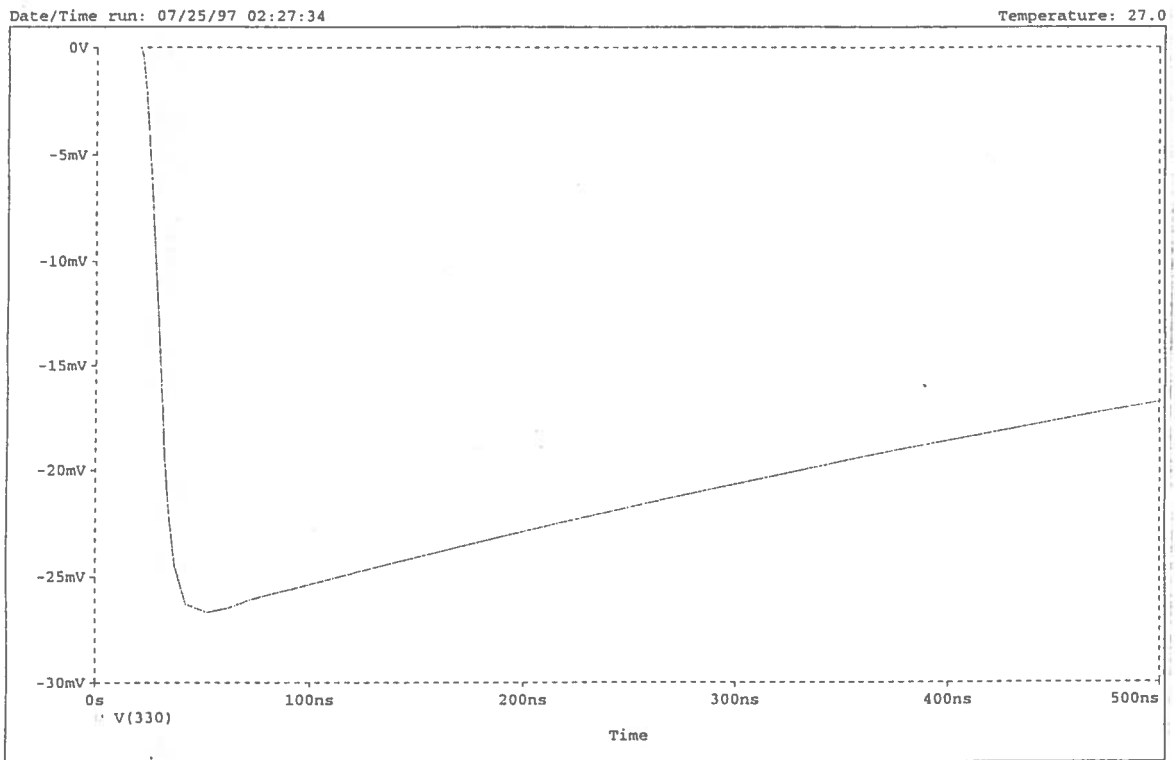


Fig. 8e HPA output for the case $L = 1450 \mu\text{m}$ (see Table 3).

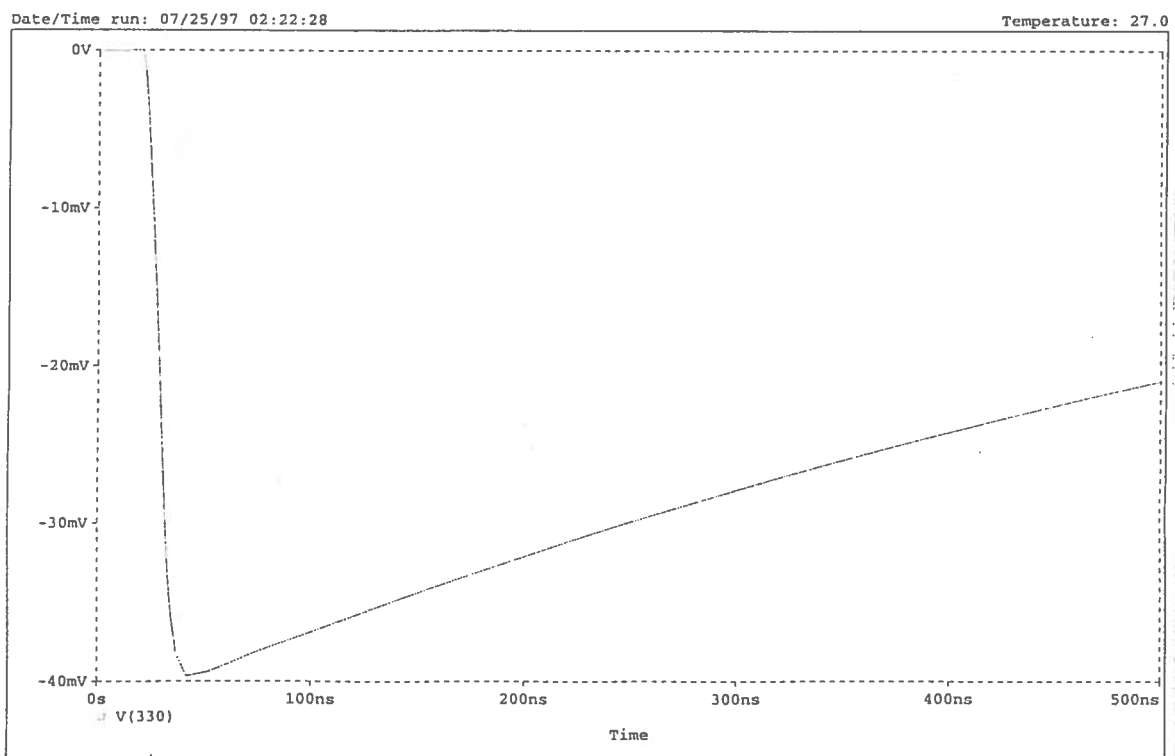


Fig. 9 HPA output corresponding to the situation of Fig. 8e, but with the detector thickness increased from $300 \mu\text{m}$ to $500 \mu\text{m}$. The smaller junction capacitance leads to a better $\text{HPA}_{\text{AC}}/\text{HPA}_{\text{DC}}$ ratio (see text).

One way to partially overcome this effect (as clearly indicated by Eq. (10)) is to increase the detector thickness. Fig. 9 refers to a situation in which the detector thickness has been taken to 500 μm and all other parameters are those of Fig. 8e, i.e. those described in the last row of Table 3. The $\text{HPA}_{\text{AC}}/\text{HPA}_{\text{DC}}$ ratio achieved in this case is 83% , to be compared with the 76% of Fig. 8e; in this case, $(\text{HPA}_{\text{AC}}/\text{HPA}_{\text{DC}})_{\text{ideal}} = 88\%$ thus showing that, again, about 5% of charge is lost on adjacent pixels.

5. Conclusions

An easy and cheap interconnection technique to intrinsically obtain AC-coupling in hybrid pixel detectors has been proposed. It relies on the screen printing of insulating glue droplets onto contact pads of suitable dimensions, followed by a chip flipping procedure. The performed simulations show that this method can be effective, provided that sufficiently large pixels are used together with a proper biasing structure directly integrated on the detector substrate.

A limitation of this method arises from the high junction capacitance that naturally comes into play when considering large (close to 1 mm side) pixels. Since C_j and C_{bond} have the same dependence (proportional to L^2) on the pixel geometry, it is clearly useless to increase the pixel area beyond a certain value, while a viable solution is to make thicker detectors in order to decrease C_j . In this case one should use very high resistivity ($\approx 10 \text{ k}\Omega\cdot\text{cm}$) substrates in order to keep the full depletion voltage at a reasonable value. Moreover, it has still to be experimentally investigated if in environments with high level of radiation (such as LHC experiments), the dielectric properties of the insulating glue do not change in such a way to significantly deteriorate the bonding capacitance.

It has been shown that with the currently available glues and screen printing limits, the critical size to apply this technique is close to $500 \times 500 \mu\text{m}^2$; nevertheless, the proposed method could be a priori applied also to smaller pixels (closer to the screen printing limits) provided that sufficiently high dielectric constant glues were available. This would also practically eliminate any interference of the junction capacitance in the charge balance.

Acknowledgements

The authors would like to thank M. Bari and P. Cristaudo (Electronics Lab. of INFN Trieste) for the use of the PSPICE simulator, and L. Bosisio (University and INFN Trieste) for helpful discussions.

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