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A POSSIBLE DATA ACQUISITION SYSTEM FOR THE BOREXINO EXPERIMENT

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Abstract

A DSP (Digital Signal Processor) on each acquisition board provides the control over all the ADC conversion signals, the temporary storage transfer on VME dual port memory. The DSP also provides low level analysis for photo-multiplier tube calibration.

For each VME crates a Power PC VME master processor assembles and filters the data from twenty acquisition boards.

The system control and the event reconstruction are made by a set of host computers via a local network connection.

INTRODUCTION

BOREXino is a real time detector for low energy solar neutrinos [1], [2], [3], [4], [5]. The BOREXino detector apparatus consists of a spherical vessel (radius 4.25 m) filled with a liquid scintillator (300 tons) and viewed by about 2000 photomultipliers placed on a larger spherical surface (radius 6 m).

The photomultipliers are expected to operate in single or few photoelectron regime.

The master trigger signal is generated when there are at least 10 photomultipliers hits within a time window of about 50 ns [6].

The acquisition electronics provide an event energy measurement and an accurate measurement of the arrival time of photomultiplier pulse better than 400ps.

The timing is used to obtain a precise identification of the scintillation position inside BOREXino vessel.

The first processing of the photomultipliers signals is performed on the front end boards.

The acquisition module is a 6U VME slave and has eight acquisition channels with a dead time of about 100ns.

An acquisition modules VME crate will have a VME master Power PC and twenty-one acquisition modules. The total number of the VME crates will be about fifteen. The several VME master Power PC will work in parallel and run the operating system lynxOS with a C language compiler.

There are several advantages of this design. First, VME is widely used commercial digital bus so maintenance and supporting hardware are easily available. Second there are different vendor of lynxOS Power PC interfacing with VME. Finally, the DAQ system is very modular and is independent of VME crates number.

DSP FUNCTIONS ON THE ACQUISITION MODULE

A Digital Signal Processor (DSP) controls the main acquisition module functions and the data transfer on the VME bus trough a 32 bit dual port RAM.

When a master trigger signal occurs, the DSP receives an interrupt signal and a master trigger number from the trigger generator module. Then the DSP must performs the interrupt routine reading the data temporary stored in the FIFOs of each channel and building the local event on the dual port RAM labelling the data with their master trigger number.

After writing the trigger event on the dual port RAM, the DSP sets a flag to give VME master Power PC the indication of the data writing end and waits for a VME master Power PC flag in return giving the indication of the data reading end.

The VME master Power PC can also control the main logical functions of the VME slave acquisition module with some flags handshaking protocol:

. programming the threshold of the discriminators;
. programming the voltage references of the fADC;
. opening and closing the acquisition channels;
. asking a energy histogram of a particular channel;
. resetting the GRAY counters;
. resetting the DSP.

In this way, the local master VME can control the BOREXino detector apparatus and send supervisor host a warning message in case of some failure.

When the master trigger signal doesn't occur, the DSP reads from single channel FIFOs only the energy data and builds the energy histogram to control the photomultiplier gain. This histogram is written by DSP on dual port RAM and is read by the VME master Power PC. When the DSP writes the channel histogram in the dual port RAM, it sets a flag giving VME master Power PC the indication of the histogram writing end on the dual port RAM.

The DSP doesn't write another channel histogram if the VME master Power PC doesn't give the indication of the histogram reading end.

MASTER VME TIMING ACCESS TO DUAL PORT RAM TROUGH VME BUS

When the VME master waits for the DSP histogram writing end flag or the master trigger data writing end flag in return on the dual port RAM, it performs a polling on the bus VME causing

successive 32 bit accesses to VME bus.

When the master trigger signal occurs, the VME master Power PC must perform read cycle addressing whole dual port RAMs on VME bus and look for the master trigger flags written by DSPs of single module acquisition. If the VME master Power PC finds a high master trigger flag in a dual port RAM, transfers whole trigger data and writes the reading end flag.

The time spent by the VME master Power PC to finish the data transfer operation on VME bus depends on the number of acquisition modules to supervise.

The data acquisition system can be organised with only one master VME Power PC for whole acquisition modules or with a master VME Power PC for each VME crate. In the first case, the handshaking and the acquisition data must go trough a vertical bus to the master VME Power PC.

Since a 1MeV energy event corresponds to 10% photomultipliers fired, the VME master Power PC must transfer the master trigger data of two hundred photomultipliers in the case it is supervisor of two thousand photomultipliers and must transfer the master trigger data of 16 photomultipliers in the case it is the supervisor of only one crate VME.

In both cases, there will usually be one master trigger data corresponding to three 32 bit words on each dual port RAM.

The VME master generally performs five 32 bit read cycle on the VME bus for each dual port RAM to transfer one master trigger data from a dual port RAM on the VME bus: one read 32 bit cycle to look for the writing end flag of the master trigger data, three read cycle to transfer the master data and one write cycle to give DSP the indication of the master trigger data reading end.

If the VME master Power PC is the supervisor of only one VME crate corresponding to twenty acquisition modules, it must perform twenty 32 bit VME read cycles to look for master trigger data flags, forty-eight 32 bit VME read cycles to transfer the master trigger data and sixteen 32 bit write cycles to give DSP the indication of master trigger data reading end.

Since a typical VME address strobe cycle lasts about 1.65μs, the VME master Power PC spends 138.6μs to transfer a master trigger data on VME bus. That corresponds to an event rate about 7kHz.

If the VME master Power PC is the supervisor of whole two thousand photomultipliers, the VME 32 bit access timing will be most than 1.65μs because the several VME crates will be connected by a vertical bus. In this case the single VME read/write cycle is about 3μs.

When a master trigger signal occurs, there are two hundred dual port RAM with one master trigger data. Then the master VME Power PC must perform about two hundred and fifty 32 bit read cycle to look for the master trigger flag, about six hundred 32 bit read cycle to transfer the data trigger and two hundred write cycle to give DSP the indication of the master trigger data reading end. The VME master Power PC will spend about 3150μs corresponding to event rate about 320 Hz.

Since a dual port RAM usually has only one master trigger data, the data block transfer cannot determine a strong decrease of the timing accesses on the VME bus.

Trigger Universal timing, time elapsed from the last trigger, number of trigger data and so on.

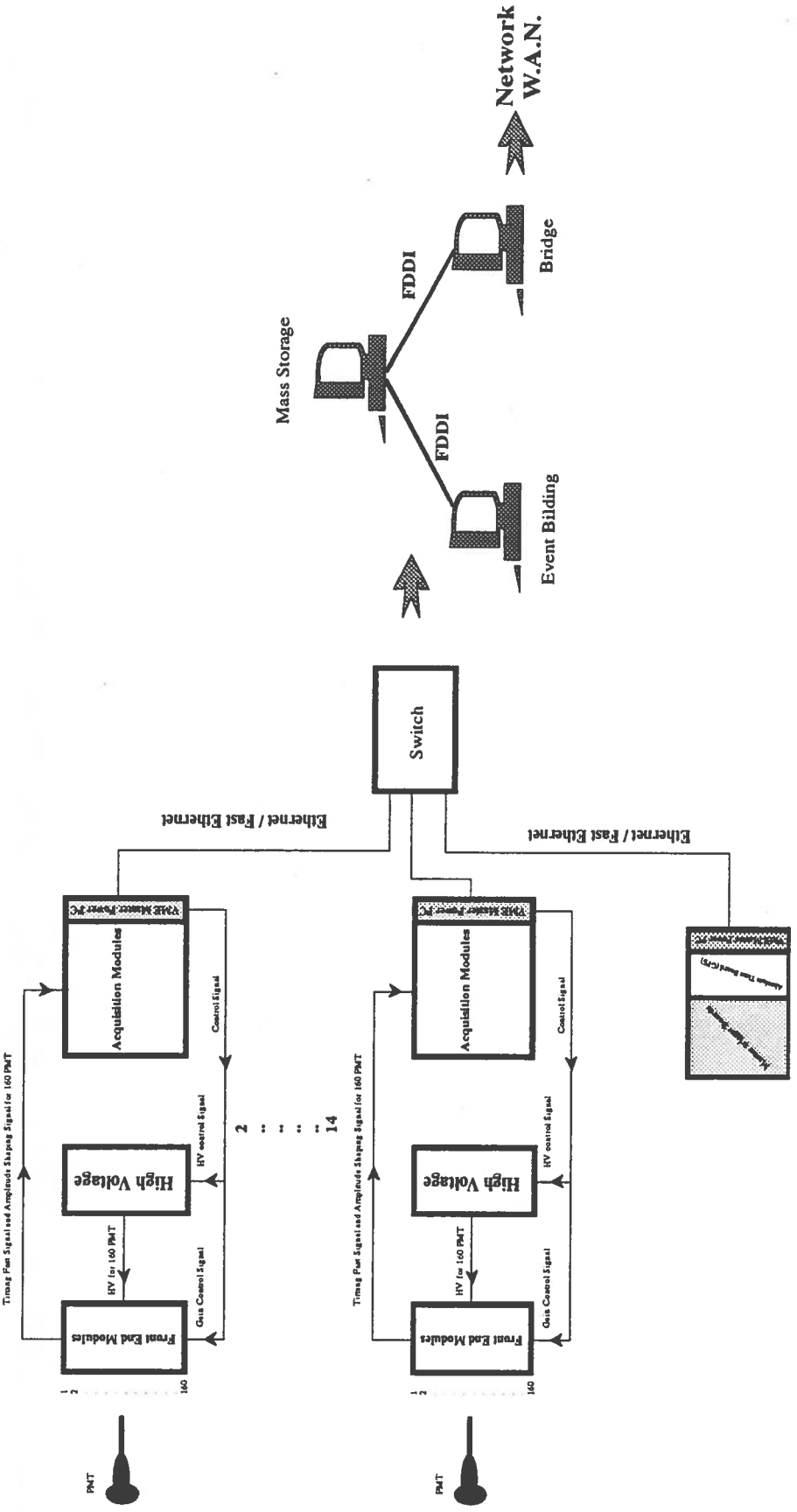

Figure 1 – A possible data acquisition system structure for the BOREXino detector apparatus.

A POSSIBLE DATA ACQUISITION SYSTEM STRUCTURE

The Figure 1 shows a possible data acquisition system for the BOREXino detector apparatus.

In each VME crate is located one Power PC providing the service for twenty acquisition modules. When the trigger signal occurs, the VME master Power PC transfers the data from the dual port RAMs and stores them in its local RAM.

Each local Power PC also provides the gain stabilisation of the photomultipliers.

The fifteen acquisition VME crates send an work-station their data via Ethernet/fast-Ethernet link. This link has a star-like structure using a digital switch as concentrator.

The work-station host collects the data from the VME crates via this local network and builds the master trigger data event storing on its mass storage.

In this local network more than one work-station can be connected allowing different parallel data analysis or sharing the DAQ control programs of the electronics and the fast data analysis and/or graphics.

The access from the external world is limited by a digital bridge.

The higher modularity of this structure allows a easy setting up the BOREXino detector apparatus.

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