ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Napoli

INFN/TC–97/21
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SIS–Pubblicazioni
dei Laboratori Nazionali di Frascati

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A TRANSIENT VOLTAGE PROTECTION NETWORK FOR ECL DATA TRANSMISSION

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Abstract

In this note we describe a transient voltage protection network for an ECL differential data transmission. We show how this network allows a Data Transmission frequency beyond 15 MHz over a 7 m distance.

1. INTRODUCTION

Voltage transients result from the immediate release of previously stored charges [1]. An electrostatic discharge (ESD) occurs each time two objects at different potentials come in direct contact, either voluntarily or accidentally. While the process of electrostatic charge generation can take many forms, some ESD models [2], [3], [4] have been developed to standardize the classification of the integrated circuits. In all models a simple RC charge mechanism (R=10 MΩ; C=20÷200 pF) is employed. Discharge is modeled either with an RC network or by an RLC network.

Whatever the transient generator may be, the failure mechanism of the integrated circuits is always due to an overvoltage stress on the input stage. Even a short transient of a few microseconds can cause the input stage to fail catastrophically.

In this note we describe a protection scheme which has proven to be effective in protecting a twisted pair ECL differential connection which randomly experienced induced spark transients with amplitudes in excess of 500 V.

2. THE FIELD ENVIRONMENT

The front end electronics of many experiments often is inaccessible. Power supply distribution networks often dictate for power supplies very far from front end cards. Moreover, to keep complexity of front end electronics to a minimum, the number of channels which are brought to the Readout electronics with the modern high energy experiment is very high. ECL data transmission is often preferred due to the high speed of the interconnection. ECL differential data transmission is currently employed for distances under 10 m in the frequency range above 10 MHz. Differential transmission of data is a must since any noise coupled into a twisted pair generally appears equally on both sides and the receiver, being differential, cancels it. To transfer data two old workhorses, an MC10124 on the transmitting side and an MC10125 (or F100325) on the receiving side, which also provide the interface with the more common TTL world, are still used.

An architecture such as the one depicted in fig.1 is often employed to transmit data at 15 MHz (or above) up to an 8 m distance. Power supplies are generally near the Readout electronics and thus located 8 m away from the front-end electronics. Due to the long distance, the ground and the power supply distribution layout are rather hostile.

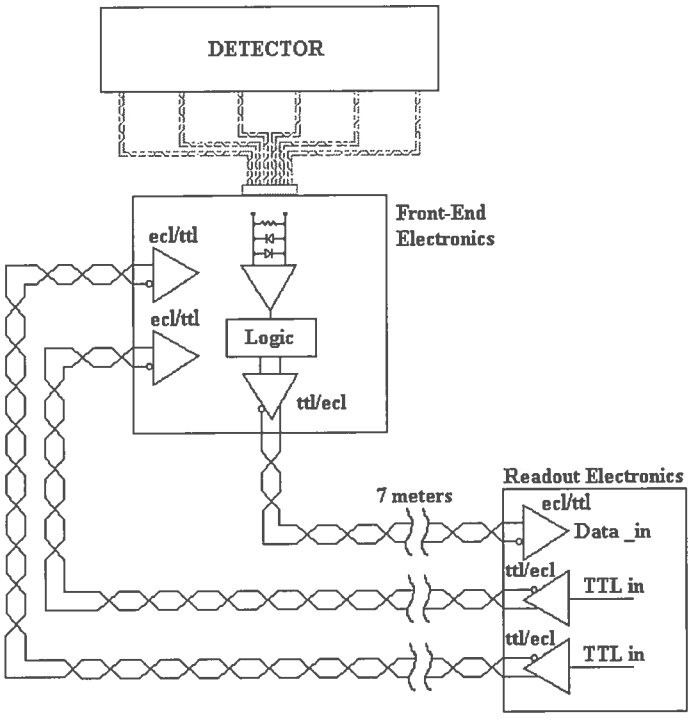

Fig. 1 - A possible electronic environment.

The ECL interface works very reliable provided that the interconnection is not subjected to electrical over stress. However if the electrical "noise" injected onto the interconnections is higher than the maximum common mode voltage of the receiver some devices may fail.

In general, bench testing on the pins of the failed driver reveals that only the outputs

connected to the line receiver fail. The other unused driver's output and the input pins in general show no damage. The same applies to the receiver. Moreover, for "moderate" noise energy the line driver simply shift the output levels from -0.8/-1.6 up to -2.2/-2.8 V. Even with these shifted levels the MC10125 line receiver is able to furnish a correct TTL output with little loss of pulse fidelity.

Indeed, a high frequency interfering electrical voltage can cause much damage. At very high frequencies, wires become transmission lines, resistors behave like resonant circuits, capacitors become inductors and inductors become capacitors. As a result, the front end electronics can experience a sudden increase of the voltage with respect to the ground of the Readout electronics. These voltage transients can be by far in excess of the absolute maximum ratings of the transmitter/receiver couple and some failure or degradation of performance can be observed. The failure mechanism leads to junction damage, surface charge accumulation and even to conductor fusing. For moderate injected voltages, increased leakage and reduced performances are typical. However damage is often cumulative: once reduced performances are observed, then the device is on the way to failure.

We have experienced random failures of the driver/receiver couple for a high energy physics experiment. In order to identify the offending ESD a TDS744 was armed with the trigger at -254 V. The observed waveform was as follows:

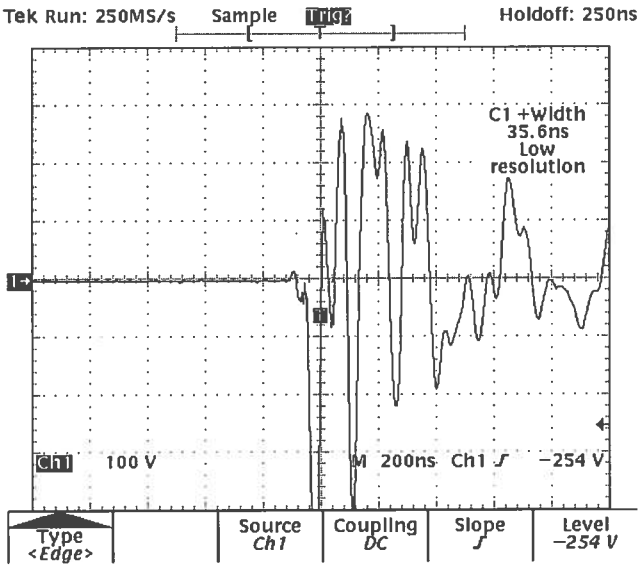

Fig. 2 - Detected transient voltage.

3. INDUCED DISCHARGE ON THE MC10124/MC10125 INTERCONNECTION

To simulate an offending ESD onto the interconnection we have built a prototype made up of two plexiglas planes (30×30 cm^2). The external sides were sprinkled with graphite. The distance between the planes was fixed at 2 cm. The "chamber" capacitance was 150 pF. An aluminum plane was placed underneath. The ground of the MC10124 was connected to this "antenna" plane; at the input of the IC an isolated oscillator provided a TTL pulse.

Once the capacitor has been charged at 8 kV via a 20 MΩ series resistor, we manually

shorted the high voltage via a two meters high voltage cable directly at the input of the high voltage connection of the "chamber" producing discharges with arcs wider than 4 mm.

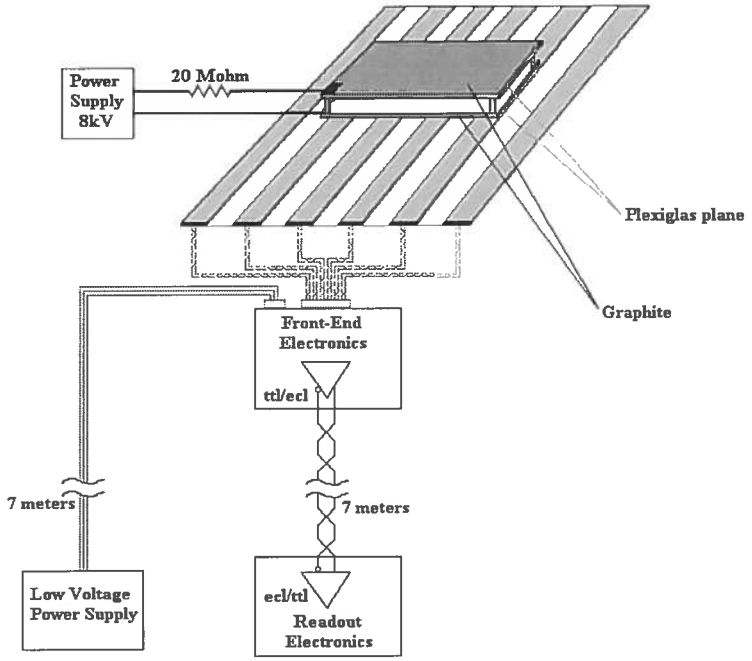

Fig. 3 - ESD model set up.

Despite the question as to how far this model simulates an effective physical phenomena, the electrostatic discharge is certainly the same. The "chamber" capacitor first charged up to a voltage of 8 kV and thereafter discharged via a two meters high voltage cable (for safe operation), so as to assure a short discharge time and to produce a great amount of electrical injected noise. The induced pulses referred to ground at the end of the 7 m twisted line at the input of the receiver were as follows:

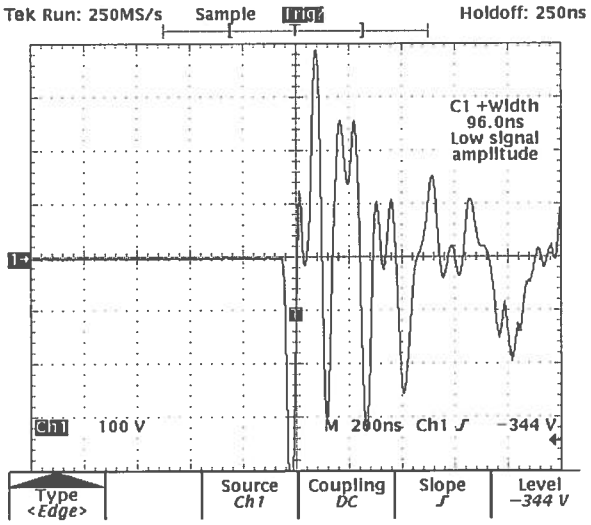

Fig.4 - "Noise" at receiver input.

A typical discharge event lasts 4 µs; spikes are well above 500 V and oscillations are in the order of 100 ns. A driver/receiver couple such as the MC10124/MC10125 cannot withstand these high spikes and in fact they normally fail after some sparks.

4. THE SP721 TRANSIENT SUPPRESSOR DEVICES

There can be many different ways to protect an integrated circuit onto a board. These include on chip ESD protection, TSV diodes and even protected connectors.

Two types of transient suppressor devices do exist: "attenuator" and "diverting" devices. The former attenuate spikes preventing their propagation to the sensitive device, while the latter divert transients thus limiting the residual voltage. The SP720 protection array [5] belongs to the second group and is made up of an array of SCR/Diode structure with 14 inputs (SP720, Fig.5).

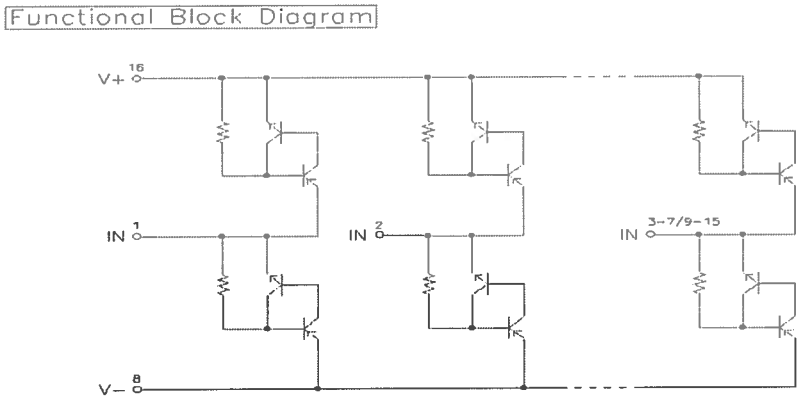

Fig. 5 - Harris SP720.

The SCR structure is designed to trigger at one V_{be} drop above V^+ or at one $-V_{be}$ drop below V^-. Each time one input line experiences a transient voltage above the threshold referred to above, a quick clamp action takes place limiting the transient voltage. The input switching speed of the SP720/721 devices is very good as it is a mere 6 ns and further they can withstand input peak currents up to ±2 A.

5. ESD PROTECTION IN ACTION

The most effective method to protect a transmitter/receiver network is depicted in Fig.6.

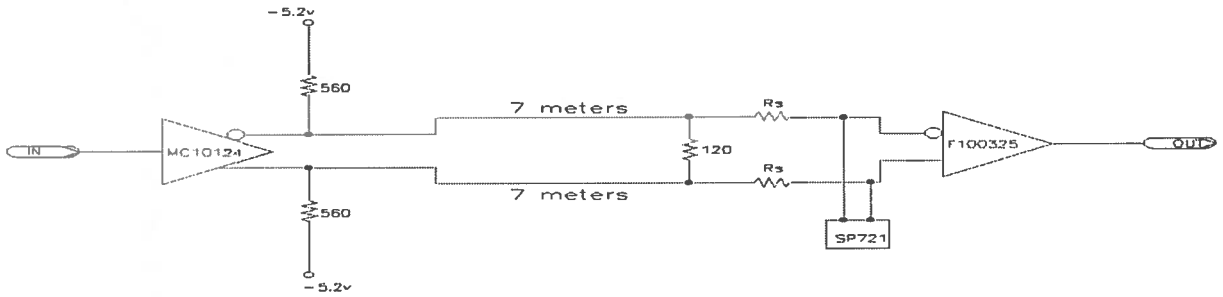

Fig. 6 - Protection network.

This scheme, with proper selection of the Rs value works either with "hot plugging" ie. insertion and removal of input/output connectors while the supply voltage is on and with ESD. The series protecting resistor limits the current while the SP720 limits the voltage at the input of the receiver so that the input voltage seen by the receiver never rises above the absolute maximum rating. The series resistor also helps in minimizing the input current to the receiver during the latching of the SCR network. The protection network as in figure 6 with Rs=1 kΩ and SP720 works as follows:

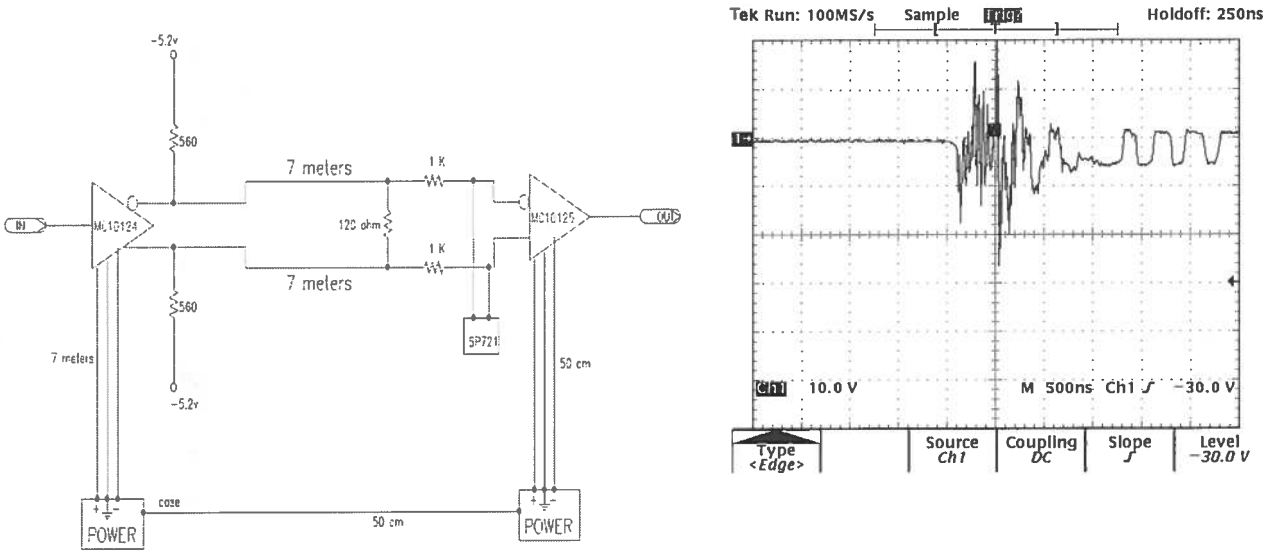

Fig.7 - Protection network in action.

The input voltage at the receiver does not exceed the absolute maximum ratings.

6. THE CHOICE OF THE SERIES PROTECTING RESISTOR

Clearly the protection circuitry does influence the characteristics of the interface. The series resistor lowers the voltage swing at the receiver input while the protecting device due to its parasitic capacitance slows down the signal slew rate and hence the maximum operating frequency. Furthermore different protection devices could exhibit slight differences in the parasitic capacitance leading to added skew.

To choose the optimum series resistor a good knowledge of the behaviour of the input stage of the receiver would be necessary. Unfortunately, many manufacturers do not provide details regarding the input stage or the behaviour of the input stage to an overvoltage stress. The receiver input impedance generally has a non linear characteristic and so it is not possible to specify it by a single resistor value. Typical values are about 10 kΩ.

Since two different driver/receiver networks can be used, we will investigate each of these interfaces suggesting different values of protecting resistors.

a) MC10124/MC10125

The MC10124/MC10125 network in absence of the protection circuitry exhibits very little pulse aberration due to the superior characteristics of the ECL components where propagation times are specified to be the same. Therefore for the MC10124/MC10125 couple we have performed timing tests with a larger than necessary 1 kΩ protecting resistor in the aim to magnify any skew in the parasitic capacitance of the protecting device, as this had to reflect into aberration of the pulse fidelity at the output. In the following graph we see that the jitter introduced by a bunch of 40 SP710 protection devices is within 1 ns (input pulse width of 31 ns).

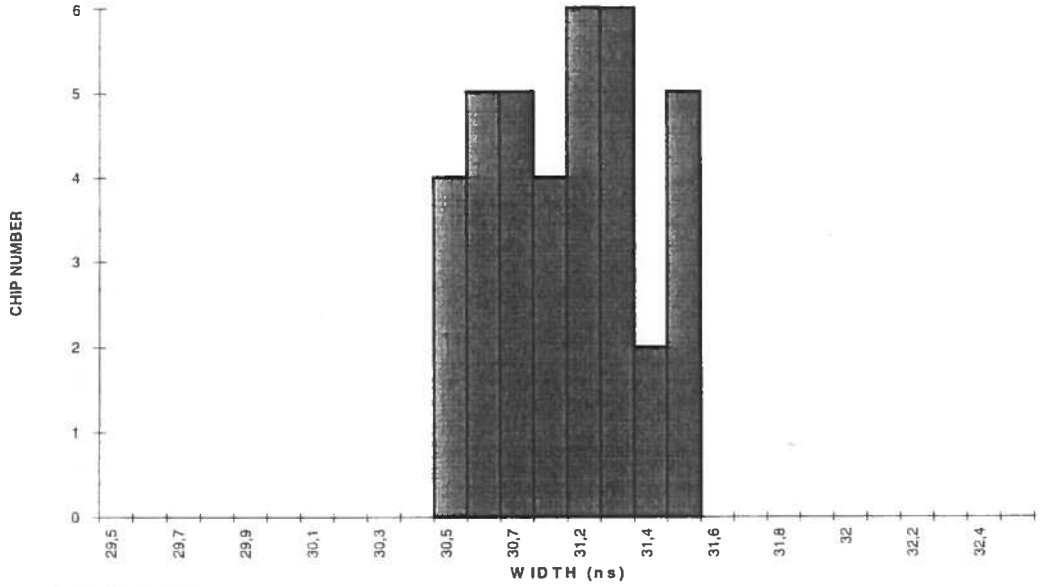

Fig.8 - Pulse fidelity as a function of different SP720.

b) MC10124/F100325

The behaviour of the MC10124/F100325 is somewhat different as the maximum series resistor allowed here reaches 270 Ω. First, the protecting circuitry has been tested to the sparks with a limiting resistor of 22 Ω. The network withstood to more than half an hour of continuous sparks without apparent damage. Timing tests were then performed with the series limiting resistor ranging from 22 Ω up to 270 Ω. The interconnecting cable was 7 m long.

Obviously, pulse fidelity is better preserved with lower values of the protecting resistor, while on the contrary the best protection is obtained with the largest value. We have tested the circuit with three different input pulse widths 10, 20 and 30 ns. In the following graph we show how pulse fidelity is achieved up to 10 ns with a protecting resistor value in the 22 ÷120 Ω range.

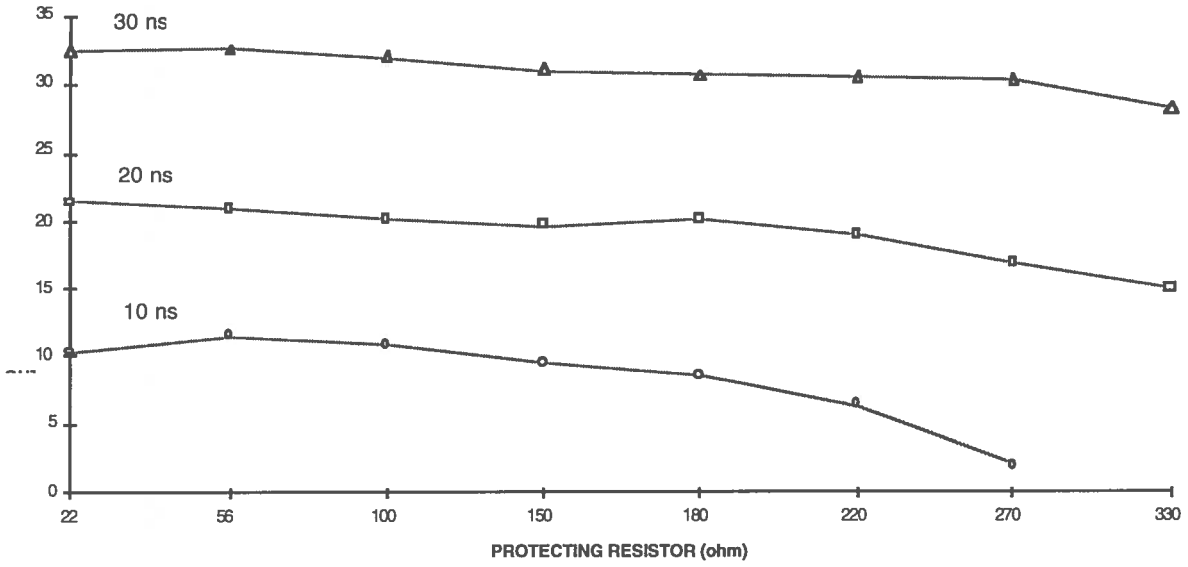

Fig. 9 - Output pulse width as a function of protecting resistor.

7. CONCLUSIONS

In this note we have outlined the behaviour of a protection network against ESD damages. The network has proven to work faithfully even with offending ESD in excess of 500 V.

REFERENCES

[1] ESD Association Draft Standard DS5.3 for Electrostatic Discharge (ESD) sensitivity Testing - Charged Device Model (CDM) component testing. ESD Association Inc., 200 Liberty Plaza, Rome NY

[2] MIL-STD- 883 Method 3015, Electrostatic Discharge Sensitivity Classification. Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA 19111-5094.

[3] EIAJ ED-4701 Test Method C-111, Electrostatic Discharges, Japan Electronic Bureau, 250 W 34 th St.., New York 10119

[4] ESD Association Standard S5.2 for Electrostatic Discharge (ESD) Sensitivity Testing- Machine Model (MM)- Component Level ESD Association Inc., 200 Liberty Plaza, Rome NY

[5] HARRIS Transient Voltage Suppression Devices, 1995