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Abstract

In this note a positive strip readout card developed to serve 16 input channels of RPC detectors is described.

1. INTRODUCTION

Resistive Plate Counter detectors (RPC) [1-2] are widely used in high energy experiment. Induced pulses are read by planes of strips. Pulse polarity, depending on the position of strips respect to the H.V. planes can be either negative or positive. This note describes the positive front end card (PFEC) we have developed for the BaBar [3] experiment to perform first stage processing of the positive induced pulses of the RPC.

The main requirement posed to the PFEC was relative to the cost which had to be kept low due to the large number of channels (about 50,000), while a fault tolerant design was of the utmost importance.

To reduce the total number of cards, keeping reasonable the overall costs, we have opted for a design where each PFEC handles sixteen input channels. Next, the reliability of the card has been carefully analyzed so to reduce the mean time between failures (MTBF) to a minimum since the cards had to be positioned close to the detector and therefore not directly accessible [4]. Further, use of SMD components was a must since, to avoid signal degradation, the cards had be installed within the iron gaps of the subdetector.

Threshold stability, good inter-channel characteristics, with low crosstalk and a time walk of 2 ns for input pulses above the typical RPC pulse, were important design goals, while - obviously- power supply requirements had to be kept at a minimum.

Actually the card is mass produced and results are satisfying.

2. PFEC DESCRIPTION

Strips data are connected to a sixteen input discriminator bank acting as an interface between the analog strip world and the more ideal digital world (Fig.1). The outputs of the discriminators are connected both to a dual bank of monostables and to a PLD programmed to achieve a FAST-OR of the board. The dual bank of monostables, hooked for 11.3 and 13.7 μs pulse widths, provides for strip pulse stretching thus keeping memory of the hit during trigger latency. A time window of 2.4 μs at the far end of the outputs width is set up and - by latching the sixteen strip status only in this time window - a factor of 5 in noise reduction is achieved. Latching of the monostables status into the MACH210AQ-15 PLD, programmed to behave as a shift register parallel in serial out, is assured by the SHIFT/LOAD signal (active high) and by the first low to high transition of the CK_CHAIN signal (a pulse train of sixteen pulses). On the first CK_CHAIN pulse, with SHIFT/LOAD signal high, strip no.15 is output; then, with SHIFT/LOAD signal low, strip no.14 follows and so on.

ECL differential data transmission to the following electronics was chosen both to obtain a high transfer rate and to achieve a good noise immunity.

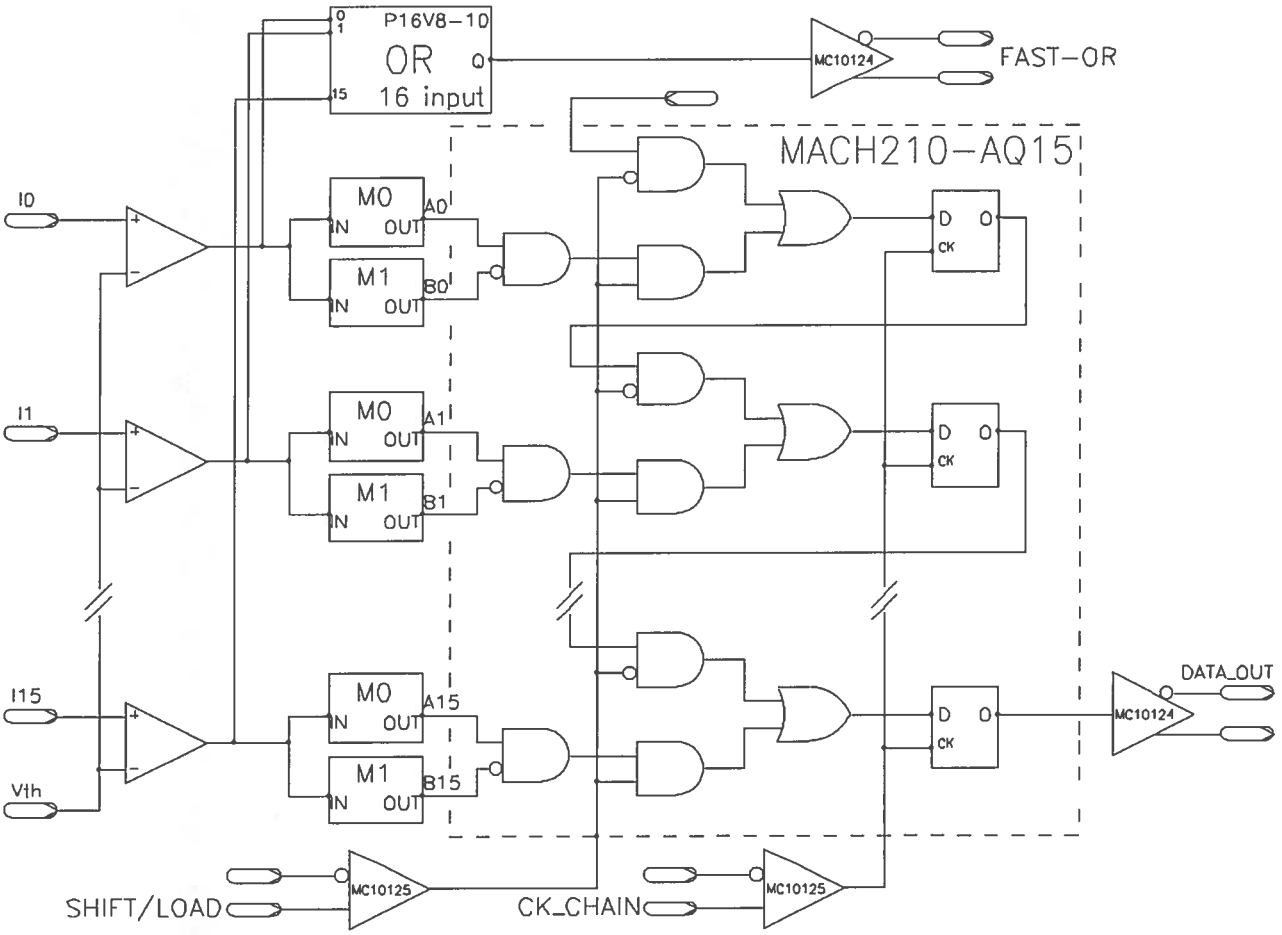


Fig.1 - PFEC Functional Block Diagram.

3. PFEC INPUT STAGE

The input stage of the PFEC consists of 16 atypical discriminators where a two stage RF amplifier (two BFS17, with a gain above 100) feeds a fast TTL buffer (74F244), as shown in Fig.2. This works well as the amplitude input spectrum coming out from our RPC is not continuous and even does not start at zero. In fact, the RPC is a low noise detector with an S/N (signal to noise ratio) better than three. Working in streamer mode, minimum pulse charge is about 100 - 150 pC, depending on the gas mixture, with rise time in the order of 2 - 4 ns and amplitude of the order of 300 mV. Noise can be injected into a strip only via a crosstalk mechanisms induced by adjacent strips.

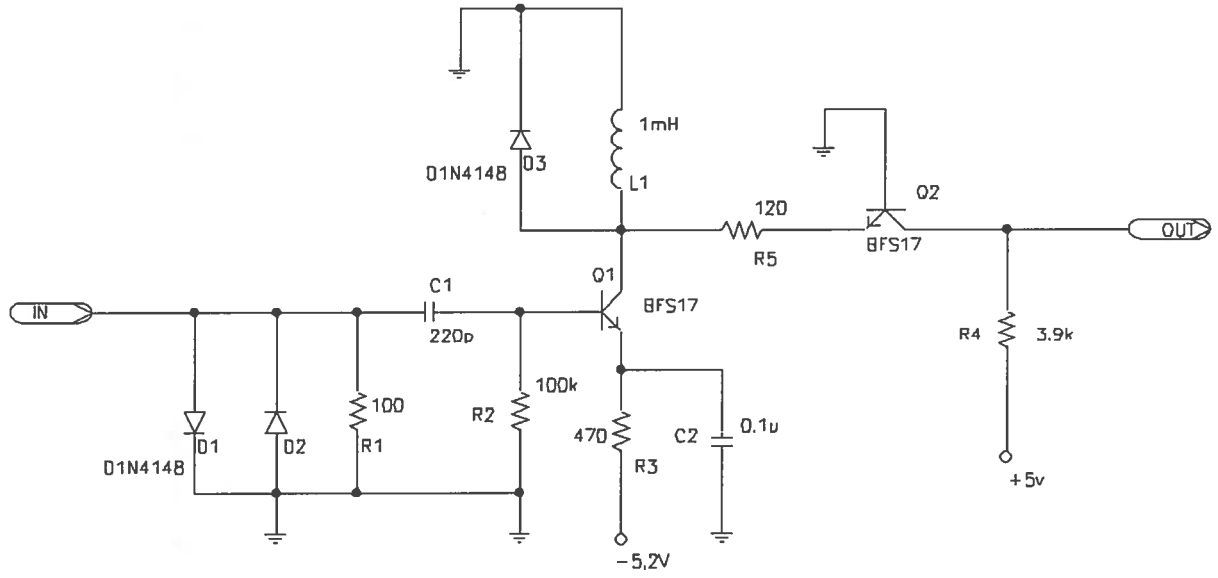


Fig. 2 - PFEC Input Stage.

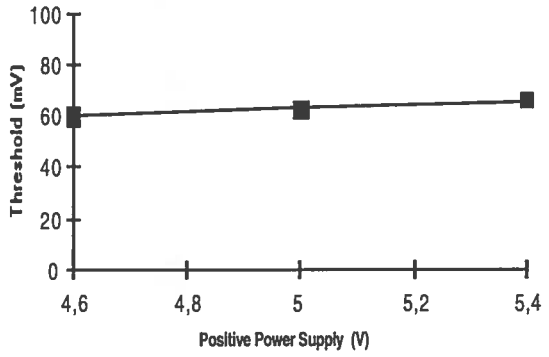
Strip signals shaped by two diodes (D_1 & D_2 1N4148) are then connected to the common emitter input stage via the C_1 capacitor (220 pF). The base resistor R_2 fixes the quiescent current of the Q_1 input transistor. In this design (R_2=100 kΩ) the quiescent current of Q_1 is fixed at about 1 mA. That way voltage at the collector of the Q_1 transistor is due to the DC resistance of inductor L_1 and is about 20 mV. The inductor L_1 on the collector of Q_1 is inserted both to achieve a large gain for typical RPC pulses (for this stage gain is above 50) and to hold collector voltage near zero. R_3 resistor is inserted both to assure a minimum of feedback at DC and for protection purposes so that -should a transistor fail going short from collector to emitter - the current requested would increase of a mere 10 mA. The high frequency behaviour of this transistor is not influenced by R_3 resistor.

Transistor Q_2 is hooked in a common base configuration, with the base at ground. Normally is at cut-off and is brought into conduction whenever collector voltage of Q_1 rises above its cut-in voltage. In the quiescent state, biased at 1 mA, Q_1 collector sits at about 20 mV, well below the cut-in voltage of the Q_2 transistor.

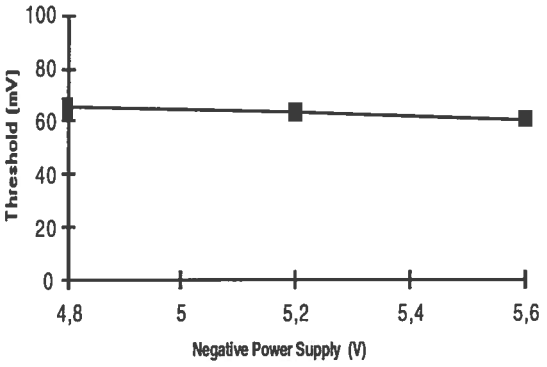
To achieve a low TTL voltage at the output of the Q_2 transistor, its collector's voltage must go down to V_{IL}= 0.8 V. The 74F244 acts as a buffer with a built in hysteresis and a threshold uncertainty of 1.2 V. The threshold uncertainty referred to the input is a mere 12 mV since the gain of the input stage for RPC pulses is about one hundred. This uncertainty is fully acceptable provided that threshold is lower by a factor of 2 in comparison with a typical RPC pulse. In our design we have chosen to be conservative as threshold is lower by a factor of 4 (for our RPC detector the minimum pulse charge is 100 pC).

4. SIMULATIONS

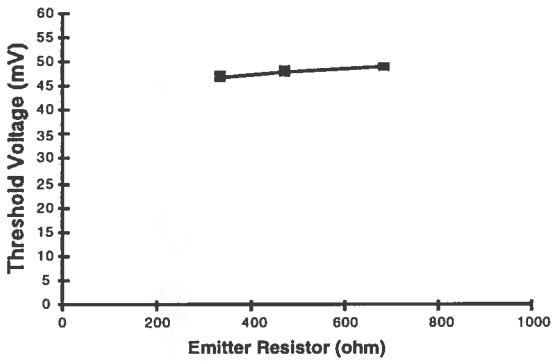
Before starting the PCB, the input stage behavior has been thoroughly investigated to ascertain the threshold sensitivity to power supply, to different pulse widths and to Q_1's inductor value.



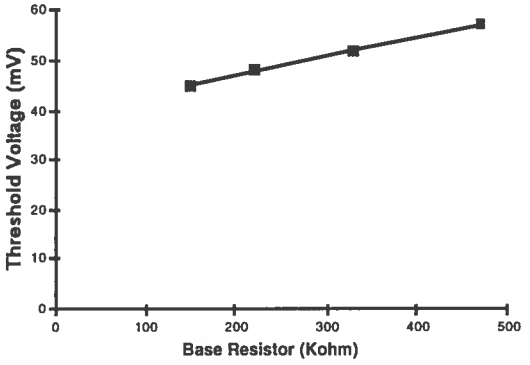
3a



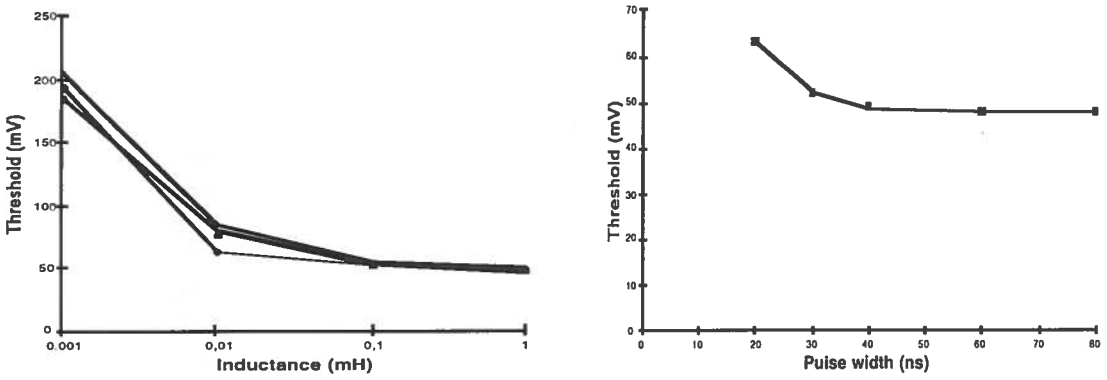
3b



3c



3d



3e **3f**

Fig.3 - Threshold simulations as a function of different parameters.

In the first two graphs (Fig.3a and 3b) threshold sensitivity against power supply both positive and negative is shown. Then threshold as a function of Q_1 emitter resistor and Q_1 base resistor is presented (Fig.3c and 3d). Simulations with different values of Q_1 collector's inductor play an important role since the boards, inside the iron gaps, could experience a residual magnetic field which in turn could cause a slight change of the inductor value. Simulations in Fig.3e demonstrate that for a two orders of magnitude variation of the inductance there is a negligible effect on threshold and that even for a 3 orders of magnitude variation results are still acceptable. Three values of parasitic Q_1 collector capacitance (5 pF, 10 pF, 20 pF) are included. Fig.3f displays the behavior of threshold as a function of pulse width (input pulse was a rectangular pulse with t_r & t_f under 1 ns). Input-output delay as a function of input pulse height is reported in Fig.4 for a rectangular input pulse 40 ns wide (t_r & $t_f \leq 1$ ns).

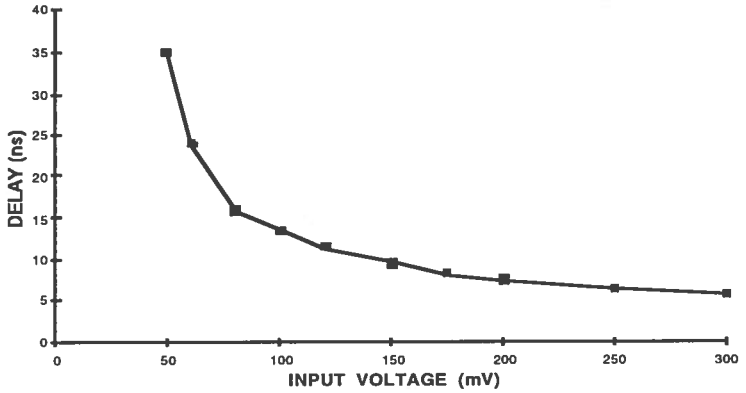
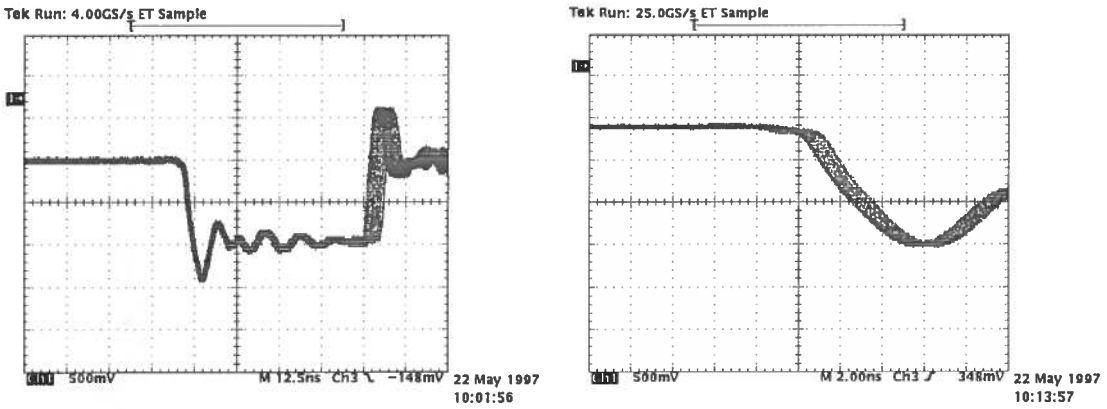


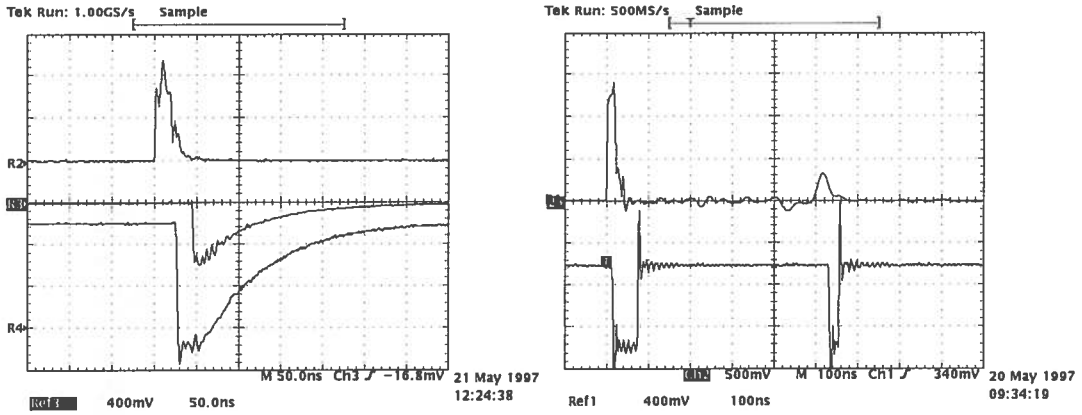
Fig.4 - In/out delay as a function of input voltage.

Time walk for an input pulse varying from 250 mV to 2 V is shown in Fig.5a. Jitter of the leading edge is 1.2 ns (Fig.5b). Crosstalk is also an important point. In Fig.6a strip 9 and strip 11 are hit with pulses well above threshold and induced signal on the collector of transistor Q_2 serving strip 10 is shown.



5a **5b**

Fig.5 - Time walk measurements.



6a **6b**

Fig. 6 - Crosstalk measurements (6a) and double pulse resolution (6b).

Double pulse resolution tests (Fig.6b) have also been performed. The first pulse is well higher than threshold, the second pulse is just above threshold to magnify any possible paralyzing effect. Results are very satisfying. After 1.5 μs, corresponding to a frequency of 500 kHz, there is no memory of the first pulse.

5. PFEC REMOTE CONTROL

To check functionality of the board a test input has been foreseen on each board. The test input is a very handy feature since it allows to ascertain proper operation of the board by simulating an hit on all the sixteen channels. In Fig.7 channel hit distribution for one board as a function of different input pulse widths is shown.

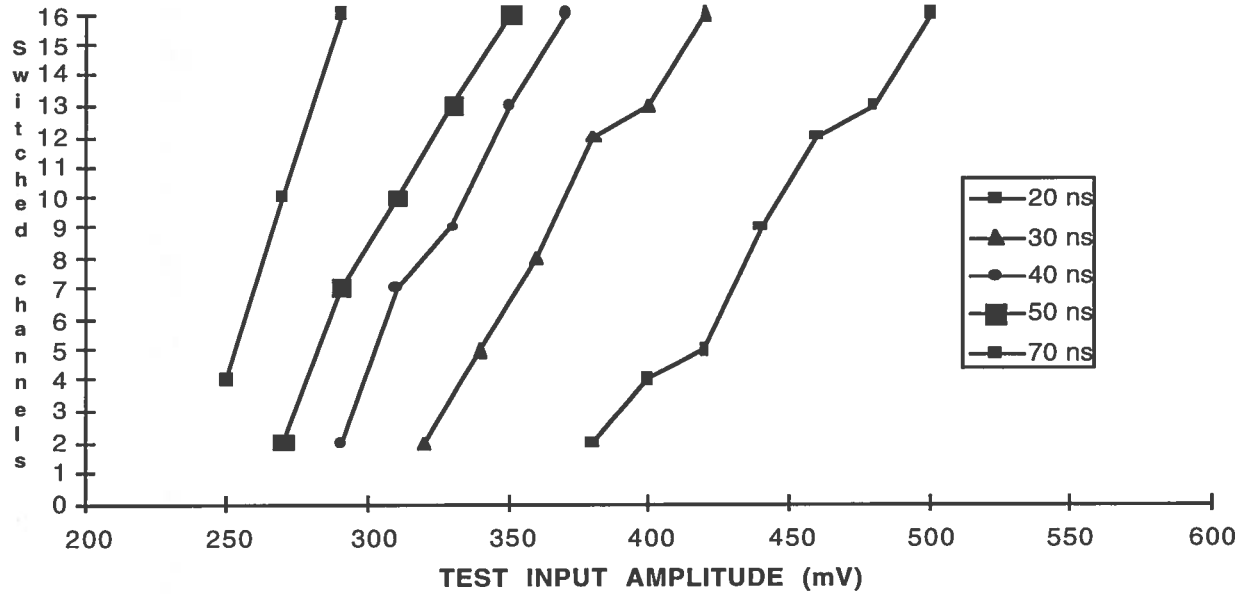


Fig.7 - Measured channel hit distribution as a function of test pulse.

Measurements show that for a test input pulse width of 70 ns the channel spread is limited to 30 mV, while for test input pulse width of 20 ns channel spread is under 120 mV.

6. READOUT SECTION

The readout section of the PFEC board has been already described in greater detail elsewhere [4]. It is based upon a MACH210-AQ15 which receives a 32 input pattern from the monostables (A0 through A15 and B0 through B15). Inside the PLD signals An & Bn (n=0 through 15) are first made in anticoincidence and then, whenever the SHIFT/LOAD signal is high, are loaded into the shift register on the low to high transition of CK_CHAIN and status of strip no.15 is output. Then, with the SHIFT/LOAD signal low, the strip no.14 is output on the next CK_CHAIN and so on.

7. SUMMARY

In this note we have shown the simulations performed before production of the PFEC and tests carried out on the first prototypes. The PFEC card is actually being mass produced and installed onto the Babar detector. Results are satisfying.

8. ACKNOWLEDGMENTS

The authors would like to thank Prof. C. Sciacca for his constant encouragement and creative discussions. We would like also to thank Mrs. C. Caiazzo and Mr. F. Manna for their support in the test of the mass produced boards.

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