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REALISATION OF RELIABLE CRYOGENIC ASIC's USING GaAs ION-IMPLANTED MESFET TECHNOLOGY

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ABSTRACT

After designing a preamplifier chip to readout at cold the signal of a LAr calorimeter, we have ordered fabrication of four wafers of a GaAs ion-implanted MESFET process and investigated the dispersion of dynamic and noise parameters of the chips. The influence of charge trapping, thermal stress, high voltage sparks and chip cooling on the reliable operation of a cryogenic read-out system has also been analised.

1. - INTRODUCTION

Development of detectors operating at cryogenic temperatures stimulated research work to make possible the realisation of electronic circuits capable to operate at temperatures well below -55 ^{o}C, the minimum temperature specified in the MIL standards. Several functions must be fulfilled by those *cold* circuits, among which low-noise amplification, multiplexing, and LED driving are common. The operating temperature requirements extend between 4 K, in case of deep cryogenic detectors(1), 77 K for a number of applications using LN, 87 K in LAr calorimeters(2) or time projection chambers(3), 120 K in LKr calorimetry(4, 5) or 150 K in LXe ionization and scintillating chambers(6,7).

So far it is well established that Si JFETs have their best performance at about 120 K and, although many JFET types operate at 77 K and even below, their performance becomes severely compromised at that temperature. MOSFETs and CMOS circuits can operate in the whole temperature range down to 4 K(8). III-V devices like HEMFETs, and MESFETs and III-V or SiGe HBT's do operate also in a wide temperature range extending even to 1 K(8,9). HBT's have very low 1/f noise even at room temperature(10). MESFETs and HEMFETs exhibit the attractive characteristic that, unlike MOS devices, their 1/f noise decreases strongly, and also their speed improves when cooling down(9). GaAs MESFET is already a mature technology available from various foundries. We have proposed its use for the realisation of low-noise preamplifiers for noble-liquid calorimetry, initially in the frame of an R&D activity and later in ATLAS(2). Use of cold electronics would allow to reduce coherent noise as the detector current signal could be amplified at the cell's end by a large factor before being sent to the outside of the cryostat where the risk of contamination by RFI is higher(11).

LAr calorimetry in ATLAS stimulated investigation of the cryogenic characteristics of monolithic processes that could be used in the realisation of reliable low-noise preamplifiers operating directly immersed in the LAr. Since beginning of 1992, we have used a GaAs MESFET process(12) for the fabrication of more than 1000 cryogenic analog chips. This process was investigated having in mind the possible production of preamplifiers for the ~100000 channels the electromagnetic barrel calorimeter. In view of the fact that the cold electronics in the calorimeter would not have been accessible for 10 years after the completion of detector assembly, evaluation of the accuracy of chip manufacturing and chip reliability at cryogenic temperatures was of utmost importance. We have recently made fabricate four wafers carrying low-noise preamplifiers of novel design to perform such evaluation.

In section 2 we recall the cold readout system proposed for ATLAS. In section 3 we give details on chips fabrication. Finally, in section 4 we concentrate on reliability issues.

2. - A COLD READOUT SYSTEM FOR LAr CALORIMETRY

The principles of the cold readout system proposed for the barrel electromagnetic LAr calorimeter of ATLAS was already illustrated[11]. The system is based on a fast dominant-pole monolithic preamplifier (DPA) fedback in a current-sensitive configuration by means of a parallel combination of a resistor and a capacitor external to the DPA chip, mounted on the mother board. The values of those components would vary according to the rapidity of the detector cell being read-out.

This fast readout configuration has an input resistance of only a few ohms that keeps limited signal cross talk. The amplification of detector current by a factor between 4 and 8 would allow lower coherent noise.

Operation at cold implies reduction of device ageing but may determine charge trapping and thermal stress, during cryostat filling cycles. The heat dissipated inside the cryostat could in principle create bubbles which are prone to break cell's isolation and therefore trigger HV discharges that could provoke damage in the chips. Radiation damage is also possible and deserved due attention. All those aspects have been investigated (see Section 4).

The DPA was designed as an improved version of our previous preamplifiers used in the prototype detector[13]. For simulation we used SPICE GaAs Statz model parameters fitting DC characteristics measured at 87 K. The "C4" chip was designed in three "flavours" (DC, SC and LV) all of them having at the input a 3 x 24000 μm^2 MESFET biased at 8 mA. The DC flavour has a double cascode loading the input FET. The SC flavour has a single cascode stage and the LV has a single cascode and an output stage with a lower DC voltage at the output compared either with SC and DC. Full details of those chips are given in ref [14] and [15].

Two channels are accommodated in the 2.5 x 1.5 mm^2 chip, whose microphotograph is shown in Fig. 1. Performance of C4-DC DPA chips immersed in LAr is summarized in Table 1.

3. - FABRICATION OF C4 CHIPS

We have ordered fabrication, in a multiproject approach, of four wafers carrying DC, SC and LV flavours of C4 DPA chip. The area occupied by our project was only ~10% of the total useful area of the wafers which carried also other projects. The process used in the past[12] has been characterised at cryogenic temperatures[16]. This process offers two depletion MESFETs with - 0.6 V and - 2 V pinch-off voltage, and enhancement MESFETs with + 0.15 V threshold voltage. Particularly useful for cryogenic operation are the 50 Ω/sq NiCr film resistors.

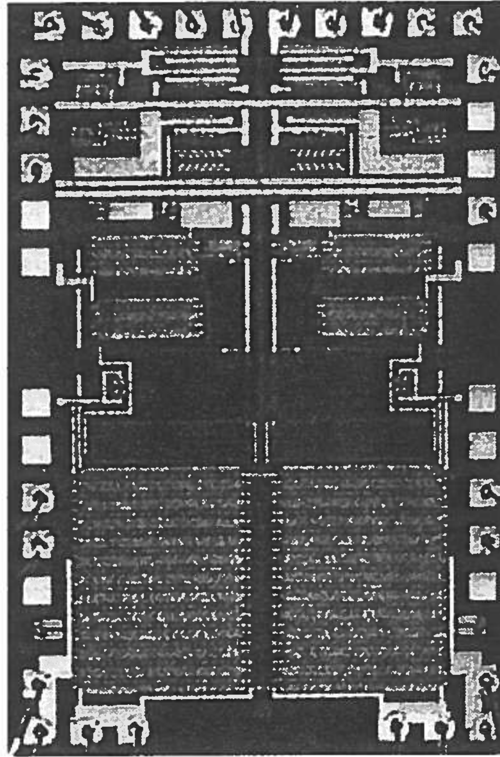

Fig. 1. A view of the dual-channel C4-DC DPA chip. Note the large area occupied by input transistors.

Table 1. Main parameters of C4-DC DPA chip at 87 K

GBW Product (compensated)	1.7 GHz
Series White Noise	0.33 ± 0.015 to ± 0.045 nV/√Hz
Corner Frequency of 1/f Noise	0.8 MHz
Dynamic Range	3 V with 0.6% INL
Power Dissipation	70 mW

The chips have been evenly distributed in 30 "tiles" along each wafer. A total of 480chips have been fabricated in the four wafers. All chips have been visually inspected, and it was verified that out of 120 DC's fabricated, 105 passed the inspection. After assembly into 18 pin DIL packages, electrical income characterisation was performed. In that operation only two chips did not work well and were discarded. The resulting fabrication yield was therefore quite high, ~86%.

Chips of the other two flavours (LV and SC) have been assembled to complete a total number of 250 units (500 channels) that were evaluated at 87 K.

The test set-up consisted in a DPA fedback as a current-sensitive preamplifier followed by a RC-CR^2 shaper. A quasi triangular test current was injected at the input node which also had a capacitor Cd simulating the detector. The capacitance of Cd was either 1 nF or 2.2 nF. The

peaking time and pulse amplitude after shaping, and the noise expressed in terms of equivalent detector current was evaluated for every unit, identified by their wafer of origin labelled from #38 to #41. In this way dispersion of noise, gain and speed in each wafer was established. The results are summarised in Table 2. Plots are presented in ref.[14].

Table 2. Uniformity of Performance in wafers 38, 39, 40 and 41.

	Peaking Time tp [ns]		ENI at tp [nA]		Amplitude [mV]	
W#	C_D=1nF	C_D=2.2 nF	C_D=1nF	C_D=2.2 nF	C_D=1nF	C_D=2.2 nF
38	40.0±1.3	40.1±1.0	114±13	222±33	287±8.9	268±13
39	39.9±0.5	40.2±1.4	101±4.8	222±20	281±7.8	269±9.0
40	40.0±0.6	39.3±2.2	101±12	204±19	287±9.5	267±9.4
41	40.3±1.1	39.2±1.2	100±10	211±22	289±4.8	266±9.6

As can be observed in Table 2, the peaking time and the gain dispersion in the four wafers was below 5%, whereas noise ranged from 5% to 15% depending on the wafer.

It must be remarked that, at cryogenic temperature, noise depends on the doping of the FET channel. It was found that either noise level and its sensitivity to temperature depends, in the 87 K region, on the resistivity of the FET channel, RSD. This parameter could in principle be comprised between 475 and 775 Ω/sq, as specified by the foundry. In practice, we have never seen RSD to be outside the 560 to 680 Ω/sq. interval, and this is understandable because there is also a boundary of guaranteed pinch-off voltage which puts another limit correlated to RSD. In Fig. 2 we show the guaranteed range of Vp correlated to the range of RSD for many of ours and other's runs.

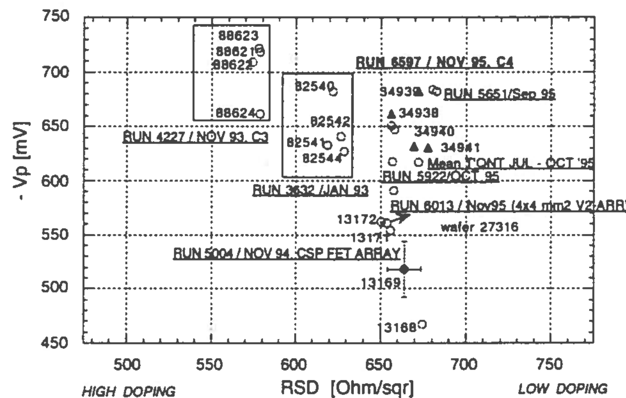

Fig. 2. Pinch-off voltage of D FETs vs. channel resistivity RSD of different foundry runs made between January 93 and November 95.

A plot showing series noise of MESFETs normalized to a reference FET having (L/W) = 3/24000 μm, at 77K and at 87 K is shown in Fig. 3. C4 chips have been fabricated with the run Nov 95. Still lower noise was obtained in the past (Jan 93 and Nov 93).

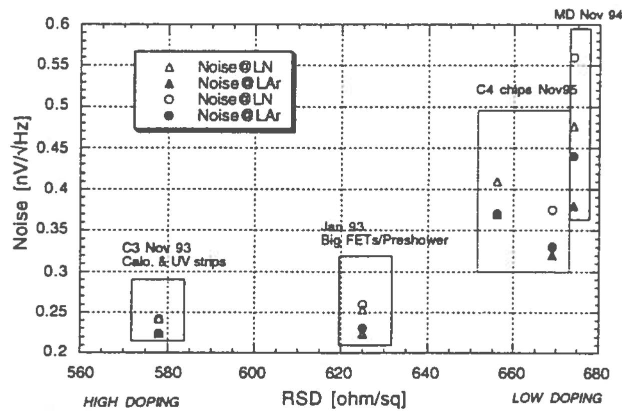

Fig 3: Noise density at 77K and 87 K vs channel resistivity of chips used with a LAr calorimeter prototype.

4. - RELIABILITY ISSUES

Operation of electronic devices at low temperatures is in principle beneficial from a reliability point of view, as processes determining failures in semiconductor devices, like electromigration, are severely suppressed when the device is cooled. The mean time between failures (MTBF) has an exponential dependence of 1/Top, where Top is the operating temperature[17]. Data verifying this law has been collected in the standard temperature range but no or scarce data is available for cryogenic temperatures.

In our case, reliability of preamplifier chips operating at cryogenic temperatures could be compromised by other processes like charge-trapping and thermal stress, in addition to the possible high voltage sparks in the detector, and radiation damage. We briefly discuss below each one of these items and present results of evaluation tests.

4.1 - CHARGE TRAPPING

At cryogenic temperatures, electrons moving in a FET channel may reach sufficient energy from the gate-drain bias field to be trapped in the interface between channel and passivation layer in the region near the drain. The charge will accumulate and will not be released back until the electric field is reversed, or the FET is warmed-up. This phenomena will provoke the collapse of the FET DC characteristics. We have observed collapsing effects in some MESFETs at cryogenic

temperatures when the drain-to-source bias voltage exceeded a certain level, close to 10 V[18]. For that reason, we looked for possible collapse in D and M FETs of the TriQuint process, in particular those devices subject to large voltage excursions. No such effects have been observed. Reports from other group working with Vitesse ion-implanted process, claimed similar results[19]. It must be noted that the relatively low breakdown voltage of the D and M FETs of the selected process naturally eliminates the possibility of developing large electric fields.

4.2 - THERMAL STRESS

We have performed thermal *shock* tests of chips and passive components. The purpose was to verify possible damage either in the dice itself, in the die attach, in the bonding or in the package.

Seven chips have been plugged in a test mother board using low profile sockets. The mother board contained also passive components: feedback components and decoupling capacitors. The chips were biased and their DC output was monitored while the board was immersed into a LN dewar and taken out, where they were heated up to ~50 ^{o}C. The cycle was repeated every 50 sec for 10 hours collecting ~5000 chip x cycles. At the end of the test, only tiny cracks have been observed in some ceramic lids. Metallic lids would be a better choice. Besides this effect, no reduction in chip performance was observed.

Also 60 electrolytic capacitors (Siemens solid tantalum B 45196 series) have been cycled 630 times (38000 units x cycles) with neither visible failures nor appreciable variation in the capacitance.

4.3 - HIGH VOLTAGE SPARKS

In the LAr Accordion calorimeter the high-voltage isolation at the 2 mm gap could be momentarily broken for various reasons. In that case, the energy accumulated at the coupling capacitance connecting the electrode with the preamplifier will be delivered to the input FET. To limit the amount of this dangerous energy, instead of making one continuous electrode, the electrode kapton includes a resistive coating between copper sections of smaller-area.

In order to make the chips insensitive to HV discharges, we designed a protective network using zener diodes, a 62 nHy SMD inductor and a 1 Ω resistor[14]. This network proved to protect chips against sparks of ~6 mJ. In fact, 3 channels have been subject to 10000 discharges of a 1.5 nF capacitor charged to 2.2 kV. The rate was 1 Hz. One channel received 25000 strokes from a 2.2 nF capacitor. Finally, 12 chips were tested in steps of 100 V up to 2.3 kV. In all cases with there

was no visible degradation.

One aspect that raised concerns about using cold electronics with the LAr calorimeter, was the possibility that the heat dissipated by the chips could create bubbles that, reaching the electrode gap, would eventually break the HV isolation. Preliminary tests of *hybrid* circuits operated in LAr with no overpressure, seemed to indicate the impossibility of avoiding the dangerous bubble formation[20]. This results was not surprising as the hybrid circuit carried discrete components dissipating power in a small area, with the consequent high temperature gradient at the LAr-package interface. Under the hypothesis that the use of monolithic chips assembled in ceramic packages would reduce the temperature gradient (simply due to the larger heat-interchange surface area) and that a slight overpressure would be enough to avoid any bubbling, a test to experimentally verify that situation was performed and described in the following sub-section.

4.4 - COOLING CHIPS WITH LAR

Two chips have been investigated: a "C3" chip assembled in 1 x 1 cm^2 28 pin ceramic package and the latest C4 chip assembled into a 18 pin DIL ceramic package. The C3 chip was mounted on a small PCB carrying also two biasing chip resistor of 430 Ω. C4 contains all biasing resistors inside the chip, therefore it was immersed without mounting it onto any PCB. The chips were installed inside a 50 cm deep glass dewar, vacuum-isolated from the cryostat wall which has five 1" diameter optical windows. The dewar was filled with different heights of the LAr column.

The dewar could be overpressurized up to 600 mbar. Using a video camera and a VTR the activity inside the LAr was recorded. Convective currents could be noted by observing the movement of small ice particles.

The test consisted in the following steps:

A) - Fill the glass vessel with a column of LAr 15 cm high.
   - Insert a C3 chip. Wait for stability: (no bubbles, smooth drifting of ice particles in LAr).
   - Put nominal bias current (8 mA per channel) and observe bubbling. Increase pressure, if necessary, to stop it.

B) - Increase bias current to 16 mA per channel. Increase over-pressure to stop it.

C) - Fill the glass with a column of LAr 50 cm high.
   - Repeat steps above.

D) - Repeat A, B and C for a C4 chip.

The results of the test are summarised as follows:

With a 15 cm LAr column, bubbles appear only when the power dissipation per unit area in the

biasing resistors reaches 4.8 mW/mm^2 and no overpressure is applied. At nominal power dissipation in the biasing resistors of C3 chips (1.2 mW/mm^2) and with an overpressure of 600 mbar, no bubbles are observed. With 45 cm LAr column, at nominal power dissipation, no bubbles are observed even with no external overpressure.

C4 chip was firstly immersed in a 15 cm LAr column. With no overpressure there were no bubbles at the nominal power dissipation, 140 mW. Only when power was increased to 320 mW, bubbles could be noticed. With 45 cm LAr column, and an external overpressure of 150 mbar, power had to be increased to 320 mW to start observing bubble formation.

Results are better appreciated by looking at the convective currents and bubbles shown in the video recording that documented all steps of this test(21). The tape shows pictures as in Fig. 4.

4.5 - RADIATION DAMAGE

Devices and circuits made with an ion-implanted MESFET process have already shown to be radiation hard at least to 2 x 10^{14} n/cm^2 and 0.5 Mrad of gammas, which are the levels of interest for 10 years of operation inside the barrel calorimeter(22). In all cases, a modest increase of noise and even stable DC operation of monolithic preamplifiers was observed, despite a shift of pinch-off voltage of ~450 mV after neutron irradiation (verified only at 1 x 10^{15} n/cm^2 1 MeV equivalent fluence).

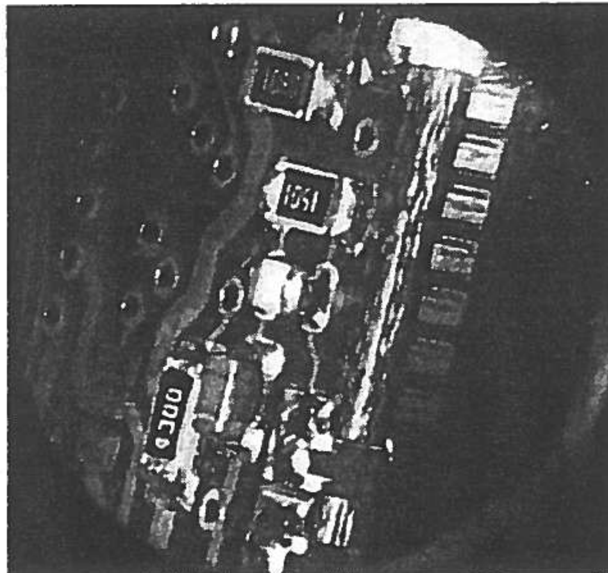

Fig. 4. View of a PCB, carrying a C3 chip in one side and biasing chip resistors on the other side, immersed in LAR as seen in the video tape recorded.

5. SUMMARY AND CONCLUSIONS

A GaAs ion-implanted MESFET process was used to fabricate four wafers containing 480 units of a 1.5 x 2.5 mm^2 monolithic preamplifiers designed to operate immersed in LAr and to read-out the signal of the Accordion e.m. LAR calorimeter of ATLAS. The fabrication yield was quite high, close to 86%. Evaluation of the dispersion of the dynamic and noise performance have shown an uniformity within ± 5% along all four wafers, whereas noise dispersion ranged from ± 5% to ± 15%.

Chips have been subject to thermal shock tests that did not revealed any visible deterioration in the chip performance even after collecting 5000 x chip cycles from 50 ^{o}C down to 77 K. The only exception was a tiny crack in a few ceramic lids noticed only during the last part of the test. No charge trapping related phenomena was observed in the chips. Passive components including electrolytic capacitors have been investigated; a solid-tantalum type passed 38000 units x cycles with no detectable failures.

The problem of HV discharge protection was affronted following two different ways: a) a protection network efficient up to 6 mJ was designed and tested with success; b) the possible generation of bubbles that could break HV isolation in the gap was studied by immersing chips in LAr and varying the pressure. It was shown that by dissipating less that ~2 mW/mm^2 and assuring an overpressure of ~300 mbar, cooling of the chip with no bubbles generation could be assured.

We believe that MESFET is an already mature process that could be used with high degree of confidence in the realisation of cryogenic integrated circuits for applications with particle detectors.

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