ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Napoli

INFN/TC–97/19
1 Luglio 1997

N.Cavallo, F.Fabozzi, P.Paolucci, L.Parascandolo, P.Parascandolo and D.Piccolo:

ELECTRONICS DESIGN OF THE FRONT-END FOR THE RPC MUON DETECTOR AT BABAR

To be Published on Nuclear Physics B (Suppl. Proc.)

SIS–Pubblicazioni
dei Laboratori Nazionali di Frascati

INFN – Istituto Nazionale di Fisica Nucleare
Sezione di Napoli

INFN/TC–97/19
1 Luglio 1997

ELECTRONICS DESIGN OF THE FRONT-END FOR THE RPC MUON DETECTOR AT BABAR

N.Cavallo, F.Fabozzi, P.Paolucci, L.Parascandolo, P.Parascandolo and D.Piccolo

INFN - Sezione di Napoli and Università degli Studi di Napoli "Federico II", Dip. di Scienze Fisiche,
Mostra d'Oltremare, Pad. 20, 80125 Napoli, Italy

A fast readout electronics has been designed for muon and neutral kaons RPC subsystem at BaBar. The overall architecture is described and requirements are thoroughly investigated. Great attention to the cost item has been necessary due to the huge number of channels.

1. Introduction

BaBar detector [1-2] has been designed to study CP Violation asymmetries predicted by the Standard Model in B meson decays. It will be installed on PEP II e^+e^- storage ring machine [3], operating at the Y(4S) resonance energy, providing a luminosity of 3×10^{33} cm^{-2} s^{-1}. Both the PEP II and BaBar commissioning are scheduled for the fall of 1998. The detector, is composed of a Silicon Vertex Detector, a Drift Chamber, a Particle Identification System, a CsI Electromagnetic Calorimeter and a magnet with an Instrumented Flux Return (IFR).

IFR [4-7] is a Resistive Plate Chamber (RPC) based detector whose task is to identify muons and detect neutral hadrons. Muons are identified by range and hit topology in the several active planes of this detector and by energy deposition in the central calorimeter detector. IFR also provides neutral hadrons (particularly K_L) detection. To achieve sensitivity down to μ momenta of 0.5 GeV/c, the IFR sub-detector (about 65 cm of steel in total) is divided into 19 iron layers (18 for the endcaps) of different thickness whose gaps are filled with RPC as the active elements. RPC layer signals will be read from one plane of strips (2÷4 cm pitches) running in orthogonal directions, thus providing bi-dimensional information.

The required physics detection performances imply a large number of strips, about 50,000 (~22,000 for the Barrel and ~28,000 for the endcaps), thus an affordable cost per electronic channel is a must.

This paper describes the front-end and fast readout electronics designed for the RPC strips readout.

Corresponding author: N.Cavallo

2. BaBar Data Acquisition System

The BaBar electronics system deals with all front-end, trigger, and data acquisition electronics.

The high-luminosity PEP-II machine poses unique challenges to this system. PEP-II beam crossings, in fact, occur at a rate of 238 MHz, which, in terms of the response time of the electronics, is essentially continuous, unlike previous e^+e^- colliders.

The severe backgrounds produce high occupancies which present a significant burden on the transport and recording of data, especially for the inner part of the detector. The rate of all processes to be recorded at the design luminosity of 3×10^{33} cm^{-2} s^{-1} is expected to be 100 Hz. The electronics system will also need to accommodate the rate and background implications of a luminosity upgrade to 10^{34} cm^{-2} s^{-1}.

An innovative architecture (that departs significantly from previous implementations at conventional e^+e^- experiments) has been conceived: all the electronics sub-systems are capable of collecting data from the detector in real-time, processing and transporting the data in parallel. To avoid deadtime losses, while making trigger decisions, data are extensively buffered. In addition, trigger logic and data acquisition system are capable to process simultaneous multiple trigger events.

3. General Architecture Overview

As the RPC is a noiseless detector [4,5], in which the rate is fully dominated by cosmics, and because the rate of particles reaching the IFR is relatively low, rejecting unwanted data as soon as possible is not so important as collecting data very rapidly.

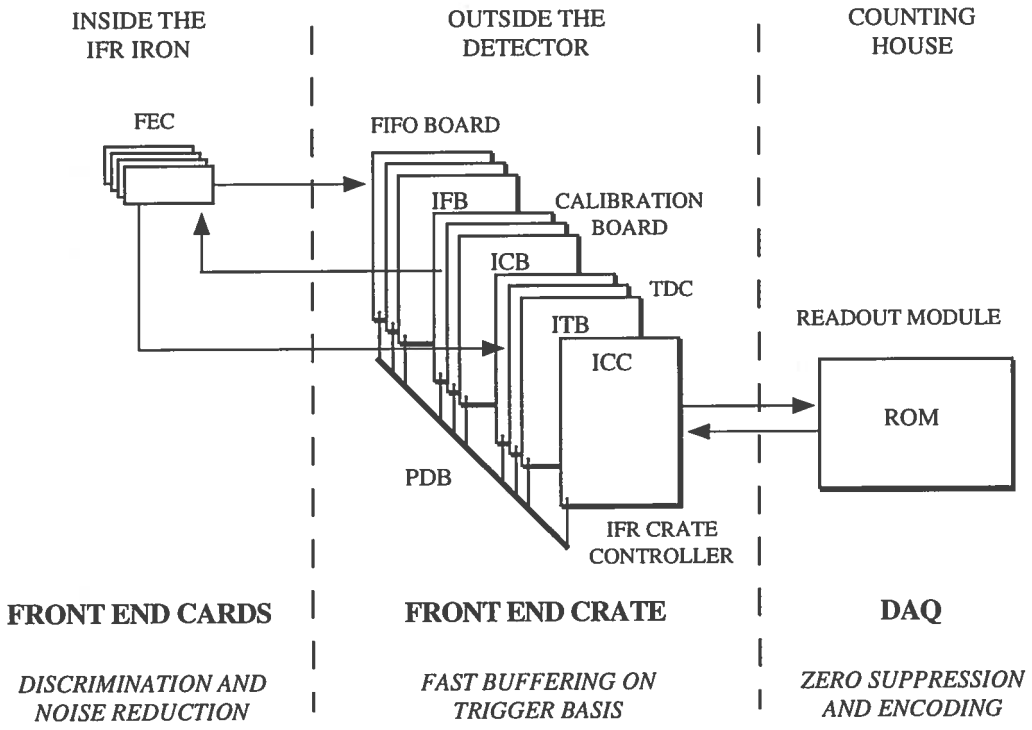

Figure 1. IFR General Electronics Architecture.

Level 1 trigger carries a fixed latency of 11.5 μs with a maximum jitter allowance of 0.5 μs. As the minimum time between successive triggers is 2.2 μs, the readout of front end electronics must be performed into the same time. Buffering during the trigger latency is unnecessary because the probability of having two hits on the same strip during this time is extremely small [8].

Strip signals are thus stored during the latency of the trigger decision (L1 Trigger Accept) simply stretching them and using a fast readout electronics to read the front-end within the prescribed 2.2 μs. IFR electronics behaves as a data driven system following the general philosophy of the BaBar experiment.

The IFR electronics records detected signals during L1 trigger latency, downloads data from front-end - without any data reduction - within the allowed time (2.2 μs) and then transfers data to the Readout Module (ROM), which performs zero suppression and digital encoding. A Readout Controller (ROC) reads hit data from several ROMs, assembles them into a full data stream, and eventually transfer them to a storage medium.

IFR particle detection also requires time measurements in order to improve μ/π separation, noise and beam halo rejection, ghost rejection and cosmic veto. These kind of measurements could also help to monitor the detector both during initial commissioning and/or data taking phases.

In order to meet these requirements the followings blocks are requested:

- A Front-End Card (FEC), serving 16 channels and acting as a discriminator card with a serial readout;
- A FIFO buffer (IFB) board;
- A TDC (ITB) boards;
- A multiplexed readout to the DAQ system.

The Front-End Card (FEC) will operate very close to the detector in the iron gaps. FIFO Board (IFB) and the TDC Board (ITB) will be outside the detector and accessible without opening the endcaps. The Read-Out Module (ROM) will be on the electronic trailer.

A block diagram of the IFR data acquisition system is shown in Fig. 1. DAQ Readout Crate (VME) housing the ROM follows the VME standard while the Front-End Crate (EUROCARD 6U) incorporates a special purpose backplane (PDB). The interface between the ROM and the Front-End Crate (through the crate controller ICC) will use the BaBar standard GLINK.

4. Front-End Electronics

Front-End Cards are used to discriminate the induced pulses of the fired strips, and to reduce noise. In the IFR detector the data is collected (and sparsified) at the detector front-end. Data must be readout, buffered in correspondence of a trigger and then moved to the data acquisition boards. FEC input stage is connected directly to the strips and operates continuously without regard to the trigger. Each strip acts as a transmission line with a discriminator at one end. The input stage feeds a dual bank of monostable, to get noise reduction, and provides a FAST-OR of the board.

To preserve the fast time response of the RPC detectors, the main requirements for the front-end electronics are both a fast response time and a good time-walk characteristic (Fast-OR jitter under 2 ns) which must be kept low to perform time measurements. Cost is also an important issue. Due to the huge number of strips, cost per channel must be as low as possible. Use of SMD components is a must as FECs are inserted into the iron gaps as close as possible to RPC (to avoid signal degradation). Finally high modularity demands 16 channels per card while operation claims low power consumption and negligible crosstalk.

The double one-shot system is fed by signal I0 to I15 (Fig. 2) and enables strip data collection only during the trigger jitter (±0.5 μs window), 11.5 μs before L1 arrival time. This reduces

possible noise coming from the RPC detector by accepting hits only in the time window established by the trigger uncertainty. Monostable's outputs are hooked to a PLD device acting as shift register parallel-in/serial-out, sending data to the following FIFO memory board (IFB).

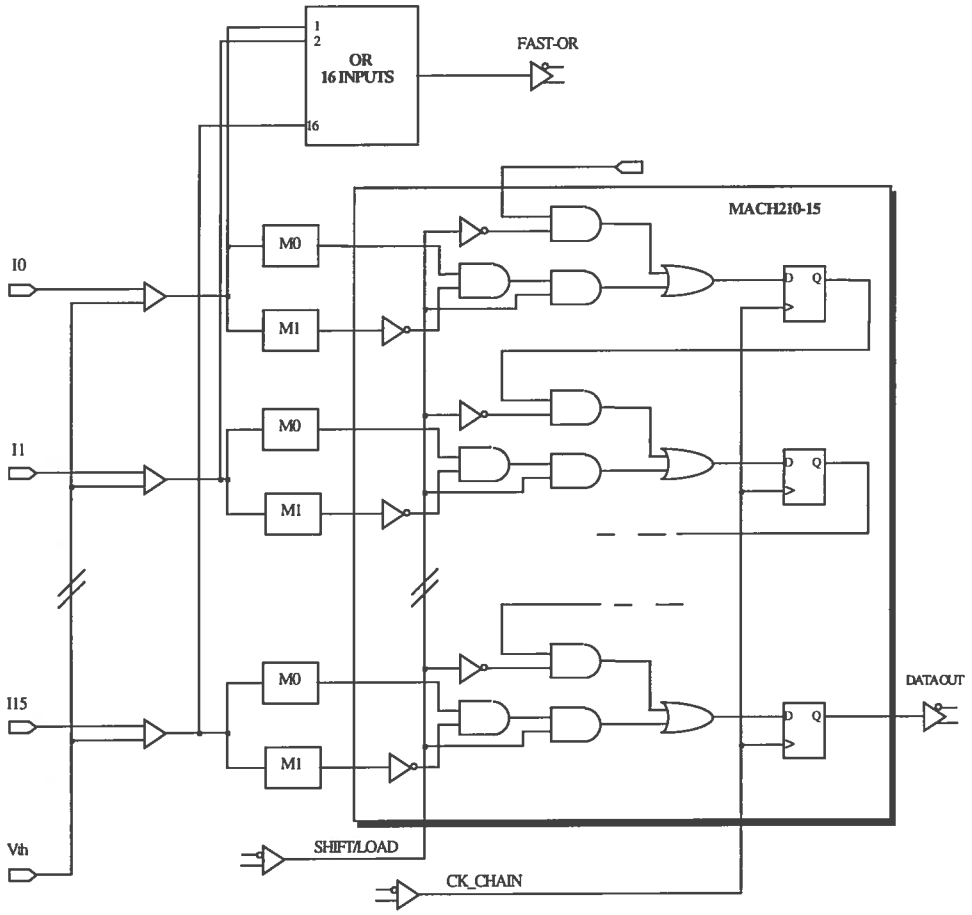

Figure 2. FEC functional block diagram.

A test input allows remote control of the board by injecting a pulse common to all 16 channels. Two kinds of input stages are required to handle negative and positive strip signals.

5. Fast Readout Electronics

Although the average acquisition frequency foreseen at BaBar is of just 2 kHz, maximum frequency peaks of 0.4 MHz could be also possible. The IFR FIFO Board (IFB) acts a as buffer memory between the front-end and the data acquisition system.

Working as an interface both vs. front-end cards and vs. data acquisition, IFB manages reading of front-end cards in less 2.2 μs, stores parallel data into FIFOs and then transfers FIFO contents into the Read-Out Module (ROM). In Fig. 3 we show the role of the IFB in the framework of the IFR readout architecture. IFB handles 64 Front-End Cards (FEC) acting as an acquisition master. Each IFB, through the PDB, receives commands (12 bit wide), transmits and receives data patterns from the ROM (via GLINK and ICC).

The system clock frequency (CK60) is at 59.5 MHz. Commands and data are fed to the IFB via the DIN input. The only output of the module is the DATA OUT line (Fig. 4).

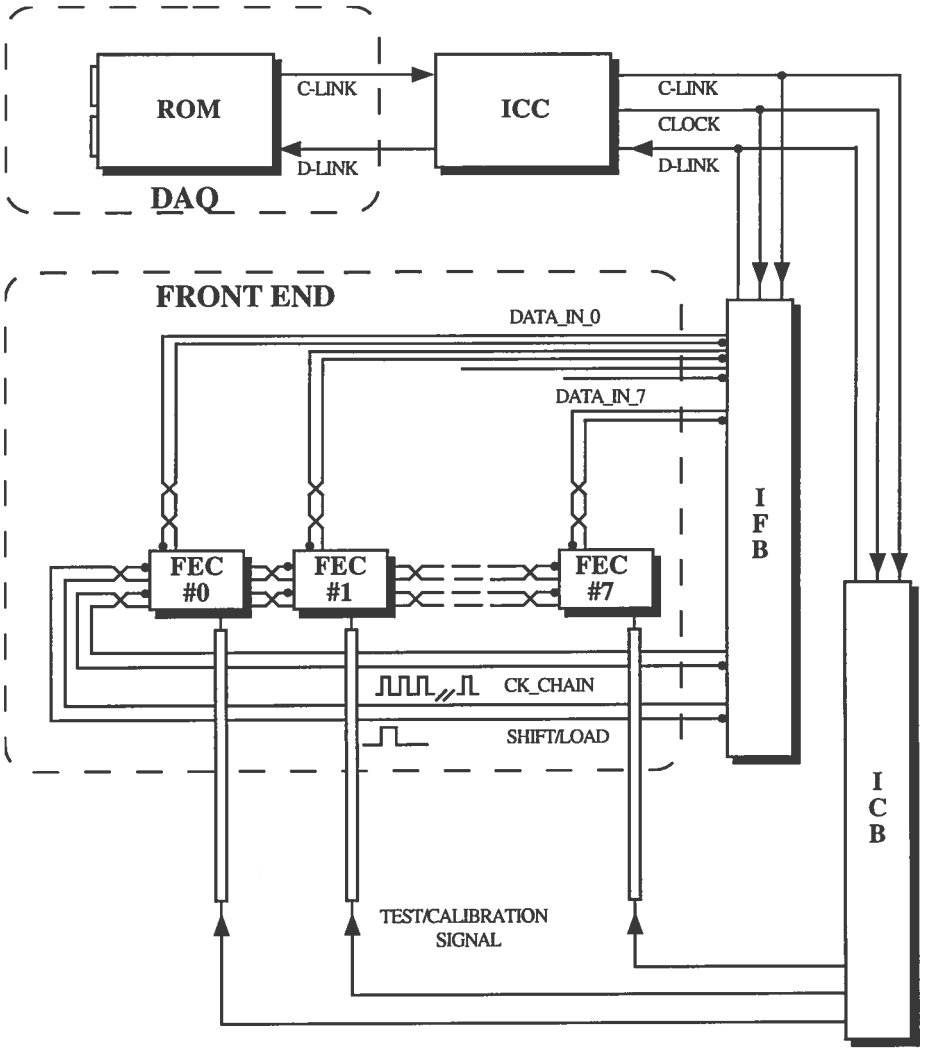

Figure 3. Front-end readout mechanism.

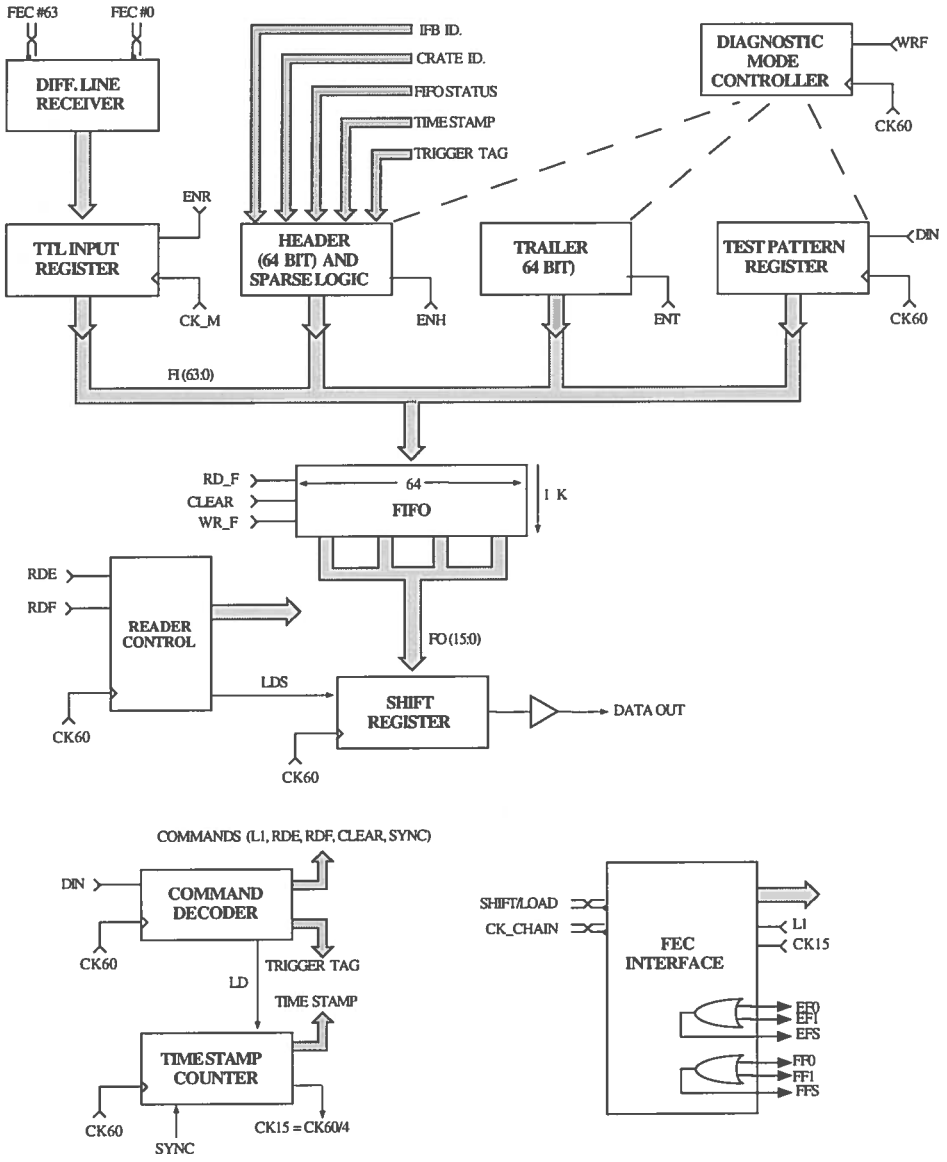

Figure 4. IFB Functional Block diagram.

When an L1 Trigger Accept is issued, strip status (hit or not), must be transferred into the IFB's FIFO set. To carry out this task IFB sends a 16 pulse train (CK_CHAIN) plus a SHIFT/LOAD signal to the FEC and synchronously store incoming data into the FIFO. Running at about 15 MHz, the readout lasts less than 1.5 μs. Elapsed this time, front-end electronics is ready to accept a new trigger.

Communication protocol between DAQ system (ROM) and Front-End Electronics follows the BaBar protocols standard [10]. Basically there is one start bit, 5 command bits, plus a 5 bit field which can contain data or address depending on the command type ("Run-time" or "Non-Run-time" commands).

Non-Run-time commands can be of variable length as they can incorporate an additional data pattern of n bits. Command code 0 through 5 are reserved for prompt commands (time critical).

Op-codes 6 through 31 are used for setup, write and read back, etc. which are not time critical. The transmission frequency is 59.5 MHz.

Run-time commands are commands that can be executed during run time. They are: NOP, Clear Readout, Sync, L1 Trigger Accept, Read Event, Calibration Strobe.

Non-Run-time Commands, executed only during calibration, setup or diagnostics are peculiar for each sub-system. For IFB, for example, they are "Write IFB FIFO" and "Read IFB FIFO" used to write and read the board for diagnostic purposes.

For each L1 Trigger Accept command 16 words of 64 bit data plus an header and a trailer are stored onto the FIFO (Fig. 4). Onto the header are inserted either a trigger tag available with the L1 command and the time stamp, which is an 8 bit counter clocked by the system clock, common to all the experiment electronics. A trailer, made up by 32 "ones" closes the event.

When a Read Event command is issued the first available event data (18 words) from FIFO are sequentially stored into a shift register (parallel-in/serial-out) and transferred to the Read-Out Module (ROM).

Data acquisition system has complete control of IFB as it is possible, via DIN, to inject a test pattern (WRF command) which writes a test pattern of 64 bit onto the FIFO.

RDF command is the complimentary of the WRF one and is used to read just one pattern (64 bit) from the FIFO to the DAQ. The CLEAR command resets FIFO's flags while the SYNC command resets the time stamp counter.

6. Test and Calibration Electronics

IFR Calibration/Test Board (ICB) is used for front-end test and calibration purposes. To test a FEC it is necessary to inject a signal in the input stage. This is done selecting "a priori" the boards to be checked and then employing the "Calibration Strobe" command.

A signal of programmable amplitude and width is thus produced and a readout command RDE issued to the IFB to check weather the FEC/IFB/DAQ chain is working properly.

To provide T0 calibration, the board can be also used together with the TDC readouts to identify the time corrections to introduce to take into accounts time shift due to electronics components (cards, cables and different delays).

Also ICB communicates with the DAQ system through the protocol as described. In this case, sub-system commands enables or not individual channels to be checked and to set amplitude and duration of the output test pulse.

7. Conclusions

The negative Front-End Card has been intensively tested at prototype level and produced in a small quantity pre-series (500 ones). They are currently operating at Frascati and SLAC RPC test benches.

IFB and ICB prototypes have been already tested and the final prototypes will be available at the beginning of 1997.

8. Acknowledgments

The authors would like to thank Prof. C.Sciacca for his constant encouragement and creative discussions. We would like also to acknowledge G.Crosetti, M.Piccolo and M.Ambrosio for many useful suggestions. We also express our gratitude to A.Anastasio for his continuous and enthusiastic technical support.

References

1. Letter of Intent for the Study of CP Violation and Heavy Flavor Physics at PEP II, BaBar Collaboration, SLAC Report SLAC-443, June 1994;
2. BaBar Technical Design Report, BaBar Collaboration, SLAC Report SLAC-R-95-457, March 1995;
3. PEP II - Conceptual Design Report, SLAC Report SLAC-418, June 1993;
4. Chapter 8 in reference 2;
5. N.Cavallo et al., Scientifica Acta - Quaderni del Dottorato, vol. XI N. 1, pg. 115;
6. P.Paolucci et al., Nucl. Instr. and Meth. A379 (1996) 472-474;
7. F.Anulli et al. these proceedings;
8. N.Cavallo et al., INFN/TC-96/22;
9. Hewlett Packard HDMP-1012/HDMP-1014 Gigabit-rate chip-sets;
10. BaBar Note 281.