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A DIGITAL READOUT SYSTEM FOR THE SYRMEP SILICON STRIP DETECTORS

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A Digital Readout System for the SYRMEP Silicon Strip Detectors

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The SYRMEP project (SYnchrotron Radiation for MEdical Phisics) intends to improve mammography performances using two non-traditional means: synchrotron radiation and silicon detectors. A silicon cristal (the monochromator) allows to choose the optimal beam energy that leads to the maximum signal to noise ratio, while the detectors are arranged to form a matrix of pixels and coupled to low noise high-gain VLSI integrated circuits making the single photon counting technique possible.
We present the data acquisition system implemented to read out the VLSI circuit with particular emphasis on two dedicated CAMAC modules that generate the control signals and store the chip digital output on memories that can be accessed via the CAMAC bus. It has been useful in testing the chip performances and can be considered a prototype of the final SYRMEP data acquisition system.

1 Introduction

The strips of the SYRMEP [1] [2] silicon detectors are read by VLSI CMOS mixed analog-digital circuits [3] with pure digital serial output consisting of a sequence of groups of 16 bits which represent the number of photons detected

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in different pixels (single photon counting technique).
In the next section we describe the chip characteristics and the control signals needed for its correct operation, while section 3 is devoted to a general presentation of the DAS system; finally a detailed description of the Control and Readout modules is presented.

2 The chip and its control signals

The CASTOR (Counting and Amplifying SysTem fOr Radiation detection) chip was designed in collaboration with LEPSI (Strasbourg) and produced by AMS (Austria), in 1.2 μm CMOS tecnology, to be used for reading the SYRMEP silicon detectors irradiated by a X-ray monochromatic beam.
A tipical mammography energy of 25 keV implies creation of only $\sim$ 6500

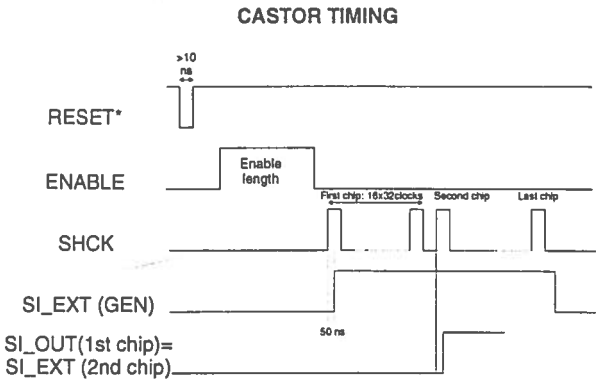

Fig. 1. Correct control signals timing

electron-hole pairs per photon inside the detector silicon bulk: this charge must be sufficient for generating an analog pulse and discriminating it from noise thus allowing the single photon counting technique. For this reason CASTOR main characteristics are its high gain ($\sim$ 200 mV/fC) and low noise (ENC (e^- rms) $\simeq 60 + 17 \times C_D$ (pF)).
The chip contains 32 identical channels for parallel processing of signals, each one featuring a low noise charge-preamplifier, a CR-RC shaper, a buffer, a threshold discriminator and a 16-bit counter. The analog part of the electronic chain limits the counting rate to around 100 kHz; during readout the 32 counters are connected to form a unique long shift register which can be clocked up to 20 MHz; storage of bits outcoming serially from the chip and production of a data file on a computer memory are two of the main tasks of the DAS described in the next section.
Another important task is the generation of suitable control signals obeying to a definite timing. As can be seen in fig. 1, the first action consists in clearing the 16-bit counters with the signal RESET*; the acquisition phase can then be started setting the signal ENABLE high. Extraction of the counting result

is achieved in the read-out phase which is started by the SI_EXT signal and controlled by the readout clock (SHCK); its completion is denoted by the SI_OUT output signal which can be used for the readout of several daisy-chained chips. All these signals obey to the logic +2V (high) -2V (low).

3 The Data Acquisition System

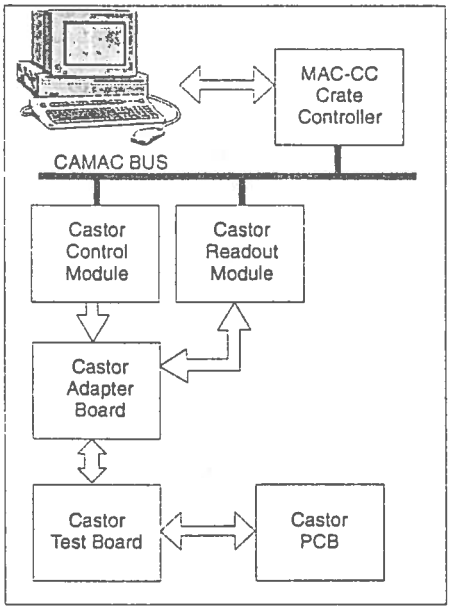

Fig. 2. DAS block diagram

Figure 2 shows the DAS block diagram. Standard CAMAC was used because of simplicity and ease of implementation; however the VME system is going to be adopted for the definitive set-up. The CAMAC system is controlled by a Macintosh 2fx computer through a Micron interface and a MAC-CC crate controller. For software development the MACUA1 package [4] is used, which includes a set of procedures that can be called from programs written in RTF (Real Time Fortran).

Generation of the control signals of fig. 1 is committed to CCM (Castor Control Module), a dedicated CAMAC module which allows also execution of two tests on the digital part of the chip consisting in sending a known number of clock pulses during the acquisition phase and a known sequence of bits (SERIAL_IN signal) during the readout phase. A second CAMAC card, the Castor Readout Module (CRM), is used to store into a set of 2 static RAMs the digital output of the chip, which is housed on a separate printed circuit (Castor PCB). A special test board (CTB) is used for the fine tuning of several operational parameters of the analog part, like the gate voltage of the preamplifier and shaper long channel feedback transistors, or their biasing currents.

Another task is the conversion from the CAMAC TTL logic (0V,+5V) to the chip one (-2V,+2V); this is accomplished by an adapter board (CAB) where the HP2630 optocouplers guarantee also a remarkable noise immunity on logic signals.
Basically this system allows to control from computer the acquisition and readout phases of the chip and afterwards to access the RAMs inside CRM to collect data. A CAMAC DAC, not shown in fig 2, provides the discriminator threshold and is controlled from the DAS program too. The final result is the creation, in the computer memory, of a file containing the numbers of signals counted by the chip 32 channels at each threshold value. Integral counting curves, very useful in studying the chip properties, can then be acquired. An example of these curves is shown in fig. 3A. The curve was obtained injecting 2.5fC by differentiating a 1mV voltage step on a 2.5pF capacitance in parallel with one channel input; after differentiation and gaussian fitting the mean amplitude of the analog pulse inside CASTOR can be found.
Using this method the gain and noise performances of the chip were found to be in good agreement with theoretical expectations; indirect techniques for peaking time estimation and signal shape evaluation were also applied to permit the understanding of detailed studies concerning counting rate capability.

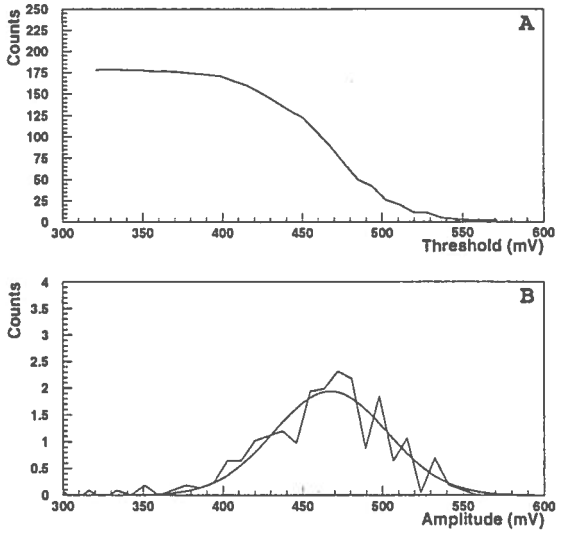

Fig. 3. Example of integral counting curve (A) and its differentiation and gaussian fitting (B)

4 The Control and Readout modules

They are the most important part of the system.
The procedure pursued in developing these cards was to assign to any oper-

ation a combination of CAMAC control and address signals, which can be issued via software. On the modules an interface block receives them from the CAMAC bus and a decode block recognizes the combination, replies with a signal and possibly activates other sections that will execute the wanted action. Examples of such actions are determining the acquisition time (i.e. the ENABLE signal duration) or read from the computer the bits stored in CRM. The heart of this module, a set of two 2kbyte static RAMs, must be accessible

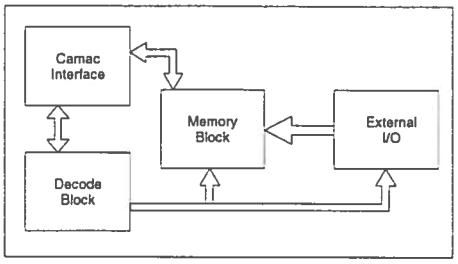

Fig. 4. CRM block diagram

from two directions: from inside, i.e from the computer through the CAMAC bus, and from outside, i.e. from the chip. For this reason it has been taken particular care in avoiding conflicts between accessing memories in internal or external mode. To overcome the CAMAC address limitations (4 address

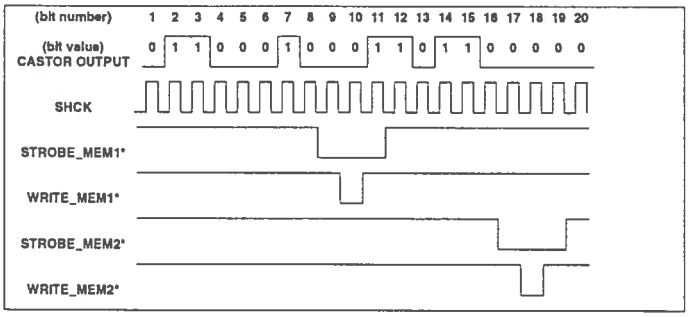

Fig. 5. Memory block timing

lines) each memory location is entered in two steps, first memorising the location address in a latch and then entering data. This approach is used both in writing and reading in internal mode. Writing in external mode is instead demanded to the "external I/O" block of fig. 4. It receives three RS-422 signals from outside: the chip serial output, SHCK and $\overline{RESET}$, the last two coming from CCM. The serial output is parallelized into groups of 8 bits and passed to the memory block whereas SHCK is counted for automatic generation of increasing addresses. Two active low strobe signals (STROBE_MEM1* and STROBE_MEM2*) are also generated for the latches connected to memories data lines to assure correct temporization of data storage (fig. 5).
According to the chip design, for each channel of CASTOR, the first memory

always stores the 8 least significant bits while the second stores the most significant ones.
The CCM block diagram is shown in fig. 6. Here the decode block is included in the interface one. A 2MHz quartz oscillator supplies the parent clock from which SHCK is obtained and the acquisition time is determined. The third operative block allows execution of two tests on the digital part of the chip as described in section 1.

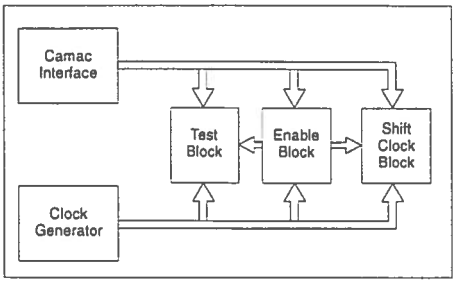

Fig. 6. CCM block diagram

5 Conclusions

The system, in spite of its prototype nature, has proved to be reliable and robust. It allowed collection of a large amount of data for evaluation of the chip performances and is now used for reading the first module of the final SYRMEP detector irradiated by the ELETTRA synchrotron beam.

References

[1] F. Arfelli et al., NIM A360, 1995, 287.

[2] F. Arfelli *et al.*, " A pixel-like matrix for digital mammography ", presented at the 9th International Workshop on Room Temperature Semiconductor X and γ ray Detectors Associated Electronics and Applications, Grenoble, France, September 18-22, 1995.

[3] C. Colledani et al., CASTOR1.0 a VLSI analog-digital circuit for pixel imaging applications, presented at the 3rd Workshop on Semiconductor Pixel Detectors for Particle Physics and X-ray detection, Bari, Italy, March 24-27, 1996; to be published on NIM A

[4] S. Cittolin et al., MacUA1: Macintosh-based development system for data acquisition, control and monitoring applications, CERN UA1 TN 90-01, 1990.