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FRONT–END CARD DESIGN FOR THE RPC DETECTOR AT BABAR

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Abstract

This note describes the Front-End Card (FEC) developed to read the signals of the RPC detector at BaBar.

Very intensive tests have been performed on the prototype cards in order to check both performances as a function of different components (i.e. transistors, inductors, LS vs. HCT family chips) and operative conditions (i.e. amplitude, duration and shape of the input pulse, supply voltages).

Introduction

BaBar detector [1-2] has been designed to study CP Violation asymmetries predicted by the Standard Model in B meson decays. It will be installed on PEP II e^+e^- storage ring machine [3], operating at the Y(4S) resonance energy, providing a luminosity of 3×10^{33} cm^{-2} s^{-1}. Both the PEP II and BaBar commissioning are scheduled for the fall of 1998. The detector, as shown in Fig. 1, is composed of a Silicon Vertex Detector, a Drift Chamber, a Particle Identification System, a CsI Electromagnetic Calorimeter and a magnet with an Instrumented Flux Return (IFR).

IFR [4-6] is a Resistive Plate Chamber (RPC) based detector whose task is to identify muons and detect neutral hadrons. Muons are identified by range and hit topology in the several active planes of this detector and by energy deposition in the central calorimeter detector. IFR also provides neutral hadrons (particularly K_L) detection. To achieve sensitivity down to μ momenta of 0.5 GeV/c, the IFR sub-detector (about 65 cm of steel in total) is divided into 19 iron layers (18 for the endcaps) of different thickness whose gaps are filled with RPC [7] as the active elements. RPC layer signals will be read from one plane of strips (2÷4 cm pitches) running in orthogonal directions, thus providing mono and bi-dimensional information.

The required physics detection performances imply a large number of strips, about 42,000 (~18,000 for the Barrel and ~24,000 for the endcaps), thus an affordable cost per electronic channel is a must.

This note describes the Front-End Card (FEC) designed for the RPC strips readout and shows the results we have obtained testing the first prototype cards.

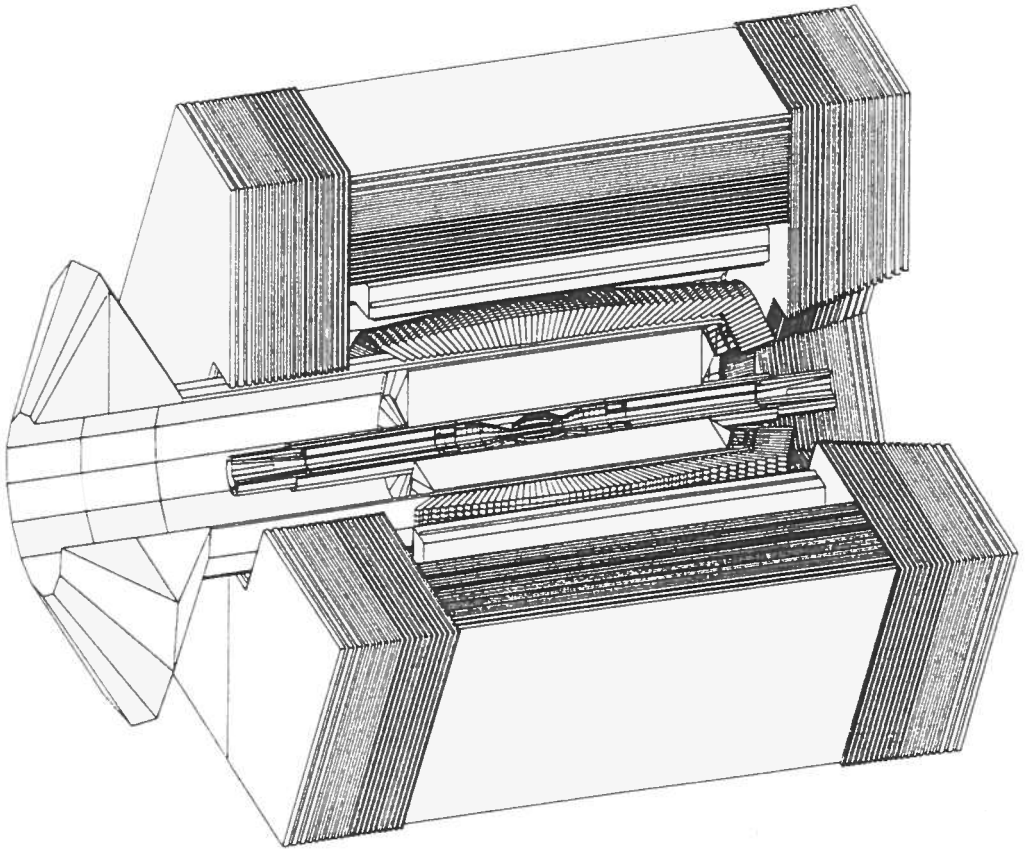


Figure 1 - Three-dimensional view of the BaBar detector.

1. Front-end electronics requirements.

In the IFR detector the data are collected (and sparsified) at the detector front-end. Data must be readout, buffered in correspondence of a trigger and then moved to the data acquisition boards.

IFR electronics must identify fired strips and associate an unique address to them. As shown elsewhere [2], the counting rate per strip and per trigger in 1 μs time, corresponding to the trigger uncertainty window, is of the order of 5×10^{-4}. Since we expect the rate of physics events being of the order of 30 Hz, we infer that IFR is a low occupancy detector. We also believe that machine background will have a negligible effect on IFR.

Accidental hits, due to background, in fact, can be detected in IFR due to two main sources. The first one is the machine induced background, that is straight muons electro-produced by the beams from outside the detector. The maximum single hit rate is completely negligible in the barrel, due to the shielding effect of the endcaps. Calculations are in progress to evaluate the implications on the endcaps RPC layers.

The second background source is due to the RPC detector itself. Tests have shown that the single hit rate is below 1 kHz/m^2. The probability to have a noise hit in the trigger uncertainty window of 1 μs is completely negligible.

Level 1 trigger carries a fixed latency of 11.5 μs with a maximum jitter allowance of 0.5 μs. As the minimum time between successive triggers is 2.2 μs, the readout of front end electronics must be performed into the same time. The expected average trigger rate is less than 2 KHz.

Front end electronics cards will perform first stage processing of induced pulse from RPC. The following are mandatory requirements for FEC boards:

1) Must be stationed close to the RPC to avoid signal degradation;
2) Must contain the minimum number of components in order to maximize mean time between failures (MTBF);
3) Must be able to handle a minimum of 16 strips/card in order to reduce the total number of cards;
4) Must have high reliability since FEC electronics are inaccessible;
5) Must use low power logic wherever possible to reduce power requirements.

The large number of readout channels implies more than 2,500 front-end cards.

All the Barrel cards and about one half of the Endcap ones will be installed inside the IFR gap, between two successive iron plates just over the RPC layer, thus as close as possible to the end of the strips. To fit in this narrow space implies to have FEC cards as thin as possible. Thus SMD components are a must.

At the time of writing this paper a unique front-end input stage for negative signals has been considered. Due to the bi-dimensional readout scheme, strips provide both negative and positive signals. Although the card we are going to describe has been designed for negative pulses, however a further front-end card with only a different input stage will be realized for positive pulses.

2. FEC Description

The RPC is a low noise detector with a good signal to noise (S/N) ratio (better than three). If working in streamer mode, minimum pulse charge is about 100÷150 pC, depending on the gas mixture, with rise time of 2÷4 ns and amplitude of the order of 300 mV. Such being the characteristics of our detector (S/N>3), instead of using a fast (and expansive) comparator, we have opted for an input configuration where an RF amplifier (gain>50) feeds a fast TTL buffer (74F240).

FEC input stage (see the block diagram in Fig. 2) is connected directly to the strips and operates continuously without regard to the trigger. Each strip acts as a transmission line with a discriminator at one end.

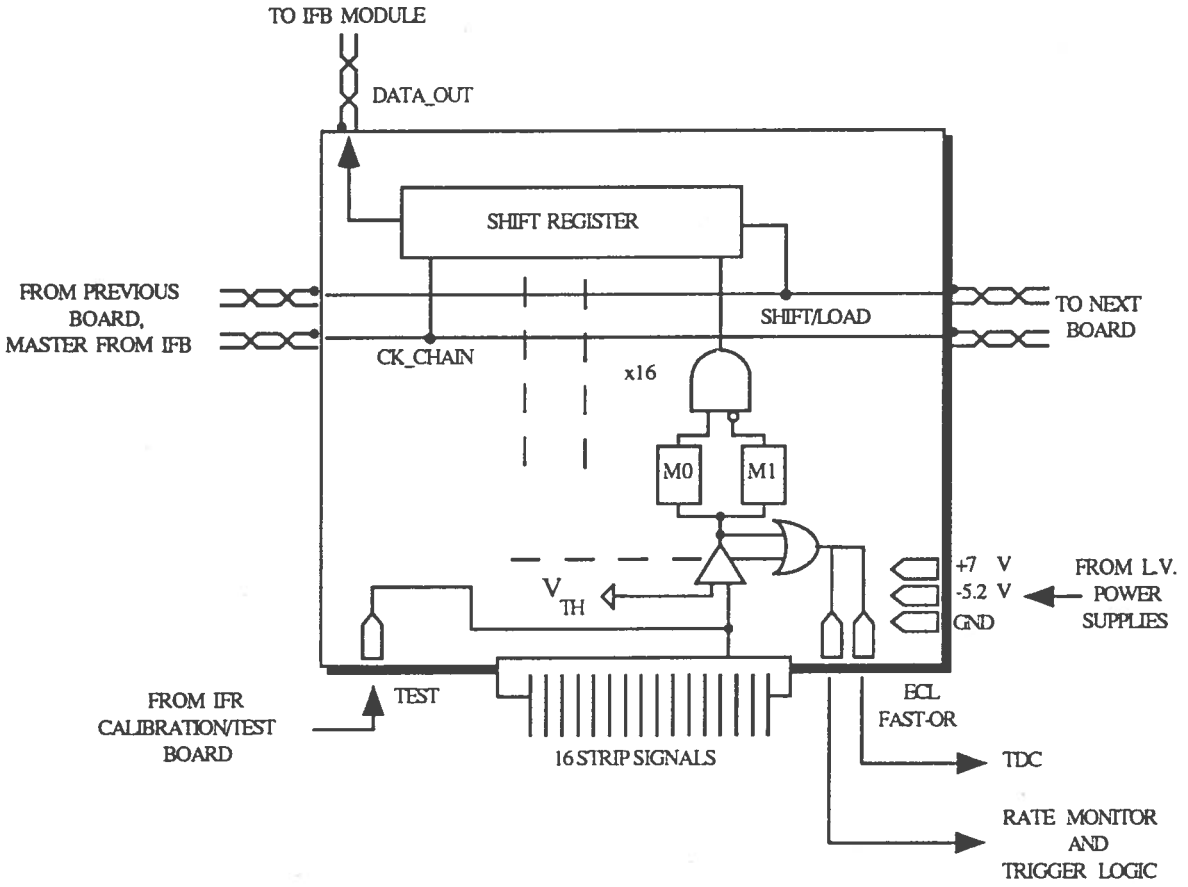


Figure 2 - FEC Block diagram.

Tests on the strip line behavior have shown a propagation speed of about 20 cm/ns [8,9] with attenuation worsen but comparable with that of a coax cable.

The input stage feeds a dual bank of monostables, to get noise reduction, and a PLD programmed to provide a FAST-OR of the board (Fig. 3).

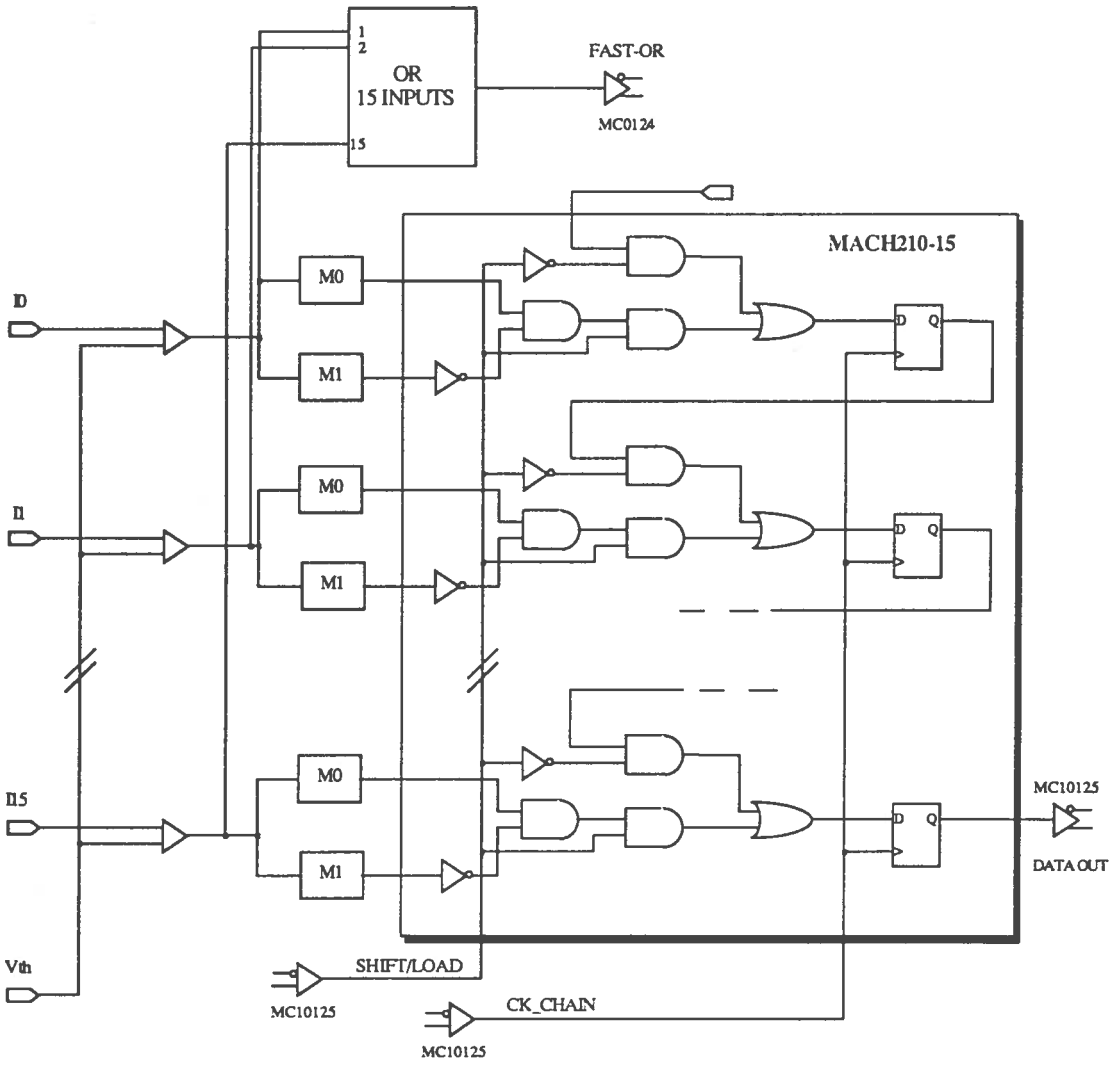


Figure 3 - FEC functional block diagram.

The double one-shot system enables strip data collection only during the trigger jitter window, of about 1 μs, thus reducing possible noise coming from the RPC detector approximately by a factor 10.

Monostable's outputs are hooked to a MACH-210AQ PLD device acting as shift register parallel-in/serial-out, sending data to the following FIFO memory board (IFB).

On the occurrence of a trigger, a Shift/Load signal together with a sequence of 16 clocks are produced in the IFB. The Shift/Load signal loads the pattern into the shift register while the following clocks shift data serially out of the board. Serial data from 64 FECs are connected to the FIFO board (IFB) (Fig. 4) which is located close to the apparatus in accessible points.

With this architecture, a failure of a FEC board will not affect data taking from the other boards.

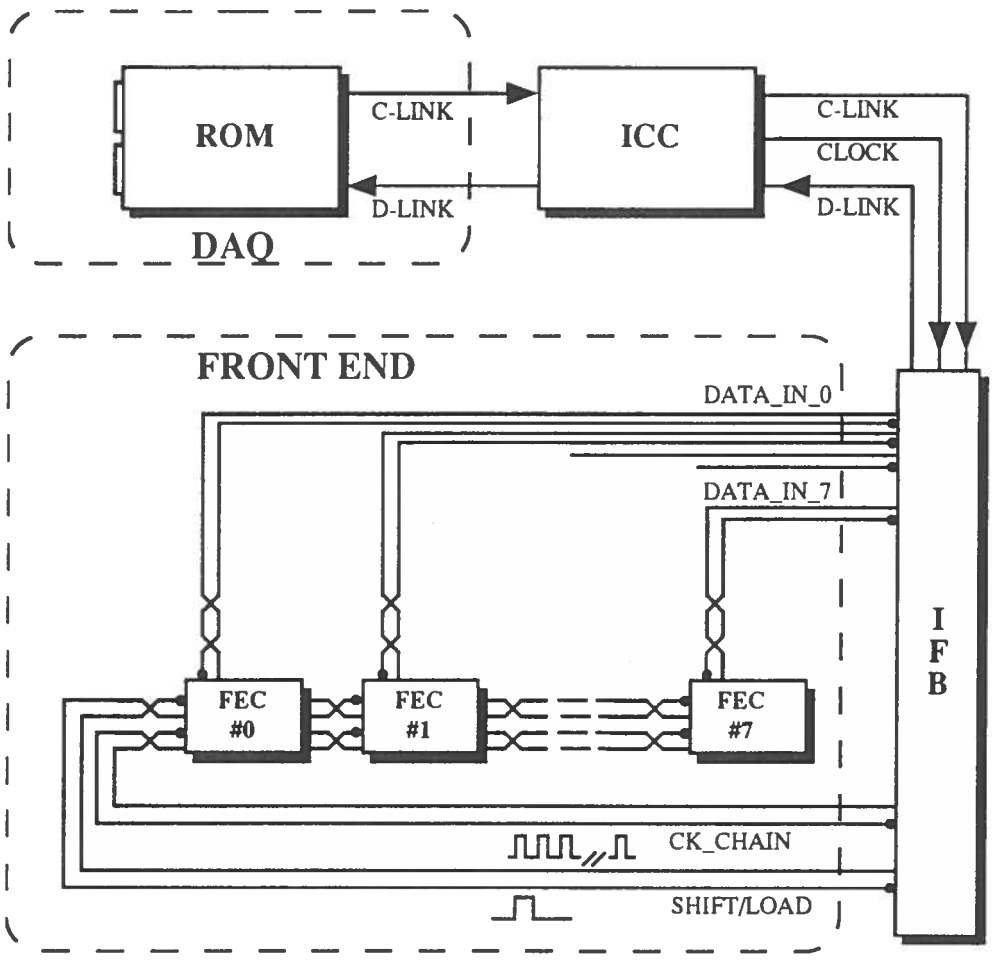


Figure 4 - Front-end readout mechanism.

2.1 FEC Input stage

The design goals for the FEC input stage (refer to the schematic in the appendix A) are:

1) Low cost, due to the large number of channels (~42,000);
2) Time walk (Fast-OR jitter) less than 2 ns for input signals;
3) To serve 16 input channels, thus implying SMD components;
4) To have good inter-channel characteristics for minimum crosstalk;
5) To have high reliability since FECs are inaccessible;
6) To use low power logic wherever possible to reduce power requirements;
7) To be fault tolerant: a failure of a single channel should not affect other channels.

Strips are hooked to the FECs via a 34 pin connector (3M type 3431.5002 or equivalent with ejectors). Strip signals numbered from I_0 through I_{15} are first shaped (two diodes LL1N4148) and then closed on the characteristic impedance of the strip via resistors R_0 (Fig. 5), and then AC coupled, via ceramic chip capacitors $C_0 \div C_{15}$, to the base of the $Q_0 \div Q_{15}$ transistors (a low cost high frequency transistor acting as an amplifier).

PNP transistors $Q_0 \div Q_{15}$ (BF-579, SOT 23 package, Ft of 1.7 GHz), are hooked in a common emitter configuration with an inductor on the collector (to provide a large gain) and biased via R_B's to about 1 mA of emitter current.

At 1 mA of emitter current, voltage gain of this stage is about 50. Voltage gain can be varied through the R_B resistor. In the quiescent state the collector voltage is about 20 mV, well below the

V_{IL}=0.8 Volt of the buffer. To achieve a low level at the output of the 74F244, the collector voltage must rise at values greater than V_{IH}=2 Volt.

In the event of a hit, the voltage on the collector of the transistor will rise very fast to a high level and then decay rather slowly with a time constant of 30÷50 ns.

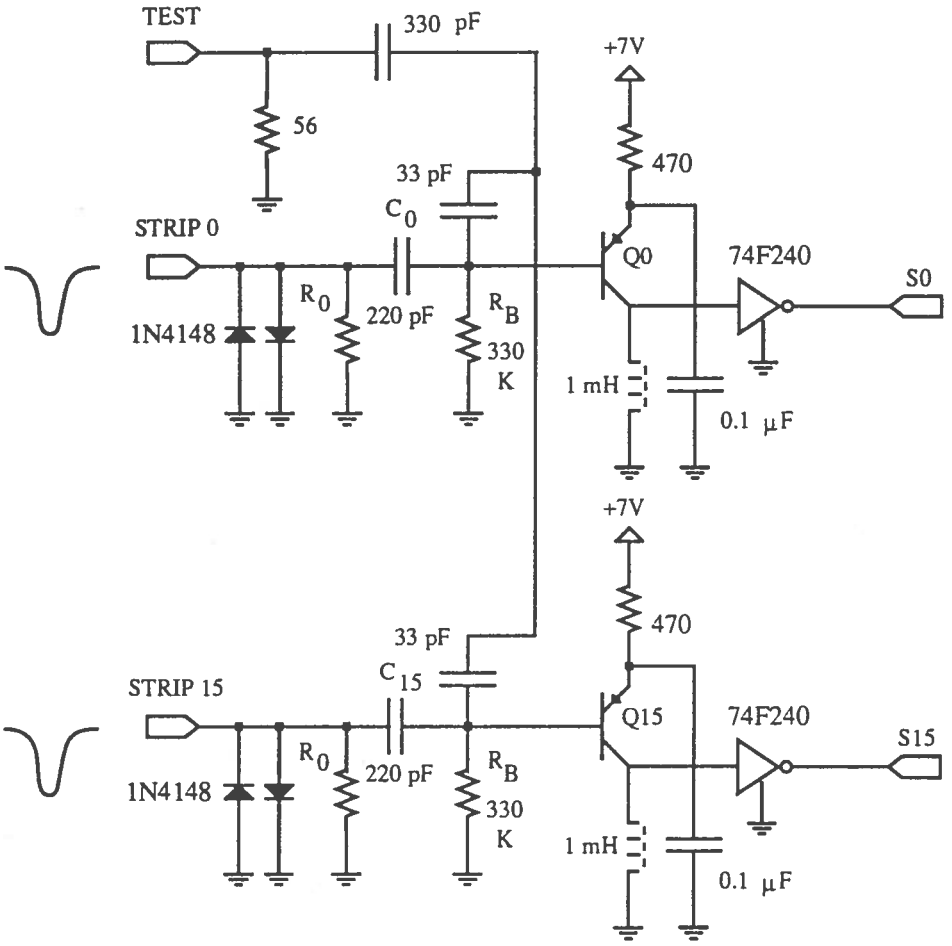


Figure 5 - Front-End Card input stage.

The resistor of 470 Ω on the emitter path to the V_{cc} (+7 Volt) is inserted for protection purpose. In fact, should a transistor fail going short between emitter and collector the board supply would increase of just 15 mA. The 0.1 μF bypass capacitor from emitter to ground is inserted so that the AC behavior of the transistor is not influenced by the protecting 470 Ω resistor.

The inductor whose value is not critical (1 mH TDK code NL4532T-102J) has a maximum DC resistance of 40 Ω, which limits DC voltage on the collector to about 20 mV. For input pulse above threshold, discharging of inductor L provides a pulse stretching action.

The positive signal on the collector of the transistor is DC coupled to the 74F240 acting both as a buffer and discriminator. When there is a hit on the strips, if the signal resulting on the collector of the transistor is above the minimum V_{IH} of the 74F240, a negative signal will appear on the output of the buffer.

Although simple in principle this design has proved to be very effective since we used it on the L3 detector where it is been working for 3 years without troubles [8-15].

2.2 Fast-Or generation

The digital output of the 74F240 feeds a CE16V8Q-10JC which is programmed to behave as 16 input AND so that if one strip fires above threshold, a low level will be set at the output of the PLD thereby forming a 16 input OR. A quarter power PLD has been chosen to achieve lower power consumption from the board.

Threshold measurements

Even with the best discriminator, the threshold cannot be specified by a single value as it can vary as a function of input rise-time, temperature, input signal duration and rate. Consequently threshold measurements have been performed with signals of different input rise-time and widths.

We have built and evaluated 5 boards employing different types of RF small signal transistors: BF-579, BFT-93 and 2N3906 (SOT 23 package). Furthermore inductors of different manufacturers have been also tested. We show performances of a board equipped with the BF-579 transistors in Fig. 6 where the threshold has been measured with a R_b resistor of 680 kΩ.

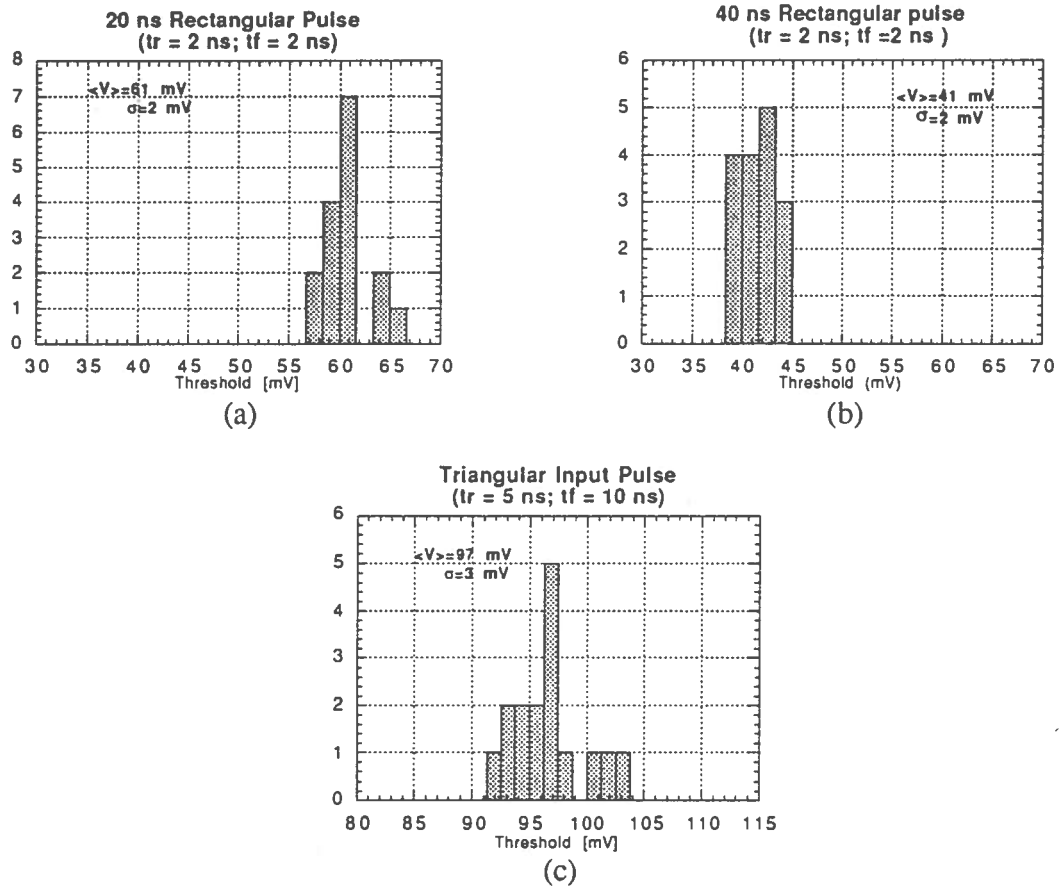


Figure 6 - Threshold measurements, all channels (BF-579 transistors; R_b=680Ω).

Clearly changing R_b varies the amplification of the input stage and the threshold. In the following Fig. 7 the threshold behavior is shown as a function of R_b for rectangular and triangular pulses. Threshold behavior as a function of the pulse width is also shown.

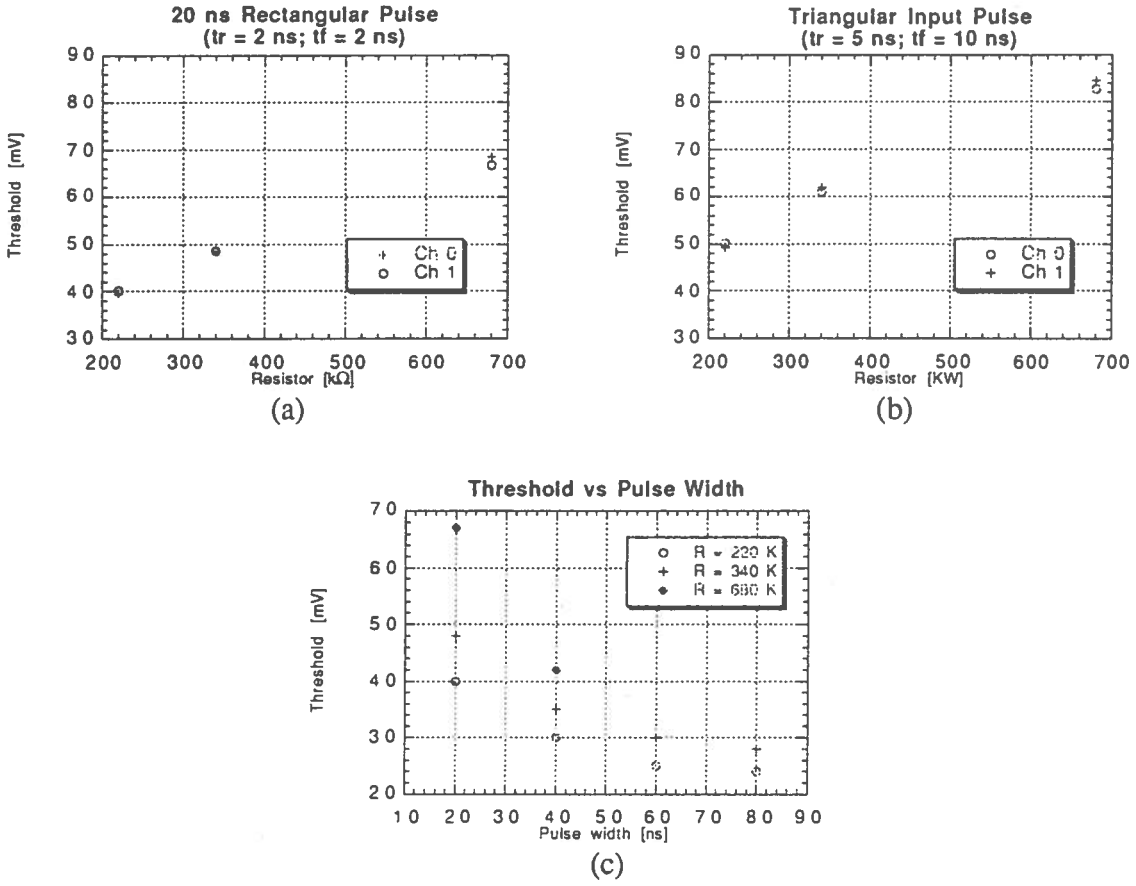
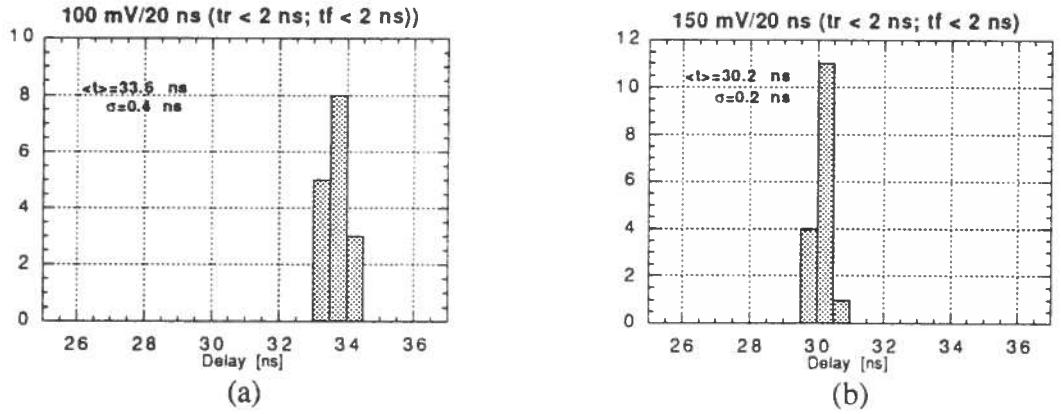


Figure 7 - Threshold versus R_b behavior as a function of different values of pulse width and shape for a board equipped with BF-579 transistors.

Propagation Delay Measurements

For timing measurements one of the most important feature of a discriminator is the in-out delay as a function of the overdrive voltage.

We have evaluated this delay with a a 20 ns signal as a function of the input amplitude in the 100 mV - 500 mV range (Fig. 8).



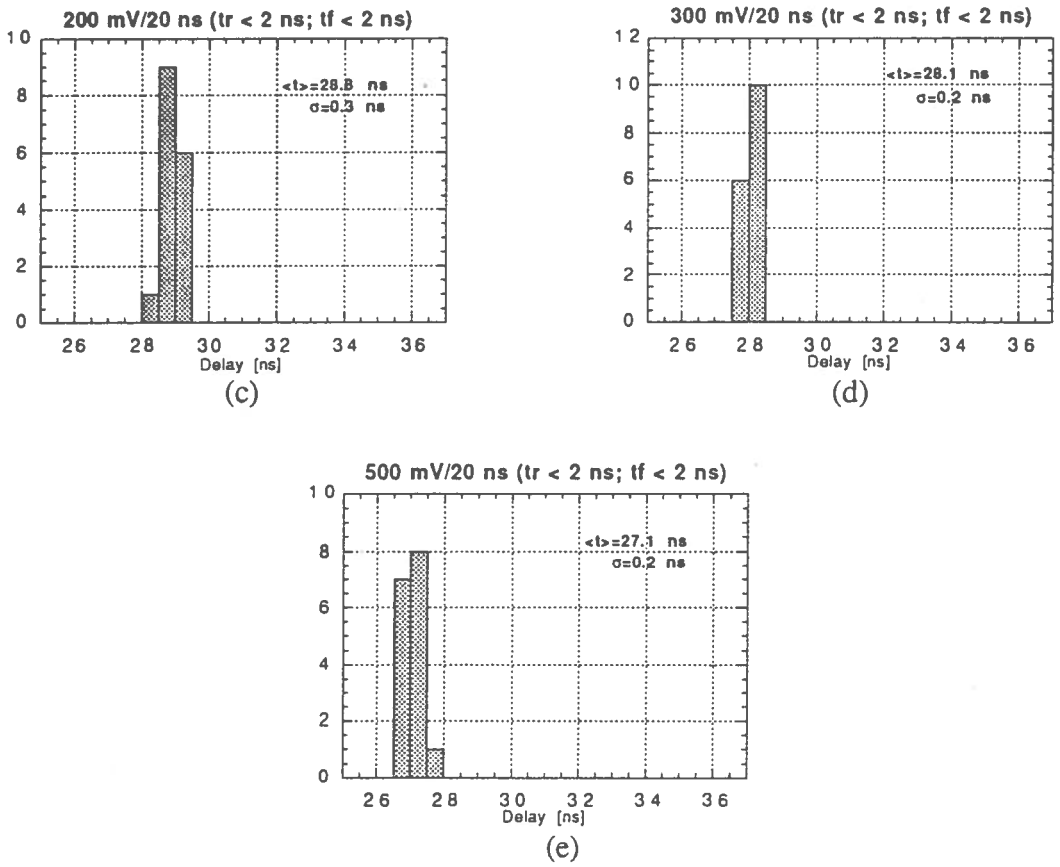


Figure 8 - In-Out delay as a function of the overdrive voltage for the input discriminator (R_b=680 Ω).

Time Walk Measurement

This has been evaluated by injecting a rectangular input pulse of 20 ns (tr ≤ 1 ns; tf ≤ 1 ns) in a 250÷600 V range (i.e. from below a typical RPC pulse) and measuring the time walk at the fast-OR output. For the first measurement R_b = 220 KΩ, while for the second one the R_b value is 680 KΩ. Time walk is about 2 ns for R_b = 220 KΩ.

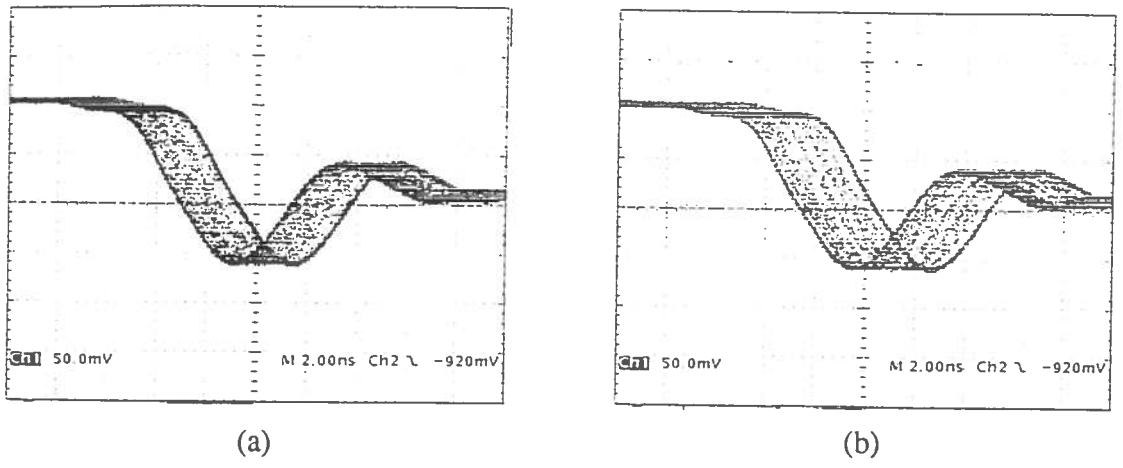
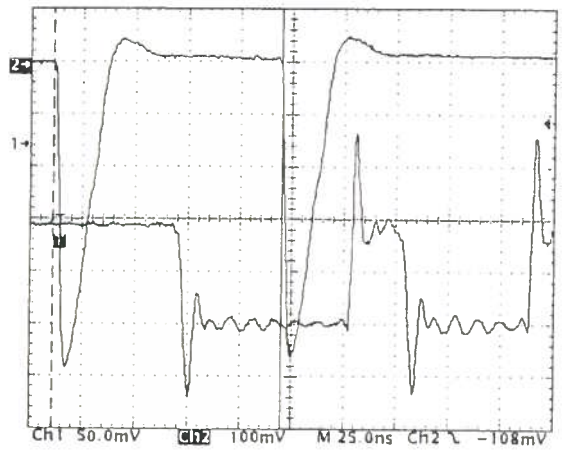


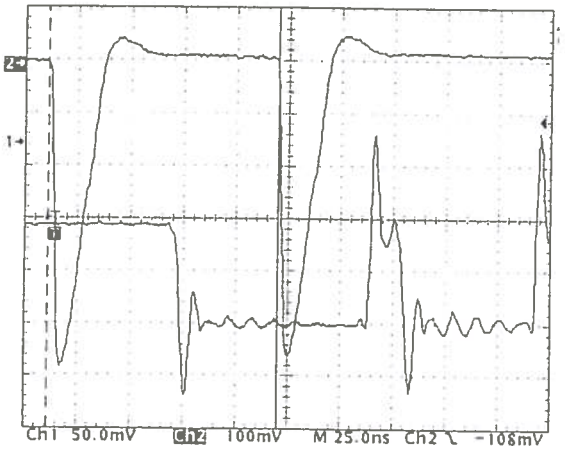
Figure 9 - Time walk ; Fig. (a) refers to R_b = 220 kΩ, while (b) to R_b = 680 kΩ.

Double Pulse Resolution Measurements

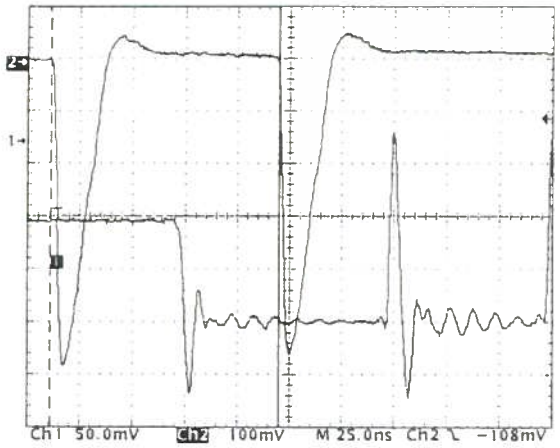
First we show that base resistor influences very little double pulse resolution (Fig. 10 a, b, c). In Fig. 10a, 10b and 10c two streamer-like pulses spaced by 100 ns (top signal) are hooked at the input and recognized (bottom signal) as such in all the three cases (R_b = 220 kΩ, R_b = 330 kΩ and R_b = 680 kΩ). Then a large pulse followed by a pulse just over threshold is injected to put in evidence a short dead-time effect (<100ns).



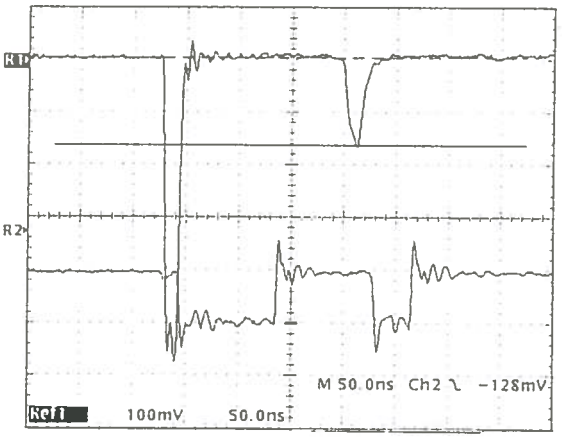
(a)



(b)



(c)



(d)

Figure 10 - Double Pulse Resolution Measurements. Fig. (a) refers to R_b = 220 kΩ, (b) refers to R_b = 330 kΩ, (c) corresponds to R_b = 680 kΩ.

Crosstalk

Crosstalk is an important feature of a multi-input discriminator. It has been measured by injecting two pulses about 20 ns width, 1.91 Volt in amplitude (see Fig. 11, R1 trace), in two consecutive even channel and observing the induced pulse on the channel in between at the scope (R4 signal, about 20 mV). Collector signals on fired channels are also shown (R2 and R3 signals).

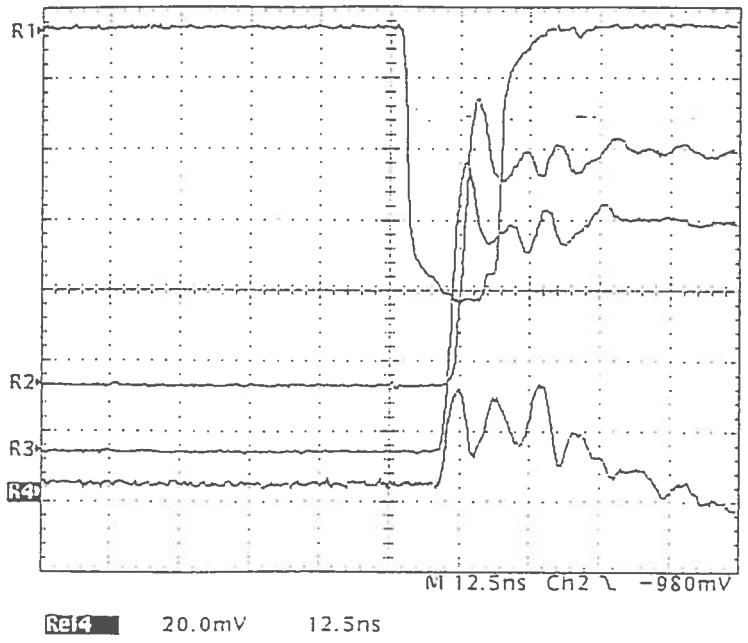
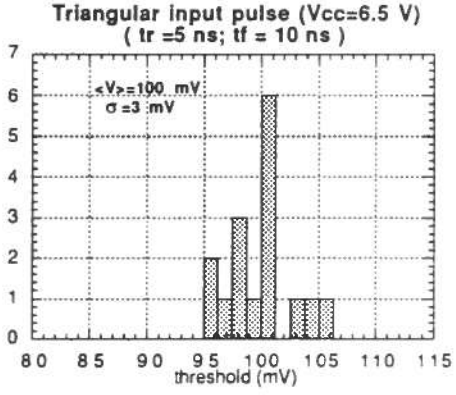


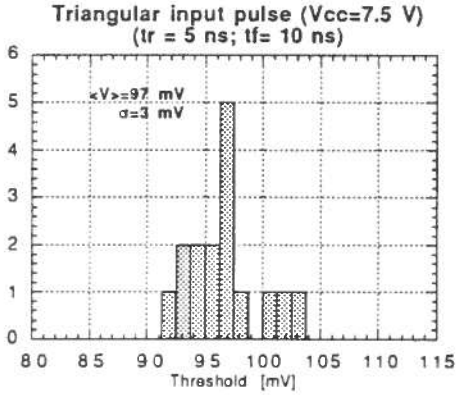
Figure 11 - Crosstalk measurement (see text).

Threshold versus power supply dependence

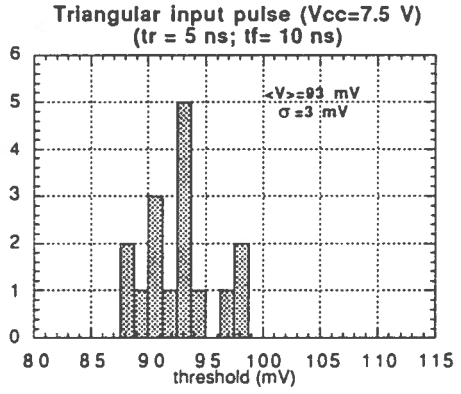
In Fig. 12 thresholds as a function of the voltage supply, using BF-579 transistors and TDK inductors, are reported. Thresholds are varying from 95 to 105 mV for triangular signals as appear from the enclosed diagram.



(a)



(b)



(c)

Figure 12 - Threshold as a function of the FEC voltage supply for BF-579 transistors.

Monostable testing

Outputs of the 74F240 are also connected to a dual bank of monostable. The first and second bank provide, respectively, 11 μs and 12 μs output signal. Stretching is necessary to achieve buffering during the trigger latency, while noise reduction is accomplished identifying strips fired within the 1 μs time window (obtained as difference between the two previous pulses) corresponding to the trigger latency jitter (11.5±0.5 μs). Signals placed outside the time window are rejected (Fig. 13).

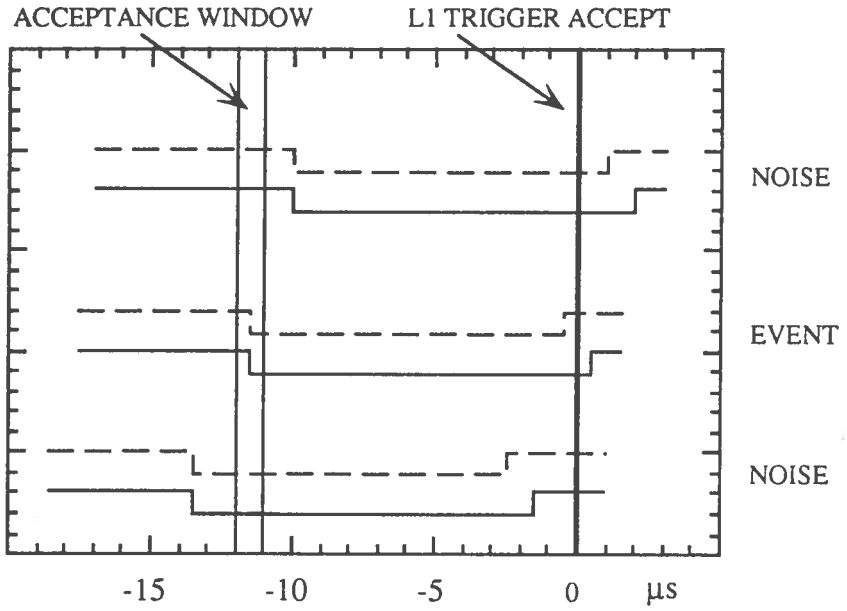


Figure 13 - Noise rejection.

As regards the monostable, we have evaluated the 74LS221 against the 74HCT221, with the former being somewhat cheaper, but with the HCT part sinking near no current, while the 74LS221 at worst case can sink 11 mA per chip for a total of 170 mA per board.

What matters for the FEC design is the stability of pulse width (i.e. changing the part, how much does pulse width change). Here the 74LS221 is much better.

In the (Fig. 14) below we show output pulse widths of a bunch (more than 100 parts) of 74HCT221 in a dual in line package. On the SMD package we have observed even worsen results (jitter more than 1 µs).

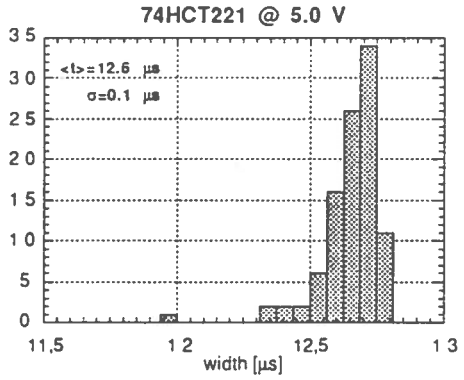


Figure 14 - Widths of a bunch (more than 100 parts) of 74HCT221.

By contrast (Fig. 15) we show the behavior of two bunches of 74LS221 (32 chips) mounted on two FEC boards, one hooked for a 11.5 µs width, the other is hooked for 12.5 µs. Negative pulse width is obtained using 1% resistor and 5% capacitors.

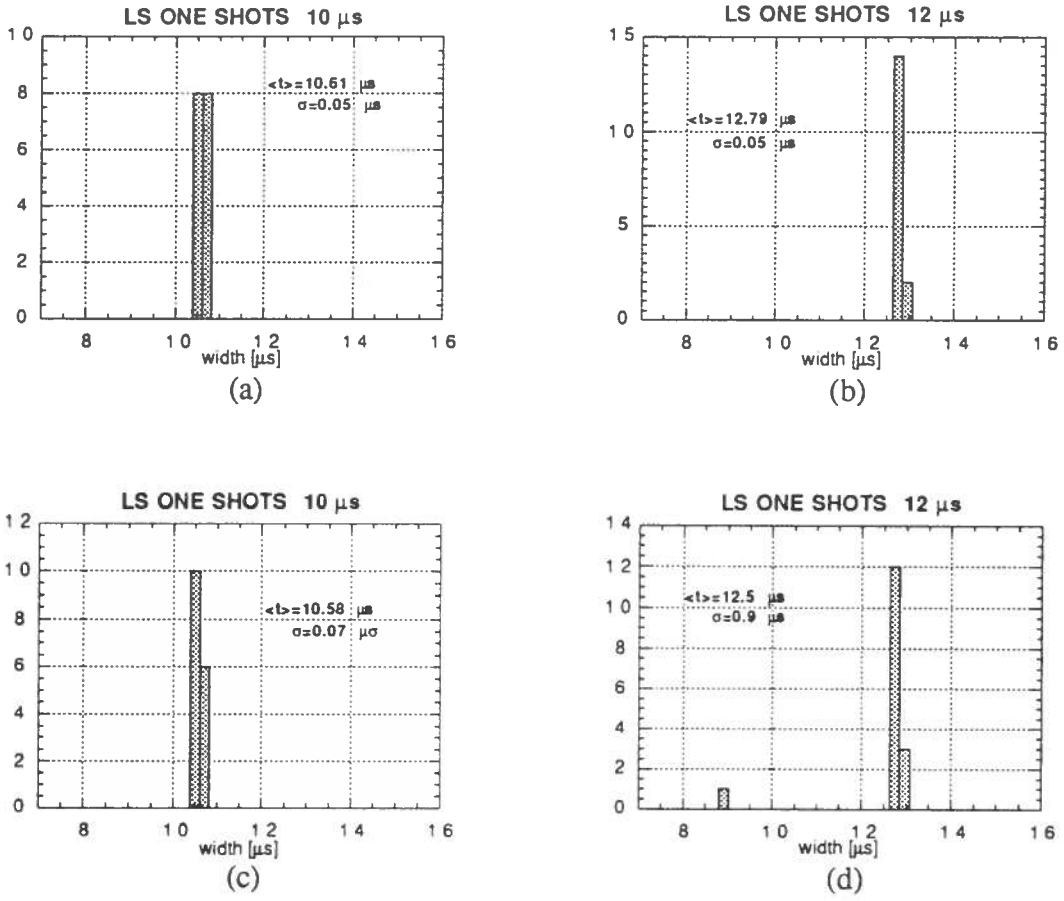


Figure 15 - Behavior of different bunches of 74LS221 chips.

Due to these results, to use HCT parts requires to widen the time window. This in turn would increase the potential noise.

Therefore 74LS221 will be used. Pulse width stability will be achieved by using 1% components (both capacitor and resistor). Inputs B and CLR of all monostables are tied to V_{cc}.

Negative outputs of the two monostable connected to the same strip are then made in anti-coincidence within the MACH 210AQ PLD.

2.3 Readout section

MACH 210AQ

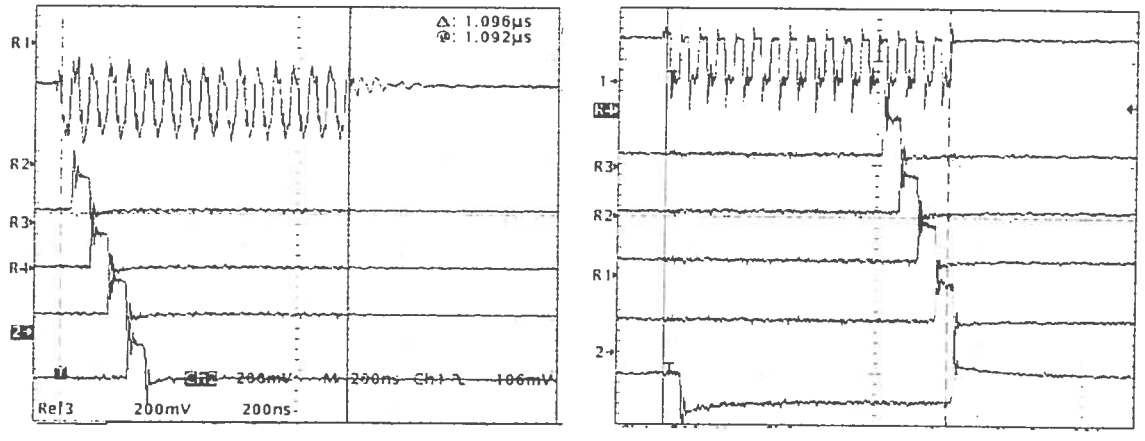
The CK_Chain and Shift/Load signals are produced by IFB module and transmitted in ECL differential format. Output of the MACH 210AQ is Data_out. Input (see FEC schematics in the Appendix) are labeled A_0 through A_{15} and B_0 trough B_{15}. First signal A_n (n=0 through 15) and B_n (n=0 through 15) are connected in anti coincidence. The positive resulting signals, assuming that the state of the Shift/Load signal is high, are connected to the parallel input of a 16 bit shift register (parallel-in/serial-out) and loaded in the first low-to-high transition of the CK_Chain clock.

When the state of the Shift/Load signal change to low, the 16 bit register acts as a shift register.

Thus, on the first clock (when a parallel load is made) the state of strip "15" is read; on the second clock (when the state of the Shift/load signal change to low) status of strip "14" is read and so on.

As CK_Chain is obtained in the IFB by dividing a 59.5 MHz clock (BaBar readout reference clock) by four, its period is 16 ns × 4 = 64 ns (32 ns low, 32 ns high). Thus a 15 ns MACH 210AQ will suffice. Also for this PLD we have chosen a quarter power version to reduce power requirements. Timing of Shift/load versus CK_Chain is not critical.

In the following plots we show CK_Chain versus the serial data out (which is active high) with different pulsed strips (strips 15, 14, 13 and 12 in Fig. 16a, strips 4, 3, 2, 1 and 0 inf Fig. 16b). Note that pulsing only strip 0 (bottom signal in Fig. 16b) data out will stay active (high) until strip no. 15 is read by the next CK_Chain train pulse. The MACH 210AQ chip has also additional inputs providing features useful in the lab and for diagnostic purposes: a serial in, reset and preset. Last two inputs, not used in the "run" will be handy in the lab to test the chip. Test_in serial input can be useful in the lab to acquire a chain of FEC in serial mode.



(a) (b)

Figure 16 - CK_Chain versus the serial data out (which is active low) with different pulsed strips (see text).

2.4 Test circuitry

A negative "NIM" test pulse will control the functionality of the front end transistors simulating an hit on all the 16 channels. This pulse is first adapted to the impedance of the line and then is AC coupled to the base of the Q_1 - Q_{16} transistors. Decoupling capacitor is 330 pF plus an array of 16 capacitor each of 33 pF.

2.5 Line drivers/receivers

Due to the required clock frequency, to assure reliable functionality, we have opted for ECL line drivers/receivers.

Line drivers are MC10124 (tpd 3.5 ns typical) while line receivers are MC10125 (tpd 3.5 ns). There are two differential output (through an MC10124FN) for the fast or (JN4 and JN5), plus one more JN3 for the serial data out of the MACH (these three connection usa an AMP MODU II connector 280.380.2).

Shift/Load and CK_Chain, produced by the IFB board, are connected each to a group of 8 FECs (FEC chain) through connector JN2 AMP MODU II mod. 280.378.2.

As the interconnecting twisted pair cable has roughly an impedance of 120 Ω, this component is foreseen on each FEC. However, only on the last FEC of a chain through jumpers P1 and P2 this connection is made so that all FECs boards are the same except for this two insertions jumper. Last FEC will be recognized by a cut in the PCB.

2.6 Power supply requirements

Power supply to the board is a +7 volt and a -5.2 voltage for the ECL components. On each board a low dropout regulator will produce a + 5 Volt starting from the input voltage of + 7 volts. Regulator actually used is LM2940CT made by National with an output capacitor of 100 μF.

We have also evaluated power supply requirements for a board with HCT monostable (power supply requirements about 200 mA on the + 7 Volt) against LS monostable (power supply requirements about than 300 mA). For the negative supply the required current is about 100 mA. At input line of power supply are foreseen two SMD fuse.

3. PCB layout

Layout of this board is made with four layer. Ground plane, power supply plane, component side with most of trace and bottom side with some other traces.

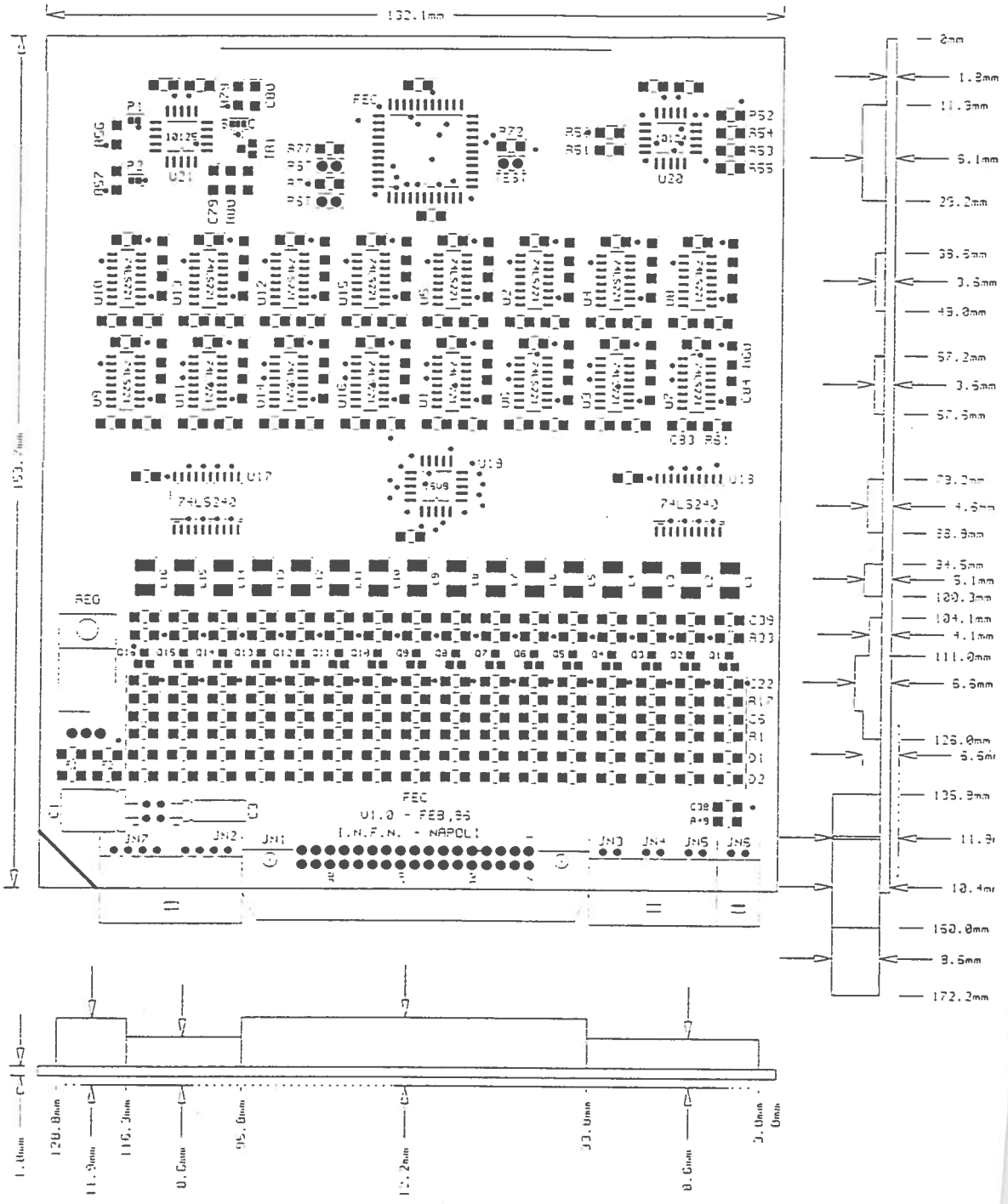


Figure 17 - Layout of the Front-End Card.

4. Conclusions

Taking into account price/performance ratio of the input stage, results are satisfying. A fast comparator, giving the best performances, whose price is about 3 dollars, would have been too expensive for more than 40,000 channels.

As far as regards the one-shot chip, use of LS parts is unavoilable to achieve a good stability. PLD components have been chosen in the quarter power version to hold current requirements down. The FEC-IFB interface is ECL differential to cope with the required frequency rate.

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Appendix - FEC Schematics