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## EBOFERA: A COMPANION FOR FERA ADC'S

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# EBOFERA: A COMPANION FOR FERA[1] ADC'S

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## ABSTRACT

A data transfer problem using FERA modules was found in a heavy ion nuclear physics experiment. The source of the problem was spotted in the handling of some signals on the FERA control bus.

A modification of this handling is proposed and performed by means of a new CAMAC-FERA control module, the EBOFERA. Furthermore this module has a number of useful features like the master gate and clear signals handling, event tagging, pattern unit and event counter.

## 1 - INTRODUCTION

In the last generation of experiments with heavy ions at intermediate energies the need to reconstruct as completely as possible every single event has called for the construction of $n\pi$ detectors for charged as well as neutral particles and photons with high or very high

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[1] FERA is a trademark of LeCroy Corporation

granularities (in some setups up to several thousands of detecting elements are counted). It follows that the electronic Front End has to be able to handle the corresponding number of logic and/or analogic signals coming from those elements. In spite of the high granularity of the setups, the average multiplicity of the events is seldom higher than few tens, but the importance of measuring cross sections with minimum bias can normally imply a counting rate of tens of kHz . Then the use of very fast bus or protocol (like, e.g., FERA ...) for data trasmission is unavoidable.

Finally the low multiplicity on a physically long bus can be a source of reading error of data if not correctly handled.

In this paper we report on a problem of this kind that arised during a nuclear physics experiment involving heavy ions at intermediate energy (around 10MeV/nucleon). The analysis of the problem will be briefly illustrated as well as a possible solution. The CAMAC module EBOFERA (Extended Boiano-Ordine FERA), or "EBO", that actually was designed to be implemented in the experiment Front End to fix the problem will be presented in some details. The several useful features of the module will be discussed.

## 2 - PROBLEM and SOLUTION

In an experiment performed at CE Saclay(France) using a $^{35}$Cl beam of around 10MeV/nucleon[1], delivered by the complex FN Tandem+superconducting booster, impinging on a $^{92}$Mo target, there were gamma and charged particle to detect. The total number of parameters to handle was around 200, including particle and gamma energies and time signals for the coincidence events. The ADC Front End was made up of CAMAC modules manufactured by several companies (LeCroy[2], Silena[3], Gan'elec[4], Atenix[5]) hosted in more than one CAMAC crate. Data from ADC's, charge and peak sensing, were read through the FERA "bus" and transferred to a VME system by means of a FERA driver LeCroy 4301 and a FERA-VME interface CES HSM 8170[6]. The use of the FERA "bus" (tipically 100 ns reading cycle) was justified by the high counting rate (several kHz) involved in the experiment. The time diagram of the transferring procedure between the FERA driver and the HSM is sketched in Fig.1 (see also LeCroy or Silena or Gan'elec instruction manuals).

The main logic control signals involved in the dialog are the REQ (request signal), the REN (read enable), the PASS, the WST (write strobe). The REQ is logically, and eventually "electrically", put on by any module that has converted data to be transferred to the HSM and it stays on until all data of the module have been read. After that it is logically

and electrically put off and the PASS signal is put on to the next module in the chain of the Front End.

Then this PASS signal becomes the REN signal for the next module, for which the reading procedure starts. If this module doesn't have any data to transfer, it simply activates the PASS for the following module and so on for all the modules of the Front End. During the WST signal every single data (consisting of 16 bits) is actually transferred to the HSM.
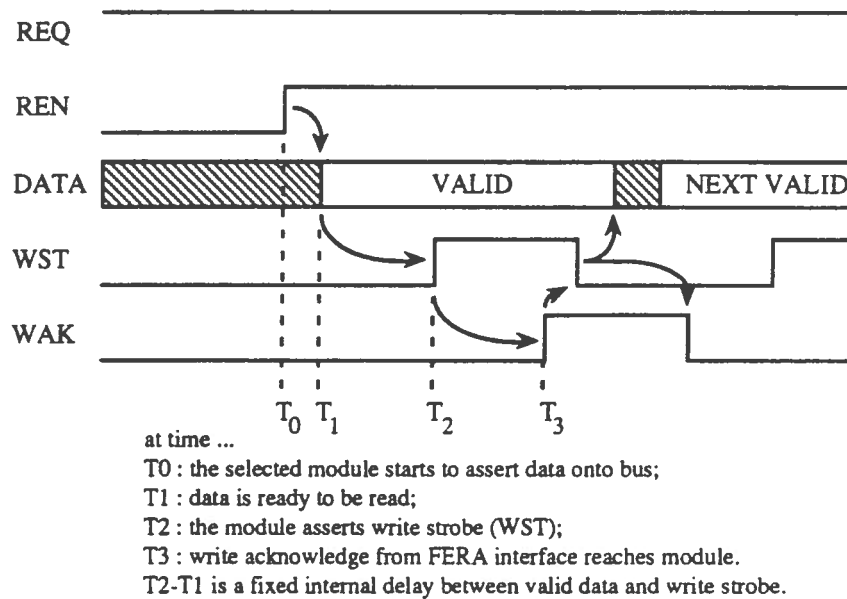


at time ...
T0 : the selected module starts to assert data onto bus;
T1 : data is ready to be read;
T2 : the module asserts write strobe (WST);
T3 : write acknowledge from FERA interface reaches module.
T2-T1 is a fixed internal delay between valid data and write strobe.

**Fig.1.** FERA data transfer (normal case).

During the setting up of the experiment it was noted that some data were not correctly transferred to the HSM, especially the first datum (the so called "header word") of last modules in the chain.

Using a logic state analyzer it was possible to see that, in given circumstances, not so rare, depending upon both the bus length and the presence of FERA modules of different manufacturers, the last module receives the REN, but in the mean time on the REQ there is a tension fall: this will, in general, imply a wrong transfer of the header word. Some time later the REN reappears and the rest of the data are correctly transferred. These data are useless, due to the fact that the information on which module was transferring is lost (this information is carried by the header word). A possible interpretation of these findings is as follows. The REQ signal is OR'ed between all modules. Those who have data to transfer put on the REQ line certainly logically, not necessarily electrically. The electronic that puts on the line could have slight differences, in "strength", from a module to another (see Appendix 1 for further details). As a consequence it could happen that some modules, who

have teh REQ logically active, have it electrically off if other modules, with a "stronger" REQ, have it electrically on.

All that could in principle happens especially if the modules are manufactured by different companies and also if the FERA bus has a physical length big enough to make the propagation times of the signals comparable with the commutation times of the ECL buffers. These two "uneasy" conditions are met in the present case (see Fig.2a-2b-2c).
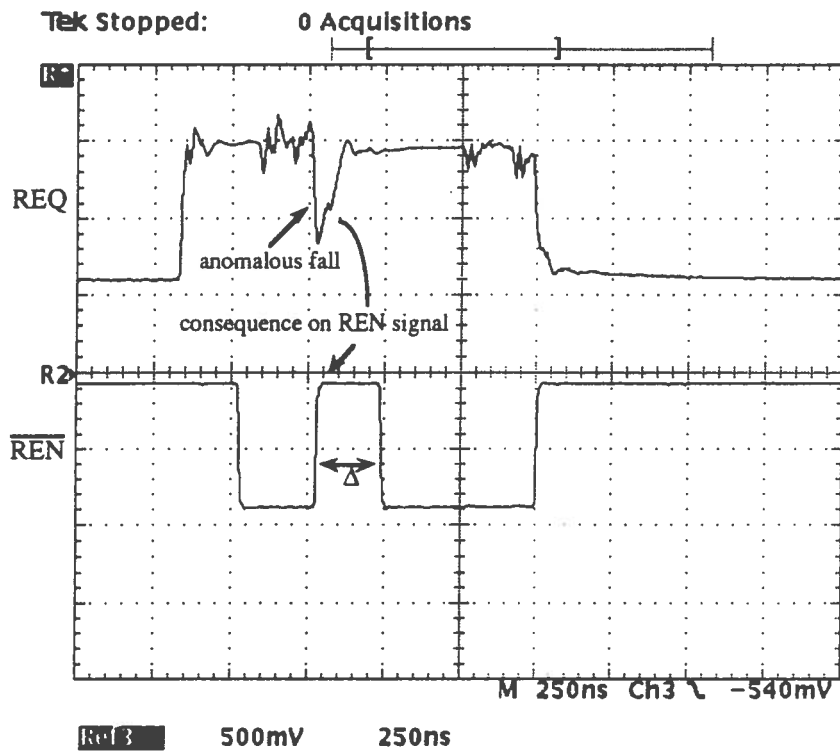


**Fig.2a.** Incorrect FERA data transfer. REQ-REN time diagram at oscilloscope. Δ width due to ADC Driver internal delay (see Fig.2b).
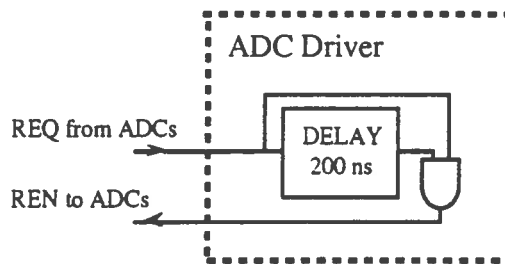


**Fig.2b.** The LeCroy 4301 ADC Driver is provided with internal delay between REQ and REN signal.

If several modules cooperate in keeping on the line, the achievement of the data transmission, and then the falling of the REQ of one of the modules, could in general be absorbed without any problem. In any case if the last module, that has data to transfer, had

the REQ electrically off, there will be no REQ signal on the bus for the time interval between the end of the data transmission from the module before the last and the moment the last module turns on electrically its own REQ.

The temporary fall of the the REQ is propagate until the FERA driver, that will remove the REN from the bus. Since the last module had already received the PASS signal from the previous module, it starts putting on the data bus its header word and prepares the WST. In the mean time the removal of the REN by the FERA driver reaches it. As a consequence it releases the bus when the WST is still on. All that will produce the transfer of a non stable, and in general not right, datum.
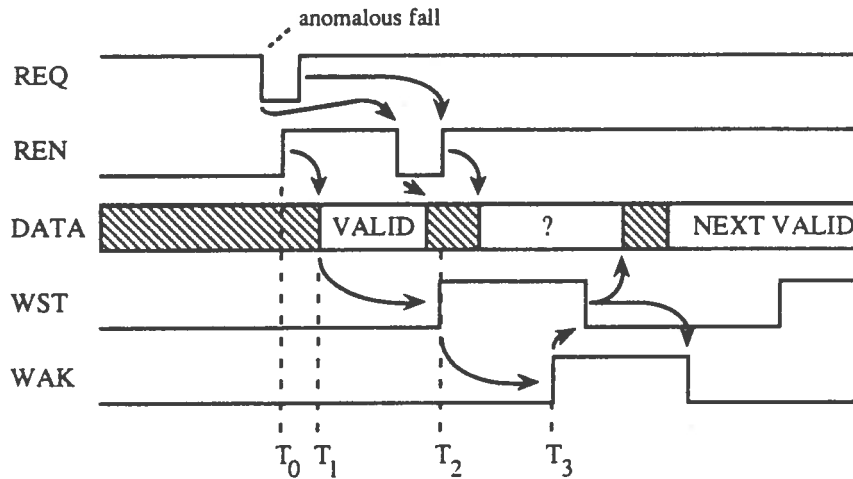


**Fig.2c.** Incorrect FERA data transfer.

The same problem, on REN signal, arises when modules use individual gates or when faster modules follow, into REN-PASS chain, slower modules. Faster and slower in the sense of the time needed to the module to have converted dta to transfer. This time is a characteristic of the converter type (peak sensing ADC, QDC, TDC ...) and depends upon the number of input that fired. In this case it can happen that the slower module leaves the REN signal to propagate to the following module that will keep it since it has data to transfer and starts transferring data. If, in the mean time, the previous module ends the conversion, it has now data to transfer and will now keep the REN signal, removing it from the faster module that was transferring data. The result is similar to the previous case: unstable and then wrong data could be transferred.

Afterward the REQ will be again on, and so the REN, and the rest of data are correctly read. On the spot it was found a patch. The REQ signal was removed from the bus and it was sent to the FERA driver only by the last module in the Front End, provided that this had always data to send. So an ADC was "sacrified" and used as a kind of "pattern unit". It

became clear that for the future a new module was needed to be used in conjunction with the FERA driver to avoid the kind of problems reported so far. Moreover a more performing event tagging procedure and variable dead time implementation were also needed.

## 3 - The EBOFERA.

The aim of this module is to solve the problem of the 'restart' of the REN. This restart is a consequence of anomalous oscillations during the reading out of an event. The problem is solved in the following way. The EBO behaves as a filter (see figg. 3 and 4), as far as the REQ signal is concerned, between the whole Front End module chain and the FERA driver.
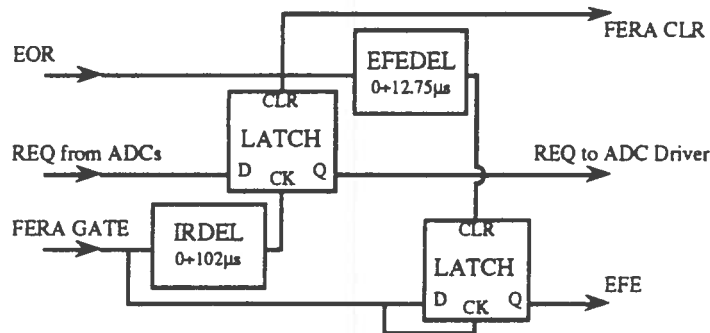


**Fig. 3.** Schematic diagram of REQ, CLR and EFE
signal generation into EBOFERA module

The REQ of all modules of the Front End are linked together, OR'ed. The REQ line is now sent to the EBO, instead of the FERA driver as in normal FERA. The EBO will "charge" the state of the line after the user programmable delay IRDEL, that starts as soon as a GATE signal is detected. Normally this delay, that can be set in the range 0-102μs, must be longer than the maximum conversion time of all ADC modules present in the Front End. Moreover it has also to take into account the time jitter between individual gates, which depends upon the time coincidence window chosen for the experiment and the shaping time of the slow amplifiers. The REQ line will be charged by means of a flip-flop in order to send it steadily to the FERA driver until the read-out has been completed on all the modules of the Front End, that have converted data. The propagation of REN-PASS signals controls the completion of the reading procedure on each individual module. The PASS of the last module in the chain is sent back to the EBO (EOR - End Of Readout input). The activation of this signal in input to the EBO will reset the REQ flip-flop and terminate the read-out of all the chain. Furthermore, at this time, EBO generates CLR signal to reset all Front End modules.

To complete the FERA system control EBO also generates Enable Front End (EFE) signal that can be used as GATE "VETO" suitable to start and stop the acquisition of events. Another useful feature of this module is its ability to detect error conditions like breaking off of REN-PASS chain or anomalous transaction between FERA modules and FERA/VME interface.
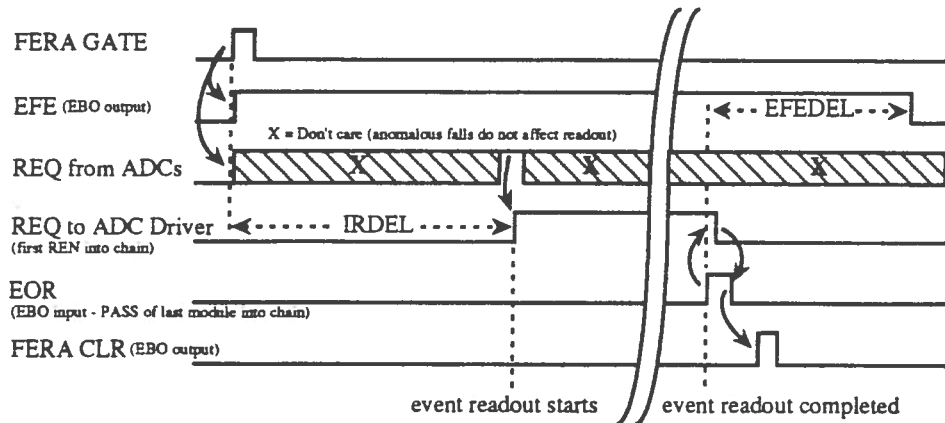


**Fig. 4.** Time diagram for EBOFERA as bus Master

The EBO, implemented as a CAMAC/FERA module, has other features. The following options can be selected individually :

1) event marking: it generates a coded word to mark the beginning of event for event packing;

2) two mode counter: on GATE or REQ signals (useful for event building in FERA multi-branch application);

3) external pattern reader: up to 96 bits.

## 4 - EBOFERA functional description

The EBOFERA (Extended Boiano Ordine FERA) is a three slots CAMAC/FERA module. It performs its main function as Bus controller (see previous paragraph) if it is configured in Master mode. Moreover the Master mode allows the event marker and pattern reader and counter options to be enabled. If it is initialized in Slave mode the EBO does not perform the Bus control, in other words it behaves like any other FERA Front End module.

Furthermore the EBO can also be used as CAMAC pattern/counter module for pattern and counter read-out. In this case EBO must be initialized as Slave.

In Tables Ia, Ib and Ic are reported internal registers with CAMAC function.

| name | read | write | size(bit) | description |
|---|---|---|---|---|
| MODE | F0 A0 | F16 A0 | 8 | operating mode selection |
| VSN | F0 A14 | F16 A14 | 8 | Virtual Station Number |
| EFEDEL | -- -- | F16 A2 | 8 | Delay between CLR and EFE generation |
| IRDEL | -- -- | F16 A3 | 8 | Delay between GATE and EBO REQ test |
| PRSC | -- -- | F16 A4 | 4 | prescaler - counter rate division - $\log_2$ unit |

Table Ia. Registers for setup (Group 1)

| name | read | size(bit) | description |
|---|---|---|---|
| PATT [0-7] | F1 A(0-7) | 12 | 8 pattern words |
| NZWORD | F1 A8 | 9 | Non Zero Words, pattern: bit 1-8, counter: bit 9 |
| COUNTER | F1 A15 | 12 | counter word |

Table Ib. Registers for CAMAC read out (Group 2)

| name | function | description |
|---|---|---|
| Test LAM | F8 A[X] | return q=1 if EBO has non zero words |
| Clear REGs1 | F9 A[X] | clear group 1 registers |
| Clear LAM | F10 A[X] | also send FERA CLR: all FERA modules into idle state |
| Clear Counter | F11 A[X] | clear counter content |
| INIT | Z | clear LAM and reset EBO state machine |
| INHIBIT | I | inhibit GATE input |
| CLEAR | C | like F9 + F10 + Z |

Table Ic. Other CAMAC functions (X = don't care)

## 4.1 MODE register

Different operating modes can be selected by means of the 8 bit "MODE" register. Bits and function mode have the correspondence reported in Table II.

Master/Slave

In Master mode the EBO performs the FERA Bus control in the way explained in the previous paragraph. It controls the REQ signal to send to ADC Driver and generates the signals (EFE and CLR) the system needs to perform trigger operations and read-out. In this operation mode the EBO must be the first module into chain (the first following the ADC Driver).

In Master mode can be useful to set event marker (Label On option) to pack events. Furthermore, if enabled, the EBO also performs pattern reading (up to 96 bits) and/or counter functions.

In Slave mode the module performs (if enabled) only pattern reading and/or counter functions. It is possible to enable the event marker, nevertheless this option becomes less significant in Slave mode. Only one EBO Master can be present, but there is no limitation about the number of Slaves.

| BIT | Function | Description |
|-----|----------|-------------|
| 0 | Master/Slave | 0/1=Master/Slave |
| 1 | Label ON | Event marker: 0/1= disabled/enabled |
| 2 | ZRM | Zero Request Mode (see text) |
| 3 | DIR | ADC driver position respect to the EBOFERA: 0/1=Left/Right |
| 4 | not used (free) | No function associated |
| 5 | Counter Mode | Counter Increment Mode: 0/1= REQ/GATE |
| 6 | Patt ON | Pattern reader: 0/1= disabled/enabled |
| 7 | Count ON | Counter : 0/1= disabled/enabled |

Table II. Correspondence between bits and
functions for MODE register.

## Label ON

It enables the EBO to write the event marker. As the REN signal reaches the EBO it write onto bus a coded word to mark the event (if option is enabled : Label ON = 1). The mark can be useful for event packing if the EBO is the first module after the ADC Driver so that the marker can be the first word of event.

## ZRM (Zero Request Mode)

After a GATE occurrence the EBO waits for the time interval selected by the user by means of IRDEL delay register then it tests the REQ input line from the other Front End modules.

Moreover when Patt ON and/or Count On option is enabled it is possible to make the EBO able to generate its own REQ signal if it has pattern and/or counter words to send[2]. By setting ZRM bit (ZRM=1) this features is enabled.

Instead if ZRM=0 the EBO set the REQ signal towards ADC Driver only if, after

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[2] The EBOFERA only performs zero suppression mode data packing for its pattern and counter words.

GATE if it is Slave and after GATE and IRDEL delay if it is Master, the REQ signal from other Front End modules is already present at its REQ input.

## DIR

The EBO has 2 connectors for FERA Control bus to allow the REQ generation control. If on connector 1 the REQ line is an input then the REQ line on connector 2 must be an output and viceversa. The REQ line is not a bus line for EBO. To free the bus cabling from topological restrictions or from uncomfortable connections this option allow to set REQ input and REQ output line for the 2 connectors. This different setting reflects the position of EBO to respect the ADC Driver. In other words the direction of data flow (left towards right or viceversa).

## InCount

It switches the counter to count or REQ occurrences or GATE occurrences.

## Patt ON

It enables the EBO to write pattern non-zero words (only zero suppression mode).

## Count ON

It enables the EBO to write counter content if it is changed to respect the previous event.

The EBO counter is provided with prescaler selectable from 0 up to 65536.

## 4.2 Other group 1 registers (Setup)

## VSN (Virtual Station Number)

Its content is the FERA Station Number. It is mandatory to set this register if pattern reader and/or counter are enabled (Patt ON = 1 and/or Count On = 1, see MODE register).

## EFEDEL (Enable Front End DELay)

FERA Front End modules require a minimum delay time between CLR signal and a new GATE occurrence to guarantee correct clear internal sequence. This minimum delay time is 2 µs for LeCroy 4300B QDC, 1.2 µs for Silena 4418V ADC, 500 ns for Gan'elec ADC812F and QDC1612F.

In Master operating mode EBO provides for generation of FERA CLR signal at EOR

(End Of Read out) input signal occurrence (see Fig.4). EBO EOR input must be linked to PASS of last module into chain (see Fig.5). EBO also provides for the generation of EFE Enable Front End) signal that must be used as VETO for eletronics generating GATE signal.

After CLR generation EBO waits an EFEDEL time interval then it removes VETO to allow new GATE to reach the FERA system.

By using EBO in Master operating mode it is mandatory to set EFEDEL register at maximum value of delay time as required by modules into system (i.e. if Silena 4418V and Gan'elec ADC812F are both present into system then 1.2 $\mu$s is minimum delay time).

EFEDEL is a 8 bit register and to allow delay time setting from 0 up to 12.75 $\mu$s (50 ns for each step).
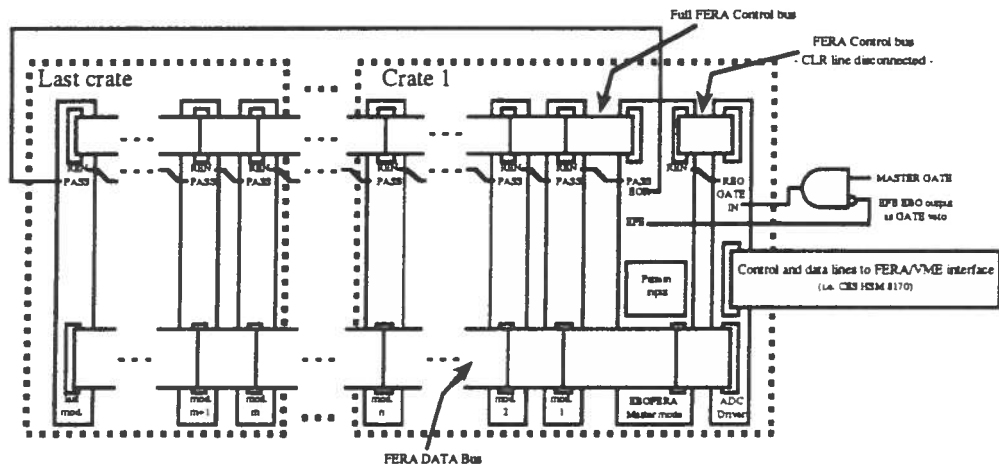


**Fig.5.** EBOFERA application in a typical Front-End

#### IRDEL (Inhibit Request DELay)

After GATE signal occurrence the EBO Master waits IRDEL time interval then it samples the REQ input from other Front End modules (see Fig.4). If it results an active signal then the EBO starts readout cycle by switching on the REQ output towards ADC Driver else EBO generates CLR signal and removes EFE by enabling the system to accept a new event occurrence.

IRDEL is a 8 bit register and it allows delay time setting from 0 up to 102 $\mu$s (400 ns for each step). IRDEL time interval has to be set at the maximum time the slowest Front End module needs to convert its data. The maximum conversion time is 8.5 $\mu$s for LeCroy 4300B QDC, 32 $\mu$s for Silena 4418V ADC, 24 $\mu$s for Gan'elec ADC812F and QDC1612F. Therefore if all module types are present into system then 32 $\mu$s is minimum IRDEL delay

time to be set.

The purpose of this delay is to prevent incorrect readout sequence through modules chain (see also par. 2 and 3).

PRSC (counter PReSCaler)

The EBO counter is provided with prescaler selectable from 0 up to 65536. PRSC is a 4 bit register and its representation of counter division is as $\log_2$ base.

## 4.3 FERA data format of EBOFERA.

In Fig.6 is shown the data block format of EBO. If Label ON bit, in MODE register, is set, then the event marker is the first word to be written by EBO onto bus at REN signal.
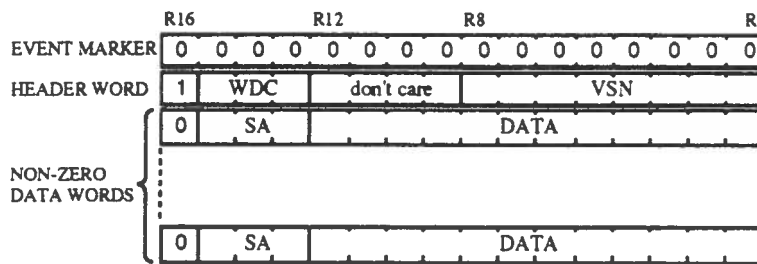


**Fig.6.** EBOFERA data block format.

The event marker is a zero word to be used for event packing. The EBO will be the first module into chain (the next one respect to the ADC Driver) to allow the event marker be the first word of event. Zero suppression allows the event marker to be the only zero word into event. If pattern reader and/or counter are enabled and if at least one non-zero data (pattern or counter) are available into EBO at GATE, then the EBO write the header word and the non-zero data words. The header word is the only one to have the 16th bit set. The WDC (Word Data Counter) is a three bit field. Its content is the number of data words following the header word but if 8 data words to be written by EBO then WDC is 0.

VSN is the 8 bit Virtual Station Number of EBO, set by user by means of the VSN register. Each data word has a SA (Sub-Address) field to identify the pattern number or the counter. Both patterns and counter are 12 bit data format. If counter is disabled then all 96 bit (8 pattern words) are available, else the last word (SA = 7) is reserved for counter contents and the pattern bits decrease down to 84 (7 data words with SA = 0 .. 6).

## 4.4 Using EBOFERA in CAMAC readout.

EBO can also operate as CAMAC module.

When in CAMAC readout operating mode it is mandatory to set EBO as Slave (see MODE register). In the Tables Ib are reported registers to read EBO via CAMAC. In Table Ic are also shown CAMAC functions involved in CAMAC readout. EBO, after each GATE occurrence, set LAM CAMAC line if it has non-zero data.

The CAMAC readout may be performed in the following way.

After GATE :

> Test LAM, if q=1 results then
>> Load NZWORD to identify the non-zero word to be read;
>> Perform the CAMAC readout by access to PATT and/or
>>> COUNTER registers;
> Clear LAM.

## 4.5 EBOFERA front panel.

In Fig.7 is shown EBOFERA front panel. Two FERA control bus connectors are present to facilitate the cabling. When in Master operating mode both connectors must be used like shown in Fig.5. In this case the cable to ADC Driver must be CLR line missing because CLR is an output for EBO Master. Instead the cable to other Front End modules will be a full lines FERA control bus. Fig.8 shows the two cabling schemes. Cabling depends on data flow direction. In other words, on EBO Master position with respect to the ADC Driver module. The bit DIR in mode register must be initialized in accordance with the position of EBO. It has no significance for EBO Slaves. Two LEDs on front panel reflect the status of DIR bit. The LED ON must be the one towards Front End modules. LEDs "T", when in ON state, indicate the presence of bus termination resistors. The only module terminated must be the one at the end of the bus. The LEDs "MST" and "RUN", when in ON state, indicate the EBO in Master operating mode and the activity onto bus (readout in progress), respectively.
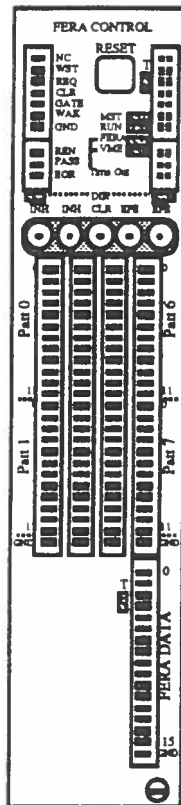
**Fig.7. EBOFERA**
front panel.

Two "Time Out" indication are present on front panel : FERA and VME. These LEDs are for error condition detection. The Time Out condition is respect to the start of an event readout and the EOR signal occurrence (the one to identify the end of readout of event). When Time Out occurs then VME LED is switched on if at this time WST are asserted, else FERA LED is switched on. These error indications are useful for electronics setup debugging to detect bad cabling (i.e. interruption of REN-PASS chain), bad timing among FERA GATE and individuals GATE to Front End modules or, furthermore, bad behaviour of Front End modules.

Error indications may also occur in case of temporary hanging of readout for non-pathological conditions (i.e. VME in temporary BUSY state due to slow tape operations).

In case of non-temporary error conditions, to restart the readout, can be necessary to act on front panel push button RESET or to perform a CAMAC Clear LAM (F10).

On EBO front panel are also available five NIM output : EFE and its complement /EFE, CLR and INH (the CAMAC INHIBIT) and its complement /INH.

As previously explained the complement of EFE (Enable Front End) is for GATE VETO purpose (see Fig.5).
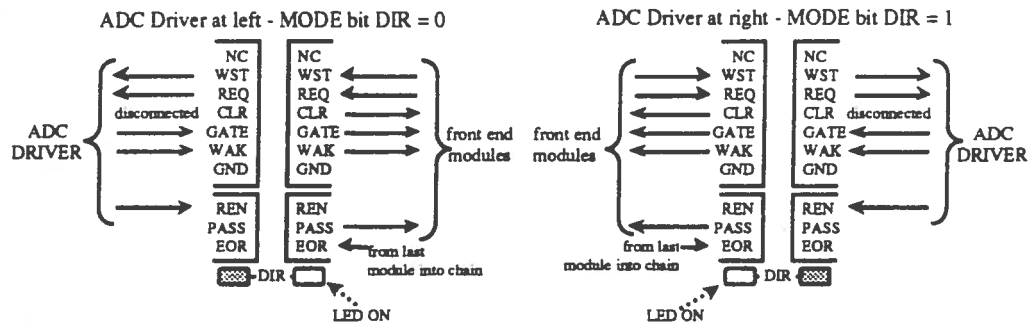
ADC Driver at left - MODE bit DIR = 0          ADC Driver at right - MODE bit DIR = 1



**Fig.8.** EBO Master cabling in two case direction flow

To perform correct FERA or CAMAC readout operations is mandatory to use the CAMAC Inhibit function. When the system is in stop state, i.e. to setup modules, all the CAMAC mainframes must be in Inhibit active state to inhibit all Front End converters to accept spurious gates. Then, at start, the Inhibit can be removed. In this case the INH and /INH can be used to control GATE and, for example, to VETO other external electronics like counter/scaler and so on.

### 4.6 EBOFERA test in a nuclear physics experiment

The EBOFERA in master and slave configuration has been successfully tested and then used in a seven days experiment performed using the ALPI facilities of the LNL (Laboratori Nazionali di Legnaro - Pd - ITALY). A beam of $^{32}$S of 320MeV incident energy, 4 pnA intensity was impinging on a self-supporting target of $^{64}$Ni, 500$\mu$g/cm$^2$ thick.

Twelve tritelescopes[7] gas-Si-CsI, were positionned around the grazing angle to detect light and projectile-like charged particles. Fifty six BaF$_2$ crystals, regular prisms of hexagonal base 20cm high and with an apotheme of 4cm, were used to detect gamma transitions in the energy range 5-40MeV.

Particle-gamma coincidences were detected at an average rate of 1 kHz. LeCroy QDC and Gan'elec QDC and ADC operated in individual gate mode were present in the Front End, made up by means of two high power CAMAC crates. The IRDEL was set to 32 $\mu$s. The overall dead time was less than 10%. At the beginning of the run the logic state analyzer was used to monitor the data transfer from the ADC driver to the HSM: no errors were detected of the kind shown in Fig. 2a.

## 5 - CONCLUSION

The needs of last generation heavy ion experiments require developments of very performing and versatile electronic modules in order to handle the high multiplicity and/or the high counting rate of the physical events involved.

The FERA generation ADC modules supplies a very fast data transfer tool. Nevertheless the standard FERA setup in case of a long ADC Front End developping on several CAMAC crates suffers of a too high data transfer error rate.

The source of these errors has been investigated and the solution to this problem has brought to the design and realization of the CAMAC module EBOFERA. The module has been successfully tested and is now routinely used in heavy ion nuclear physics experiments.

## Appendix

The FERA bus, by its own nature, may create spurious signals on the line "wired OR" of the REQ. If one analyzes this line from the electrical point of view and replaces the ECL drivers of each module with an output circuit equivalent to a standard ECL port and the flat cable, interconnecting the modules, with a trasmission line, the circuit shown in the figure will be obtained.
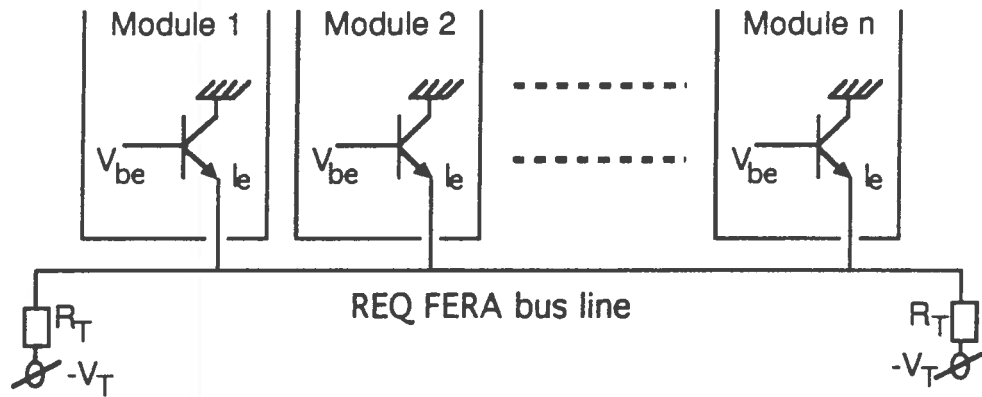


**Fig.9** Equivalent circuit for the REQ signal generation.

In a standard operation of the FERA the REQ line is normally kept "high" by more than one module. In this case it could happen that there is a slight difference between the drivers which cooperate to the activation (level H) of the REQ line. Taking into account that the relationship between emitter current Ie and base-emitter tension $V_{be}$ is:

$$I_e = I_{eo}e^{\frac{V_{be}}{V_t}}$$

(where Vt = 25 mV at 20°C) one sees that small variations of $V_{be}$ could imply large variations of $I_e$ (e.g. for a $\Delta V_{be}$ of 60mV there will be a $\Delta I_e$ of $10 I_e$). As a result, if there are differences between the different drivers, only one module will effectively supply current to keep the H state of the line. It could then happen that the delay due to the flatcable between the "active" module and the next module that has data to transmit (but wich is not supplying current to keep the H state) be higher than the decay time of the REQ signal. In this case a spike will arise on the line (see Fig.2a).

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