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A POSSIBLE FRONT-END READOUT SCHEME FOR THE RESISTIVE PLATE CHAMBER DETECTOR AT BABAR

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Abstract

A possible front-end readout for the Resistive Plate Chambers strips of the BaBar experiment, based on the constraint to read all the 40,000 sub-detector channels within 1.5 μs is described.
The flexible architecture we suggest, while well suited for a machine with a short inter-bunch structure, is readily adaptable to other RPC based detectors.

INTRODUCTION

BaBar detector [1] has been designed to study CP Violation asymmetries predicted by the Standard Model in B meson decays. It will be installed on PEP II $e^+ e^-$ storage ring machine [2] that will operate at the $\Upsilon(4S)$ resonance energy, providing an initial luminosity of 3×10^{33} cm^{-2} s^{-1}. Both the PEP II and BaBar commissioning are scheduled for the fall of 1998. The detector, as shown in Fig. 1, is composed of a Silicon Vertex Detector, a Drift Chamber, a Particle Identification System, a CsI Electromagnetic Calorimeter and a magnet with an Instrumented Flux Return (IFR)[3].

Muon are identified by range and hit topology in the IFR and by energy deposition in the central calorimeter detector. IFR also provides neutral hadrons (particularly K_L) detection. To achieve sensitivity down to momenta of 0.5 GeV/c, the IFR sub-detector (60 cm of steel in total) is divided into 21 iron layers of three thickness whose gaps are filled with Resistive Plate Chambers (RPC) [4] as the active elements. RPC layer signals will be read from two planes of strips (3 cm pitch) running in orthogonal directions, thus providing bi-dimensional information.

This note describes a possible readout scheme for the RPC strips of the IFR detector and is based on the constraint to read all the 40,000 strips within 1.5 μs from the Trigger. The

brute-force architecture developed (32 strips per card and 16 cards per chain) assures the most straightforward encoding of the hits and, should the timing constraints get looser, it will be readily adaptable to accommodate longer chains, while preserving the actual flexibility to read chains of arbitrary lengths. However as our front-end boards will be not easily accessible, in spite of the highest standards of quality gained by the semiconductor industry, a remote possibility of a chip failure does exist. Therefore at the time of writing we are also investigating on a different readout consisting of single card chains (16 strips per card, however) to ensure non redundant performances. We expect to have ready by the first quarter '95 a cost-vs-performance trade-off between the two systems.

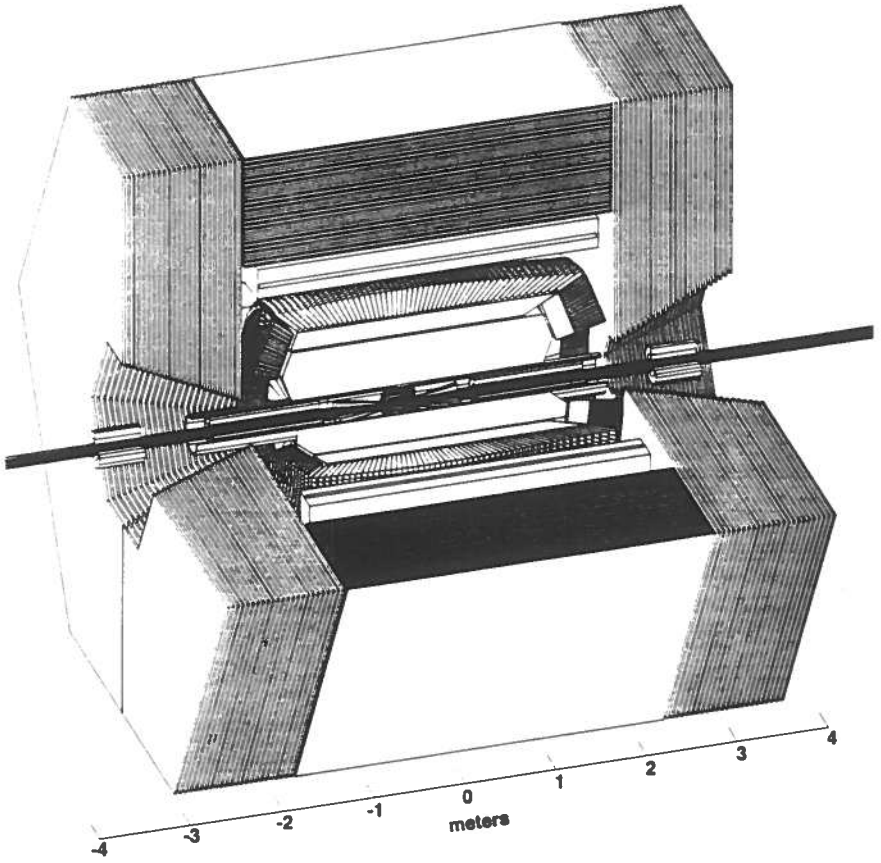

Fig. 1 – Three-dimensional view of the baseline detector.

1. – FRONT-END ELECTRONICS REQUIREMENTS

The functional requirement of the IFR electronics is to identify fired strips by associating them to an unique address.

The RPC high resistivity bakelite (10^{11} Ω×cm) single counting rate is of the order of 400 Hz/m^2 [5], fully compatible with the cosmic flux at see level. Considering this figure for the noise, times a safety factor of 10, and multiplying it for the maximum strip area (9×400 Hz/m^2), we obtain the single strip rate, which is about 480 Hz. If we accept strip data in a 1 μs

time window, the present time jitter, the counting rate per strip and per trigger is of the order of 5×10^{-4}. In the 40,000 channel system, assuming the safety factor of 10, the number of accidental hits is below 20 hits per trigger. Since the event physics rate is quite low, of the order of 30 Hz at $L=3\times10^{33}$ $cm^{-2}s^{-1}$, and we expect that each event releases at most few tens of hits, IFR is a very low occupancy detector. Due to IFR geometry and iron screening of RPCs, we believe that machine background has a negligible effect on IFR.

Level 1 Trigger (the so called Si Strobe Trigger) carries a fixed latency of 10 μs with a maximum jitter allowance of 0.5 μs. Minimum time between successive triggers is 1.5μs. This is the time allotted to empty front end electronics. The average trigger rate is less than 3 kHz while maximum expected rate is 0.2 MHz, mainly determined by machine background and cosmic rays.

The main constraint of this design is due to the relatively small time (1.5 μs) in which the ~40,000 channels have to be ready to accept and record new data. Obviously the main target is to reduce the electronics cost by minimising the number of modules and connections while assuring a completely safe operation of the system. This is achieved both reducing the overall complexity and by using well established technologies.

With reference to the block diagram in Fig. 2, the Front-End Card (FEC) will operate very close to the detector in the iron gaps while the FIFO Board (FIB) and the Zero Suppressor and Digital Encoding Board (ZEB), located outside the detector, will be accessible without opening the endcaps. The other modules will be in the counting room.

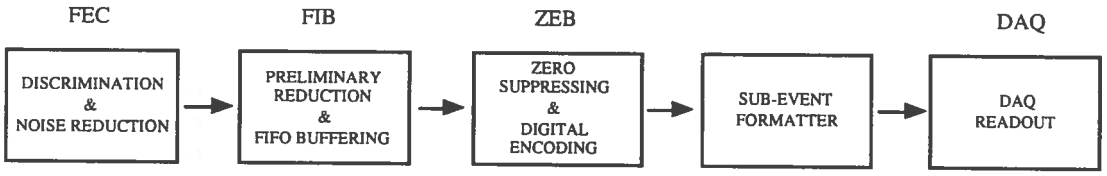

Fig. 2 – Each box corresponds to a specific function performed by the RPC readout architecture.

2. – GENERAL ARCHITECTURE

It is well known that RPC, with high resistivity bakelite (~10^{11} Ωxcm), is practically a noiseless detector with a rate fully dominated by cosmics. As in the BaBar detector the rate of particles reaching the IFR is relatively low, rejecting unwanted data, as soon as possible, is not as important as collecting data very fast.

Furthermore, as the probability of having two hits on the same strip during the latency time is essentially zero, we "store" strip signals during the time requested by the trigger decision (that is until the L1 trigger arrives) simply stretching them and reading within the mandatory 1.5 μs. Whenever large number of strips must be handled and acquisition time is not a critical parameter a serial readout scheme is used. However, as timing requirement for the BaBar detector to read front end cards is rather tight, we suggest a mixture between a serial and parallel readout.

The electronics for the IFR must perform the following functions (see also Fig. 2):

- record detected signals during L1 trigger latency;
- unload data from the front end cards within the allowed time (1.5 μs), rejecting data from front-end cards without fired strips;
- zero suppress and digital encode strip data into hit data (later stored in a sub-event hit buffer);
- read hit data, assemble them into a full data stream and eventually transfer them to a storage medium;

3. – FRONT–END CARD (FEC)

Front-end electronics cards will do first stage processing of induced pulses from the RPC's (Fig. 3).

Mandatory requirements for FEC boards:

- Be hooked onto the RPC's to avoid signal degradation;
- Contain the minimum number of components in order to maximize mean time between failures;
- High reliability, since the FEC electronics is inaccessible;
- Handle at least 32 strips/card in order to reduce the total number of cards;
- Provide its own card identifier number for debugging and diagnostic operation.

FEC's will be installed "inside" the IFR gap, between two successive iron planes just over the RPC layer, connected very close to the end of the strips. Each card will serve 32 adjacent strips.

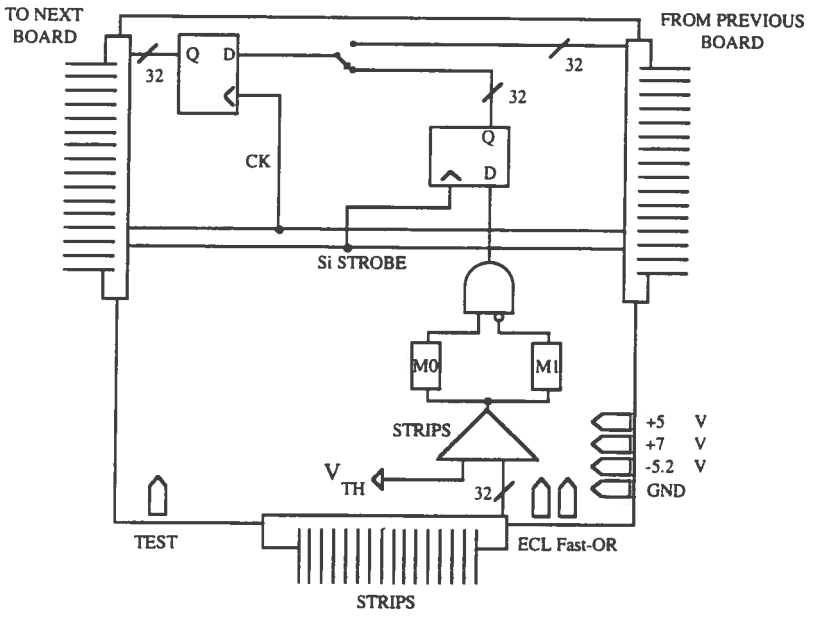

Fig. 3 – Schematic of the Front-End Card (FEC).

Front-end input stage can be quite simple. Since typical charges to be collected are of the order of 100 pc, there is no need for preamplifiers. Each strip acts as a transmission line with a discriminator on one end. The digital signal coming out from the discriminator has a width of more than 40 ns. Tests on the transmission line have shown that propagation time is about 5 ns/m with negligible attenuation from the induction point to the end of the strip.

The discriminator output is TTL compatible. A valid hit is obtained ANDing two one shots, 9 μs and 10 μs wide; stretching is necessary to achieve buffering during the trigger latency, while noise reduction is accomplished identifying strips fired within the 1μs time window (trigger jitter) and rejecting signals placed outside (Fig. 4).

A Fast-OR signal of the 32 strips is also provided. This signal can be splitted and used for time measurements, monitoring purposes, diagnostics and T0 calibration.

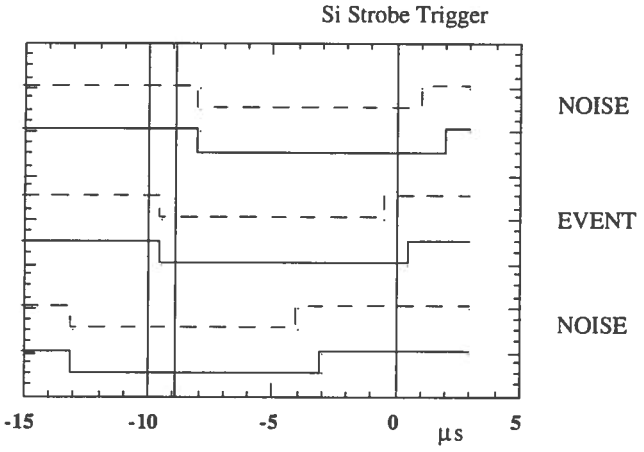

Fig. 4 – Only strips fired in the 1 μs window will be considered.

As shown in Fig. 5, 16 Front-End Cards (FEC) form a chain consisting of 16×32 = 512 strips and, depending on the choice of the VME crate (6U or 9U) 2 or 4 chains will be hooked together into a FIFO Board (FIB).

The line drivers card is necessary as the distance between chains and crates (although not yet fixed) is expected to be about 8÷10 meters.

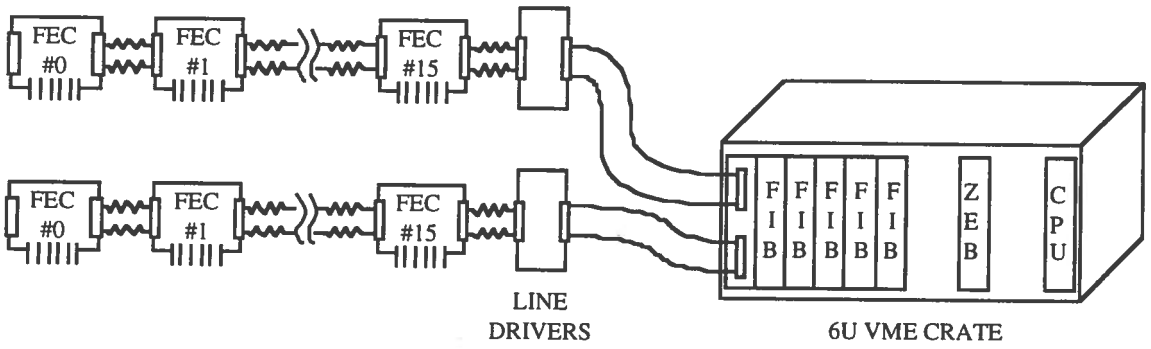

Fig. 5 – Front-End Card (FEC) chain.

In the occurrence of a Si Strobe Trigger, the status present on the strip 10 μs before will be latched onto a FEC register and then a sequence of 16 clock pulses will load into the FIFO the contents of the sixteen FEC registers.

In each VME crate there will be 4 to 6 FIFO modules collecting data from the chains on a frame by frame basis and storing data as 38 bit data word (32 bits of data, 4 bits of board address and 2 bits indicating start plus end of frame) as shown in Table I.

Table I — Data format as stored into the FIFO after the chain readout.

DATA # 15	Address board0	1	
DATA # 1	Address board	1	1
DATA # 0	Address board	1	1
Load #	X X X X X X	1	0

4. – FEC DESCRIPTION

FEC input stage is connected directly to the strips and operates continuously without regard to the trigger. The next stage performs three functions: (a) noise reduction; (b) storing of data; (c) shift of data.

4.1 – Input Stage

Strip signals 0 to 31 are first roughly adapted to their characteristic impedance through the resistor R_o (Fig. 6). Diodes D1 and D2 limits the incoming signal thus acting as a protection for the common emitter pnp RF transistor Q1 (BFQ 23 or equivalent). This transistor biased at about 1 mA by the base resistor R_b (680 KΩ), has the collector voltage sitting at about 20÷30 mV assuring a low level at the input of the buffer.

In the occurrence of a hit, the voltage at the Q1 collector due to the inductor L (1 mH) will raise very fast to an high level and then will decay rather slowly with a time constant of 20÷30 ns.

This input stage is the same we used for the L3 experiment [6,7] and is based on a design originally developed at ROME II University [8]. The main advantage of this design is the low cost and the very good timing performance. Threshold is fixed for all channels and could be changed only applying a negative voltage on the L inductor at the Q1 collector. The buffer outputs are fed both to a logic block performing the OR of the board and to the store and readout block.

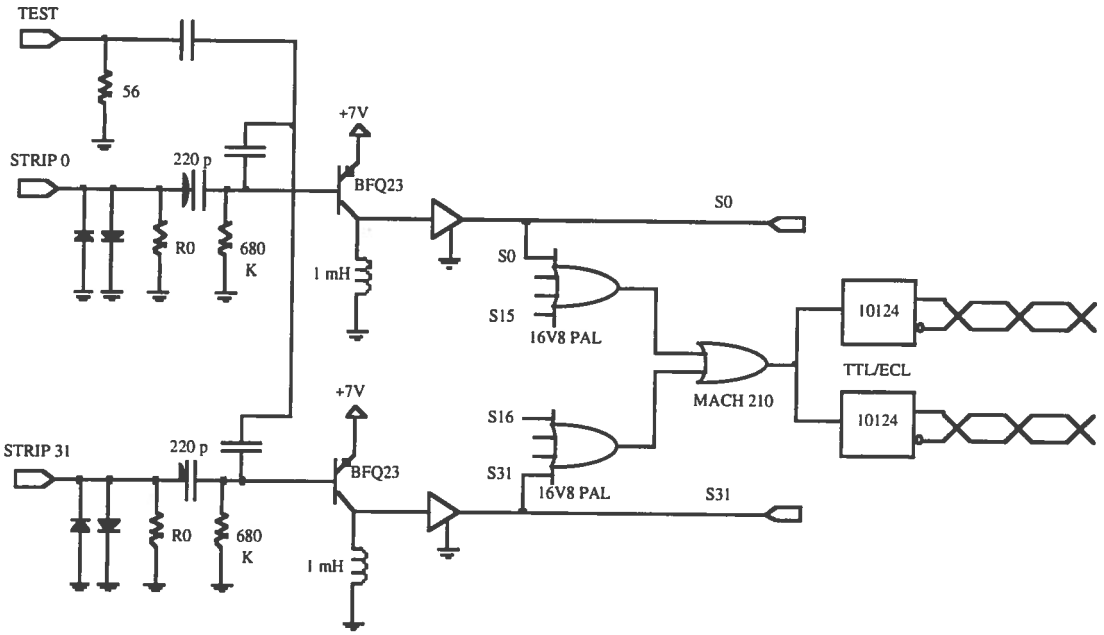

Fig. 6 – Input stage and Fast-OR generation scheme.

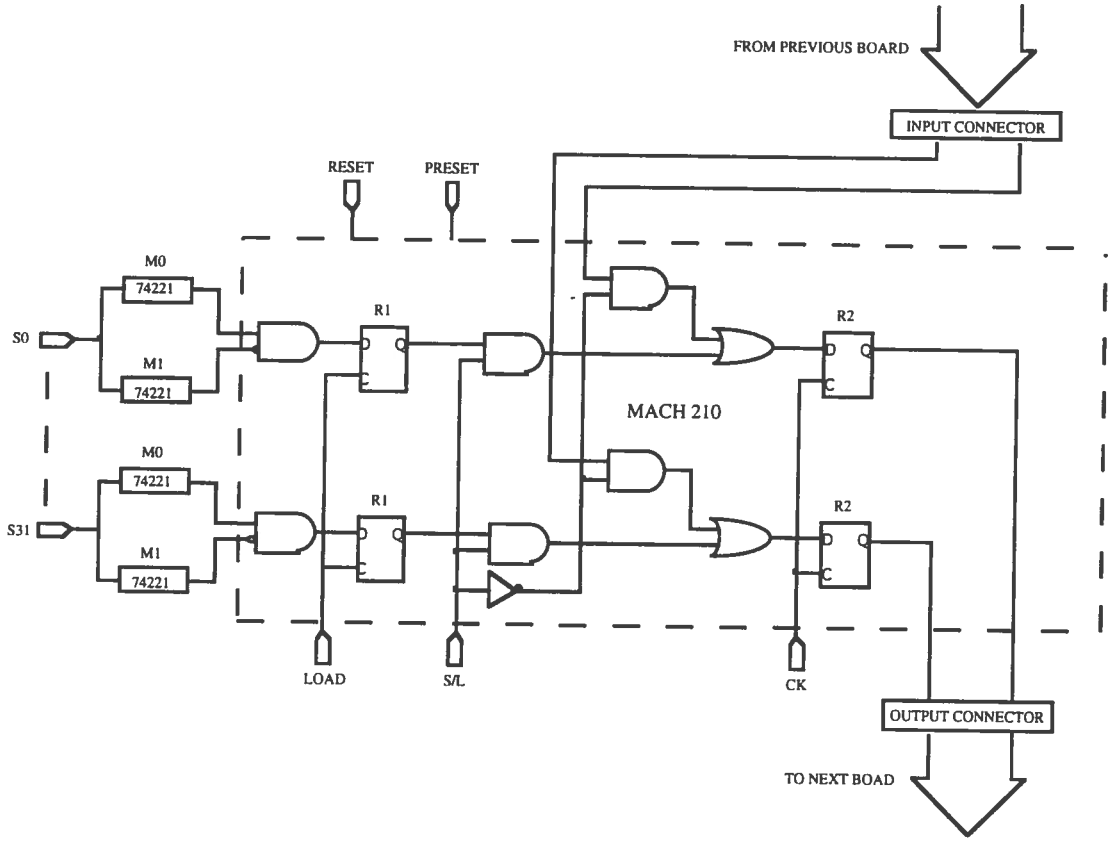

Fig. 7 – Readout mechanism of the Front-End Card.

4.2 – Logic Block

Based on Programmable Logic Device (CE16V8 HD PAL) this block produces an OR of the strips for the whole card. As each chip produces a 16-input OR function, two PALs are necessary. The two output are ORed in a MAC 210 whose output feeds the output driver (an MC 10124 TTL/ECL converter).

4.3 – Store and Readout Block

Buffer outputs also feed a double one-shot circuit (Fig. 7). Collecting strip data only during the trigger jitter (±0.5 μs window, 9.5 μs before L1 arrival time) reduces eventual noise coming from the RPC detector by a factor 10. On the front edge of the Si Strobe Trigger (L1 Trigger), the double one-shot output is latched into the R1 register, acting also as a memory buffer, and then it is transferred into the R2 register. Data stored is now available for reading by the FIB driving module. Switching the status of the S/L (Shift/Load) signal, 16 clocks will transfer data into the FIFO memory (Fig. 5).
Readout operation is performed such that data (32 bits plus board address) are serially passed from one FEC to the next so that the whole chain will form a serial chain 36 bit wide terminating into the FIFO buffer.

With this "shift register" like design it is possible to download the chain within the prescribed 1.5 μs and to free the chain for the next L1 Trigger.

Five MACH 210 PAL are necessary to implement this logic (Fig. 7)

4.4 Test Circuitry (Diagnostic)

A test pulse (Fig. 6) will control the functionality of the front end transistor simulating an hit on all the 31 channels, while two of the input coming the FIFO board will give a pre-set or a set pulse to all the MACH of the chain allowing a shift of all zeros or all ones for diagnostic purposes.

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