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A 250 Msps CAMAC DATA ACQUISITION SYSTEM

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Abstract - A 250 Msps CAMAC-compatible Data Acquisition System (DAS) is presented. The DAS represents a first approach to the measurement of the number of primary ionization acts for particle identification in gaseous detectors.

- Introduction

A drift chamber aimed also at a measurement of particle identification with the method of cluster counting is required to sample the signals produced on the sense wires at the highest rates. For Helium based gas mixtures, resolving times of the order of 2-3 nsec are adequate[1].

We have chosen the direct A-D conversion technique to digitize the drift chamber output signals. This technique adds a high use flexibility to a suitable sampling rate (500 Msps) of Flash ADC's (FADC) available on the market. Unfortunately, the state of the art of the integrated circuits does not allow a direct readout of the FADC digital output, limiting consequently the sampling rate.

- The DAS project

Generally, a large general purpose detector must allow for the readout of a number of data channels in excess of 10,000. The DAS project, then, impose the use of integrated circuits (IC) at low cost and low power dissipation. On the other side, it is necessary to perform the readout of the ADC digital output by means of fast IC. In order to meet these opposite requirements, the high speed six bits data stream has undergone at a double de-multiplexing. A block diagram of the DAS is shown in fig. 1.

The ADC board includes a 6-bit AD9016 FADC and demultiplexing circuits which provide two 6-bit data banks with several timing signals[2]. The fig. 2 shows the timing relation between the digital data and the timing signals for the ADC board.

In the ECL-TTL translation board, the data banks are de-multiplexed again and converted at TTL level. At the same time, four clocks are derived from the two strobe signals and then converted at TTL level. The fig. 3 shows the timing relation between the digital data and the strobe signals on this board.

The four buffer blocks, together with the CAMAC[3] interface, allow for the temporary recording and subsequent storing of the digital data in the host computer.

The memory buffer is a MCM6706 32Kx8 bit static RAM with a 10 nsec access time [4]. This IC adds a low power consumption to a fast access time and to a good density. In fact, for a 4 nsec time resolution, the maximum record length is about 0.5 msec (Tgate).
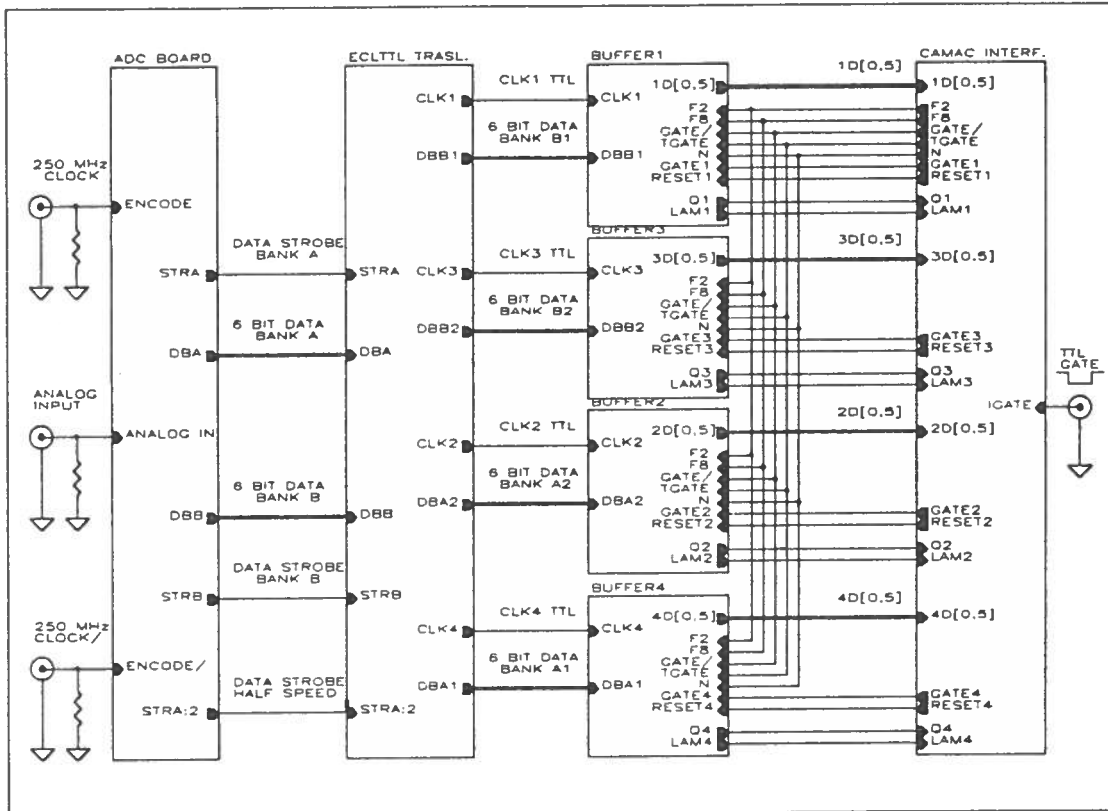

Fig. 1 - Block diagram of the DAS.
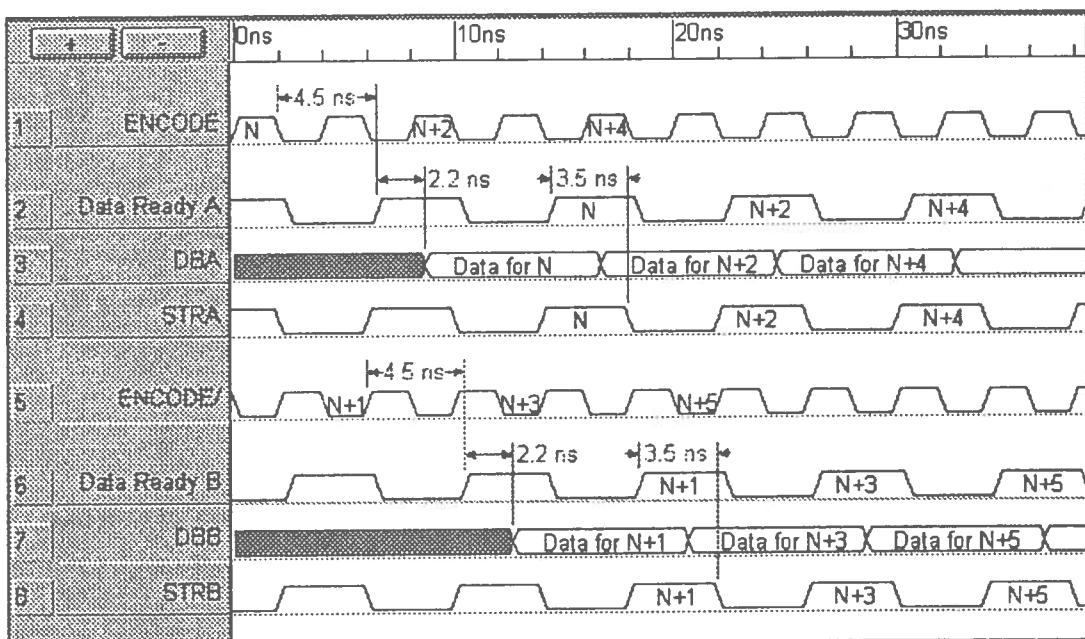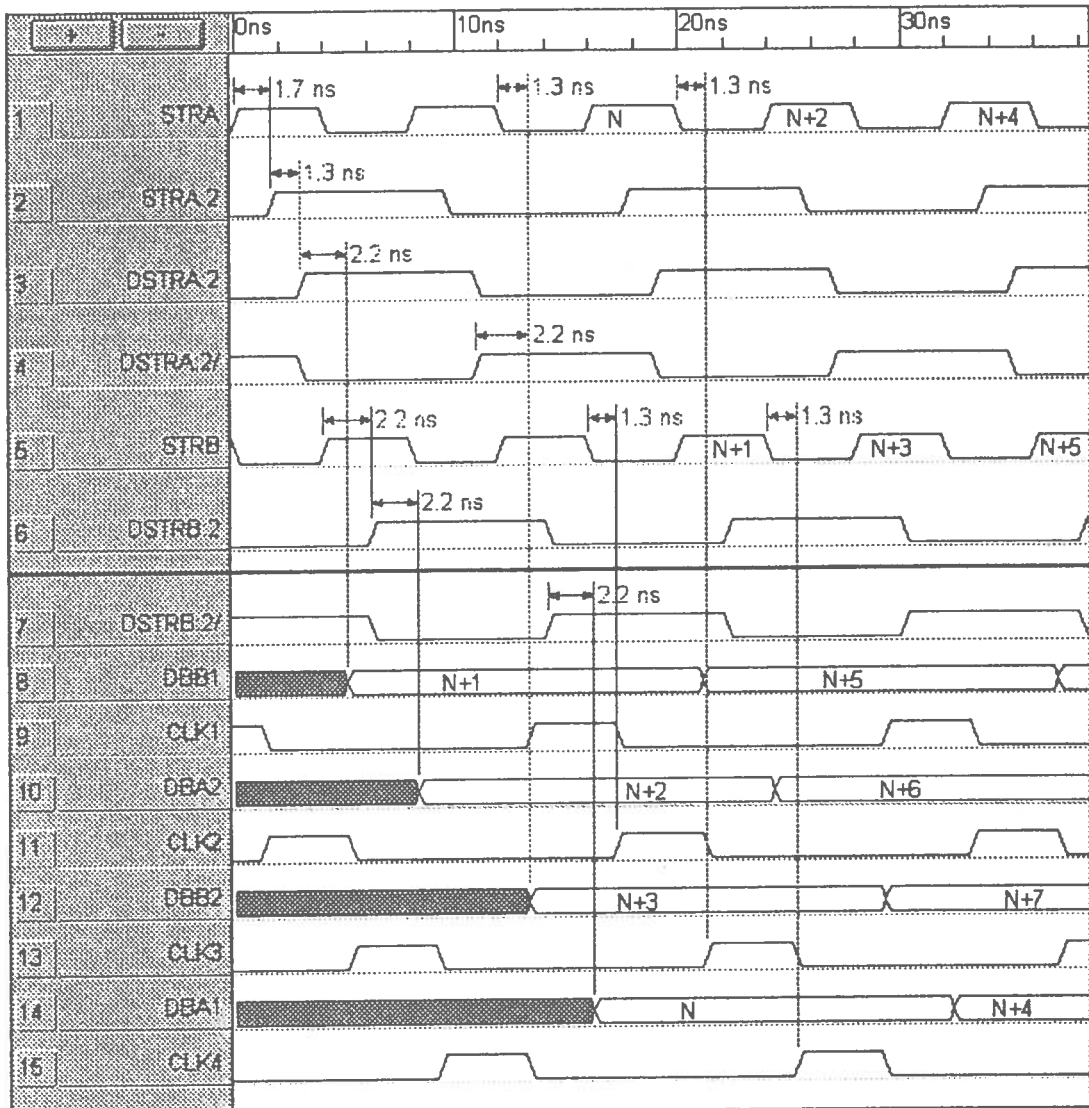

Fig. 2 - Timing relationship for the ADC board.

Fig. 3-Timing relationship in the ECL-TTL translation board.

- The DAS tests

In the next figures you can see some waveform DAS plots. The figures 5 and 7 are the output of DAC (AD9768) whose inputs are driven by digital data from AD9016 data banks A and B. DAC is updated at one half of ENCODE rate and is used for monitoring the input analog signal. The figures 4 and 6 are the CAMAC records related to figures 5 and 7 respectively.

This records are obtained by a dedicated software used for interfacing a MS DOS PC to a CAMAC crate for data postprocessing.

- Conclusions

The system is now operating at 250 Msps with encouraging results; successive development is a plan to use memory with access time below 10 nsec to update the system sampling rate at 500 Msps.
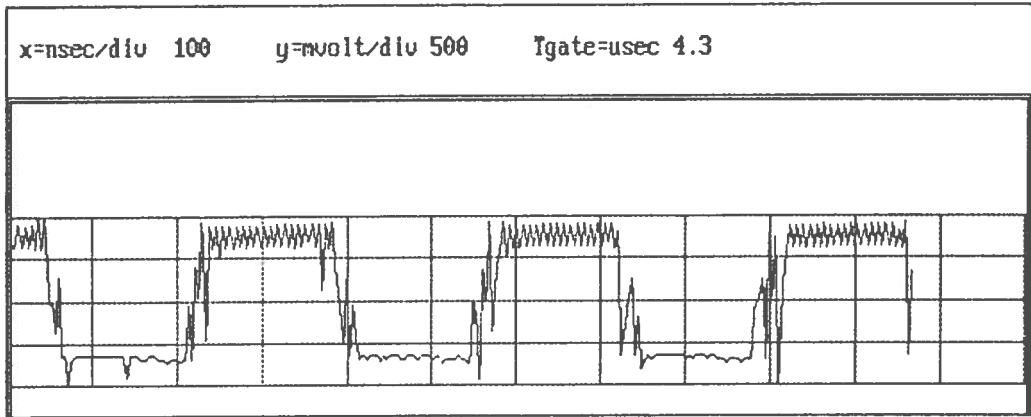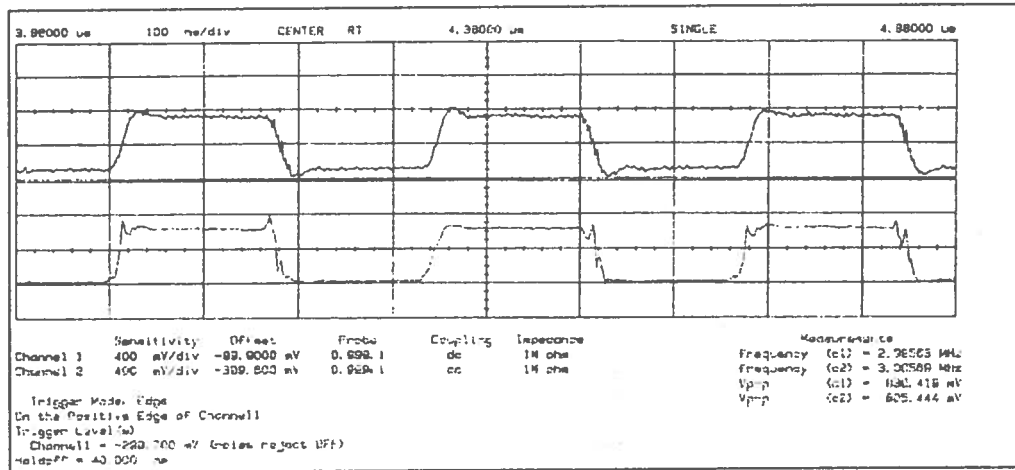
Fig 4

Fig. 5

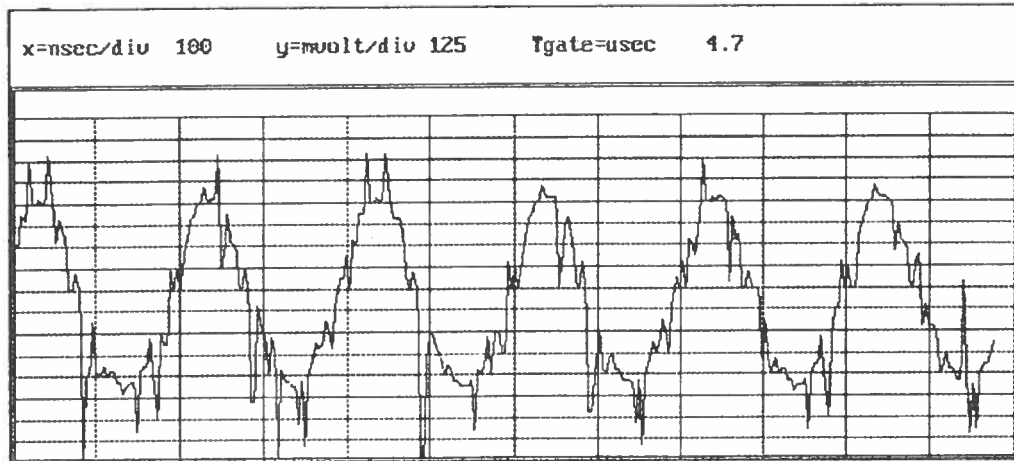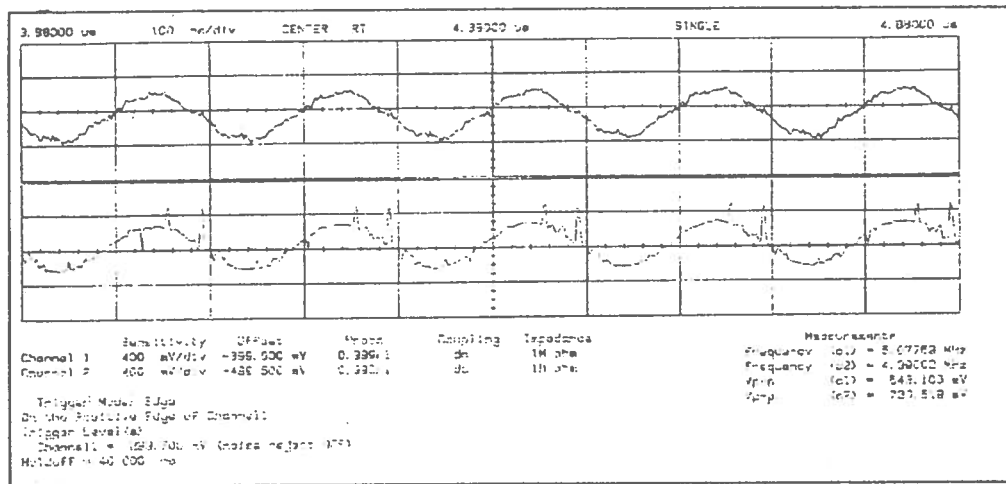x=nsec/div 100   y=mvolt/div 125   Tgate=usec   4.7

Fig. 6

Fig. 7

- **References**

1) G. Cataldi, F. Grancagnolo and S. Spagnolo, "Cluster Counting in Helium Based Gas Mixture", INFN/AE 95-xxx, submitted to Nuclear Instruments and Methods.

2) "Evaluation board for AD9016 High speed 6 bit flash ADC", ANALOG DEVICES Technical note, April 1989

3) "IEEE Standard Subroutines for CAMAC", ANSI/IEEE Std 758-1979

4) Motorola Memory Databook 1990