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Simulating capacitive cross-talk effects in DC-coupled hybrid silicon pixel detectors

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Abstract

An electrical model of a 5x5 pixel matrix has been developed. Cross-talk effects following the passage of an ionising event in the central pixel have been investigated with the help of the simulation program PSPICE; a small-signal equivalent circuit of a front-end charge sensitive preamplifier has been used for the analysis. The possibility to exploit the interpixel capacitive coupling to substantially reduce the number of readout channels, provided that a suitable analogue front-end electronics is used, has been discussed.

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1. Introduction

Since pixel detectors have been proposed [1, 2, 3], hybrid and monolithic detectors have been successfully tested in some pilot experiments in High Energy Physics [4, 5]. The first HEP applications of hybrid pixel detectors with binary readout are currently under implementation [6, 7]. Recently, a prototype of an analogue VLSI readout cell for hybrid pixel detectors has been successfully tested [8, 9]; interest for analogue readout of pixel detectors arises from the possibility of high precision particle localisation by exploiting interpolation techniques. Charge division mechanisms would profit from the high signal-to-noise ratio due both to the small capacitance of the collecting electrode (small area of the pixel and absence of wire bonding) at the preamplifier input and to the low leakage current. In a low multiplicity environment, the centroid finding method, applied on channels belonging to the same cluster, would give an extremely accurate definition of the track position in space.

In this paper, a study of cross-talk in silicon pixel detectors is presented. In Section 2 the electrical model of a 5x5 pixel matrix is described, together with a schematic, simplified small signal equivalent circuit of a charge sensitive preamplifier developed to be used in the PSPICE (version 5.0 © 1991 MicroSim Corp.) simulations. Section 3 presents the results of the simulations for various values of the most critical parameters, i.e. the interpixel capacitance and the circuit characteristics of the front-end p eamplifier. In Sections 4 and 5 the possibility of using capacitive charge division between neighbouring pixels is discussed. Of course, high granularity large area detectors (needed to allow precise charged particle tracking in HEP experiments) would benefit from the reduction of readout channels obtainable with this technique. Finally, conclusions and perspectives are drawn in Section 6.

2. The model

2.1 Generalities

The problem of cross-talk (illustrated schematically in Fig. 1) occurs in any segmented detector, like for instance silicon microstrips.

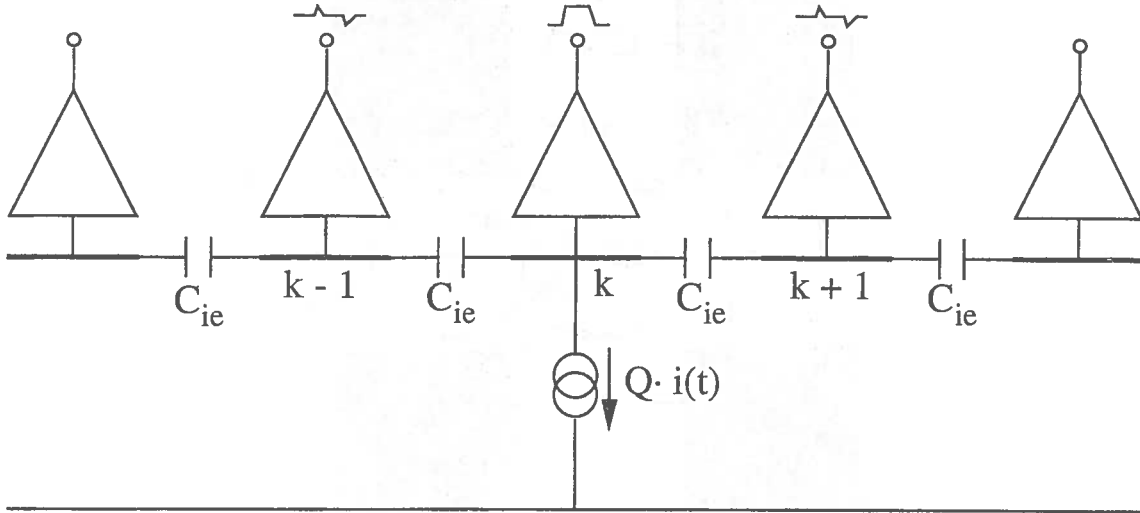


Fig. 1: Schematic illustration of cross-talk in a segmented detector. Spurious signals appear on the not-collecting electrodes $k-1$, $k+1$ after an ionising event interesting the electrode k . The preamplifiers are supposed to be current sensitive.

It is due to the fact that since the input impedance of the amplifier connected to the collecting electrode is finite, a signal appears across it [10]. The inter-electrode capacitances are then responsible for the injection of signals, proportional to the derivative of that appearing on the collecting electrode, into the contiguous preamplifiers. These signals have zero net area and their time separation is determined by the duration of the pulse at electrode k .

2.2 Pixel array model

To study these effects in pixel detectors, a 5×5 matrix has been considered (Fig. 2). Each pixel is connected to its neighbours via inter-pixel capacitances (C_{diag} , C_{ipx} , C_{ipy}) and resistances (R_{diag} , R_{ipx} , R_{ipy}). Capacitances between not-neighbouring electrodes have been neglected; this assumption is sufficiently precise as supported by Ref. [11, 12]. From the electrical point of view, each pixel is a reversely biased p^+-n junction, so that its equivalent circuit consists of a bulk resistance (R_{bulk}) in parallel with a junction capacitance (C_j). Assuming $300 \mu\text{m}$ thick square pixels having $100 \mu\text{m}$ side and a typical leakage current of about 0.1 pA/pixel (corresponding to about 1 nA/cm^2 , see Ref. [13]), a bulk resistance near to $250 \text{ G}\Omega$ is evaluated [14]. In a fully depleted reverse-biased diode, the junction capacitance is given, to a good approximation, by the well-known parallel plate capacitor formula [11].

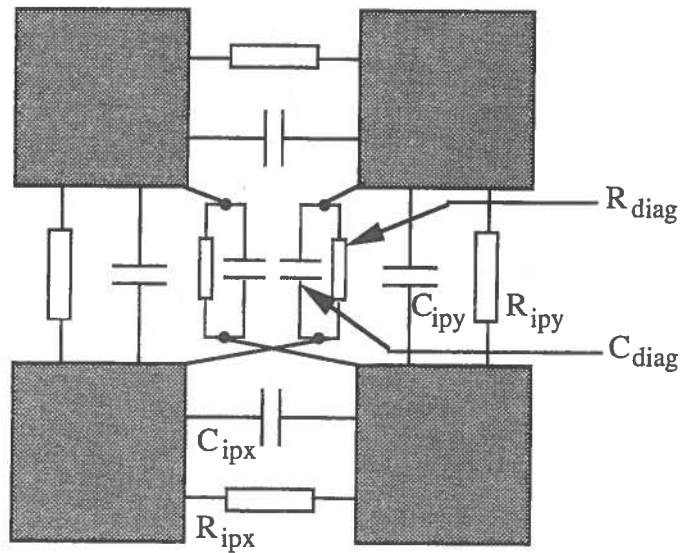


Fig. 2: Given the complexity of the full network, only a 2x2 subset of the 5x5 pixel array is shown in this figure. The interpixel resistances and capacitances described in the text are indicated.

We assumed in the simulations a n-bulk resistivity of 5 kΩcm, corresponding to a full depletion voltage of about 60 V.

2.3 Preamplifier model

Fig. 3 sketches the layout of a generic charge measuring system. The detector is modelled as a capacitive current source, delivering, in a very short time, a charge Q on the parallel of the total detector capacitance C_D and the preamplifier input capacitance C_i . C_f is the feedback capacitance and C_o the capacitance associated with the preamplifier output. g_m indicates the total transconductance of the preamplifier.

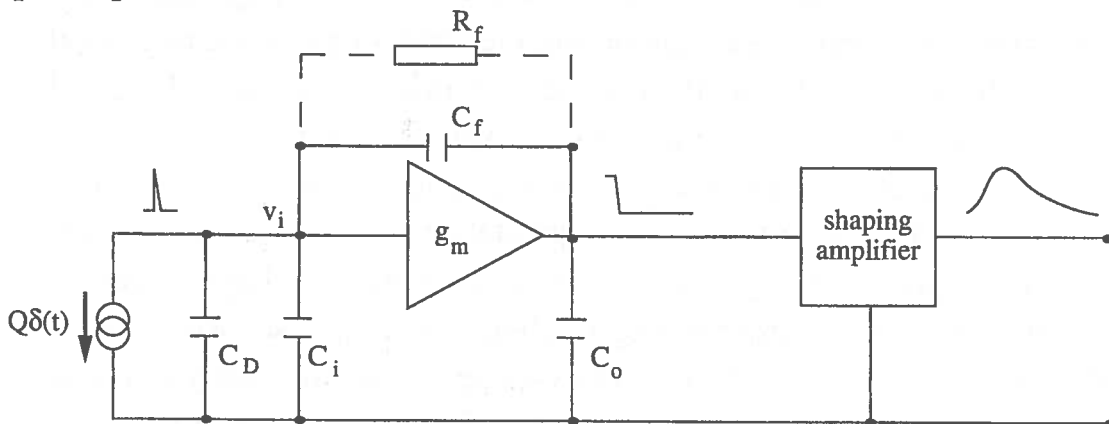


Fig. 3: General representation of an analogue front-end for charge measurement.

The closed-loop input impedance of the preamplifier, Z_i , is given by:

$$Z_i = C_l / (g_m C_f) \quad (i)$$

where

$$C_l = C_o + \beta(C_D + C_f) \quad (ii)$$

is the total closed-loop load capacitance seen by the preamplifier and

$$\beta = C_f / (C_D + C_i + C_f) \quad (iii)$$

is the feedback factor [10, 15]. Since the feedback resistor R_f is usually kept very large, in order to decrease its noise contribution, the integration time constant is determined by the preamplifier input impedance and by the total capacitance shunting the amplifier input:

$$\tau_{in} = Z_i(C_D + C_i + C_f) \quad (iv)$$

To be sufficiently general, we limited our analysis to the signals appearing at the preamplifier output, since the choice of the shaper characteristics is, of course, strongly dependent on the particular application and since we are not doing any noise analysis in this paper. In the simulation, each pixel is read out and the equivalent circuit is shown in Fig. 4. The charge preamplifier has been modelled according to Refs. [10, 16]. The transfer function $T(s)$ of the amplifying block of Fig. 3 has been considered to be characterised by a single pole (the so called "dominant pole"), so that

$$T(s) = g_m R / (1 + sRC_o) \quad (v)$$

where the parallel of R and C_o is the internal load across which the current $g_m v_i$ flows, thereby producing the voltage gain. In considering the equivalent schematic of the charge preamplifier of Fig. 4, basically two approximations have been used. First, R_f should in principle appear also in the input port of the preamplifier, but it has been omitted because of its large value (when compared to Z_i). Second, a capacitance given by $(g_m R + 1)C_f$ should be present in series with Z_i ; since the d.c. gain $g_m R$ is assumed to be very large, in practice we have that

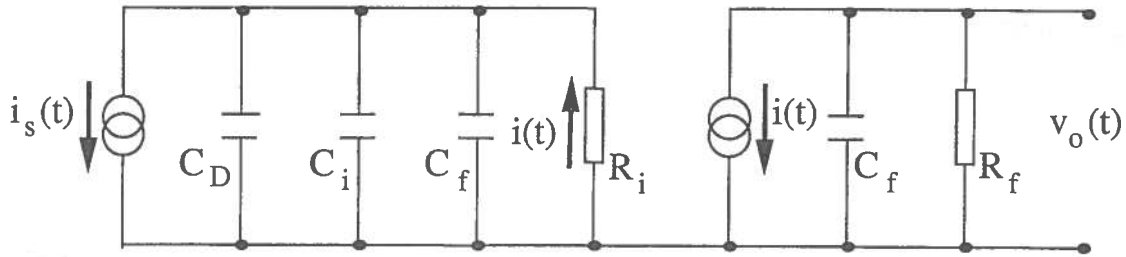


Fig. 4: Small signal simplified equivalent circuit of the charge sensitive preamplifier used in the simulations.

$(g_m R + 1)C_f \gg C_D + C_i$ and therefore also this capacitance has been omitted. The decay time constant of the output voltage is given by $\tau_s = R_f C_f$.

2.4 Charge signal model

A minimum ionising event is supposed to occur in the central pixel. From the signal point of view, this is equivalent to a current source (in parallel to C_j) delivering in a very short time a charge corresponding to about 24000 electrons (we are supposing a $300 \mu\text{m}$ thick detector). This current has been approximated as a rectangular pulse having a duration of 10 ns [10] and, therefore, an amplitude of $0.384 \mu\text{A}$ (Fig. 5).

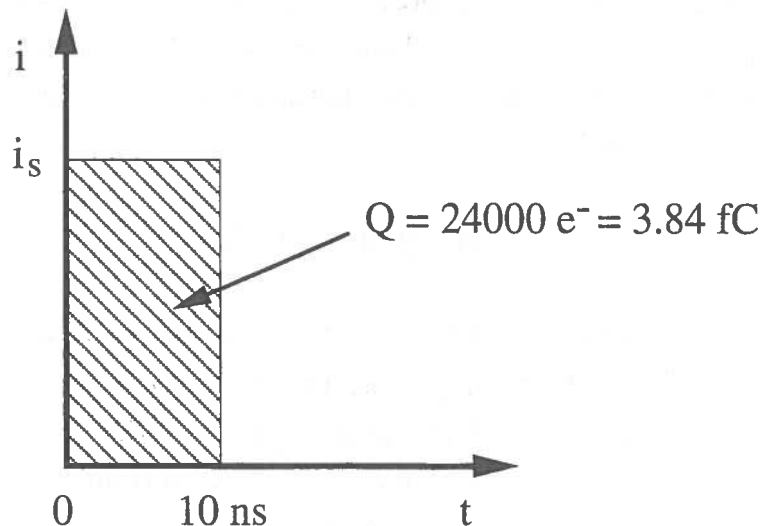


Fig. 5: Representation of the signal current generated in the detector by a minimum ionising particle. The current shape is simplified to a rectangle.

3. Simulation and results

3.1 Simulation scheme

In the simulations we varied the following parameters: the transconductance g_m , the feedback capacitance C_f and the geometrical characteristics of the square pixels (side and gap) determining the junction and interpixel capacitances. The different sets of parameters are summarised in Table 1. The first situation corresponds to a "standard" choice of the parameters [15] and it will be considered as reference. In particular, g_m has been chosen to be 0.2 mS in order to have an integration time constant less than 10 ns (see Subsection 2.4) with the typical capacitances involved (iv).

Using the pixel side and gap it is possible to evaluate the junction and interpixel capacitances according to Refs. [11, 12]. The interpixel resistances have been taken to be 100 G Ω while R_{bulk} has been taken to be 250 G Ω (see Subsection 2.2). The total detector capacitance C_D is given by (see again Subsection 2.2):

$$C_D = C_j + 4C_{\text{diag}} + 2C_{\text{ipx}} + 2C_{\text{ipy}} \quad (\text{vi})$$

where, given the square geometry, $C_{\text{ipx}} = C_{\text{ipy}}$. We have assumed $C_i = C_o = C_D$. The β and C_l parameters are then evaluated according to (iii) and (ii).

3.2 Results of the reference simulation

In the following, we labelled the upper left pixel as "11" and the bottom right as "55" (see Fig. 17 of Section 5), therefore the central pixel is "33". The suffix "0" indicates the output of the corresponding amplifier.

The results of the reference situation are shown in Figs. 6a-e. Fig. 6a shows the signal appearing at the output of the hit pixel amplifier (HPA). As it can be seen, the peak voltage is close to Q/C_f (370 mV instead of 384 mV); the integration time constant and the decay time constant are 2.3 ns and 100 ns respectively, as expected.

Fig. 6b shows the outputs of the first-neighbour pixel amplifiers (FNPA). $V(320)$ is clearly bigger than $V(220)$ given the different interpixel capacitances. In Fig. 6c the zero net area cross-talk signals appearing on the input impedances of these pixel amplifiers are shown.

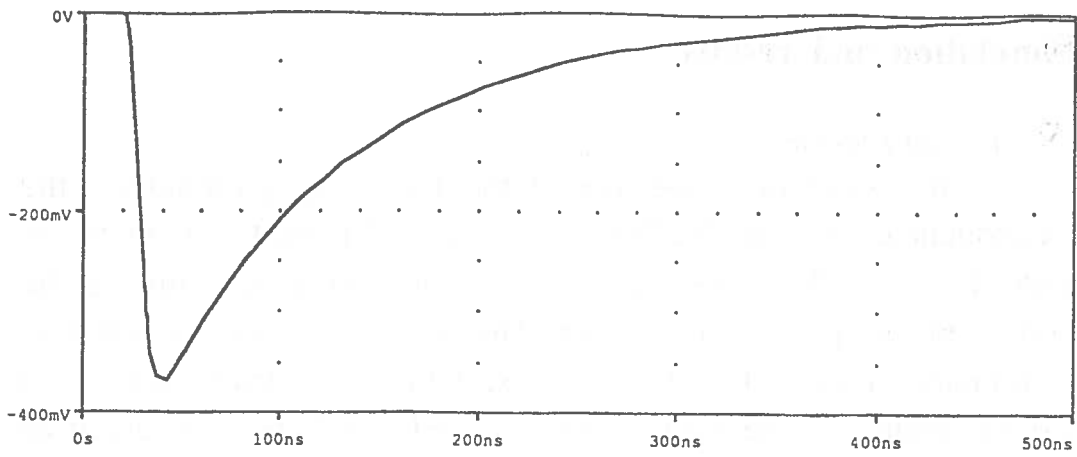


Fig. 6a: HPA output of the reference simulation.

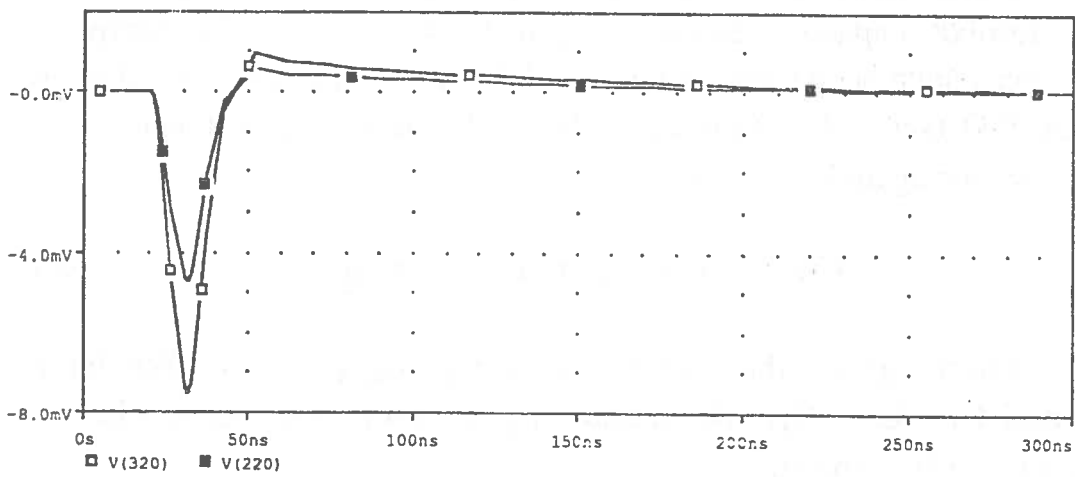


Fig. 6b: FNPA outputs of the reference simulation.

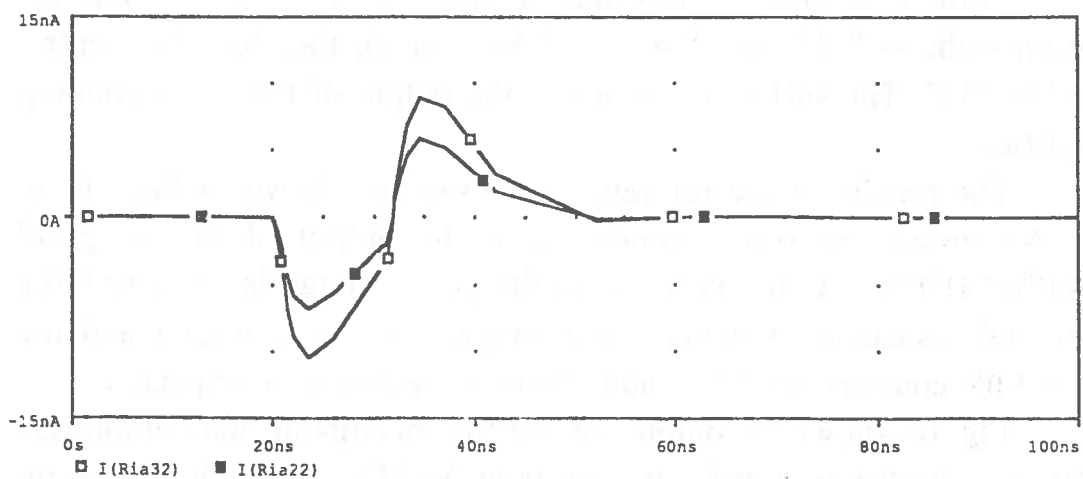


Fig. 6c: Induced current signals on the input impedances of the FNPA (reference simulation).

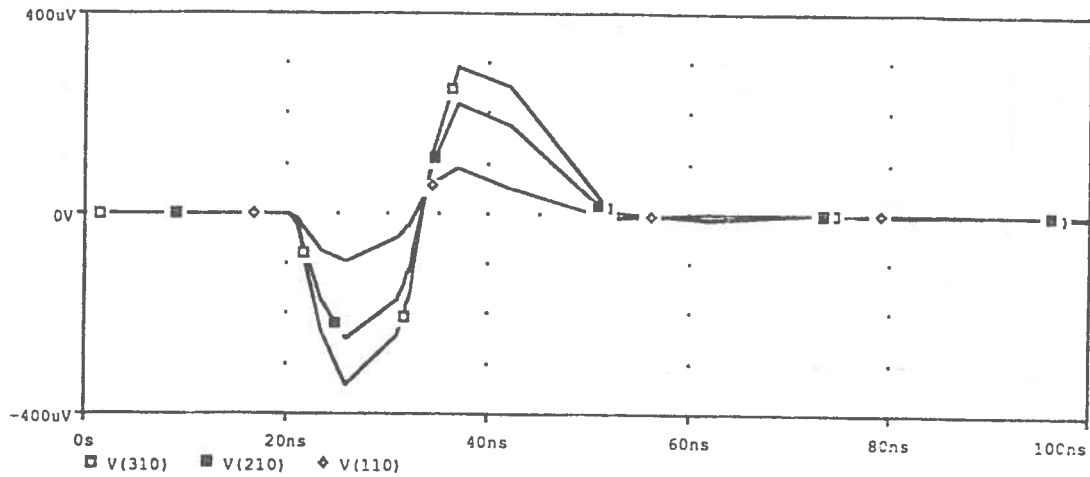


Fig. 6d: SNPA outputs of the reference simulation.

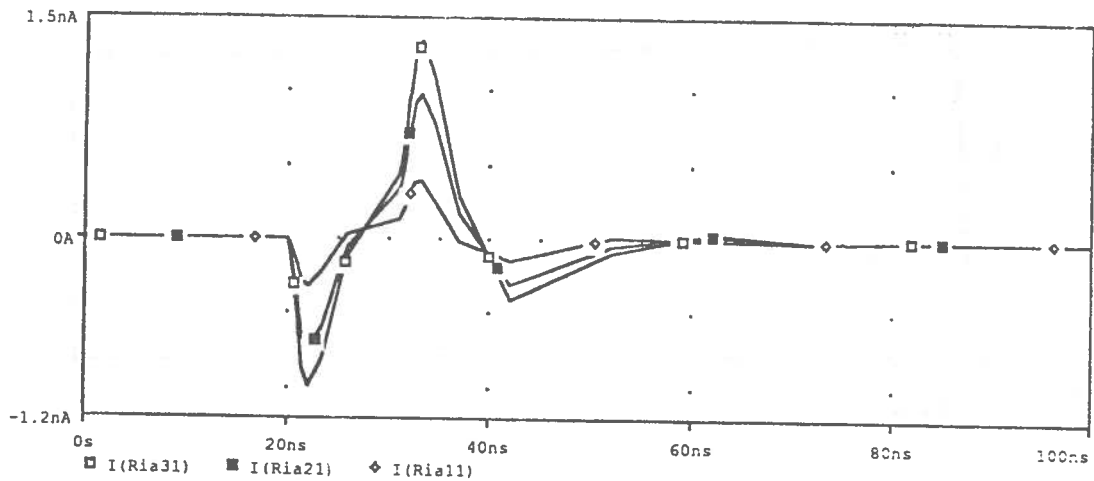


Fig. 6e: Induced current signals on the input impedances of the SNPA (reference simulation).

Figs. 6d and 6e show the same quantities (as Figs. 6b and 6c) but for the second-neighbour pixel amplifiers (SNPA). The peak values are 10 times smaller than those of the FNPA outputs.

3.3 Effects of transconductance variation

In a first simulation, g_m has been increased to 0.8 mS, thus reducing Z_i of a factor of 4 (see Table 1). The HPA output is similar to Fig. 6a but its rise time is smaller and its peak magnitude reaches the full value (Fig. 7a). Figs. 7b and 7c show FNPA and SNPA outputs respectively. As expected the induced signals decrease considerably because of the smaller input impedance.

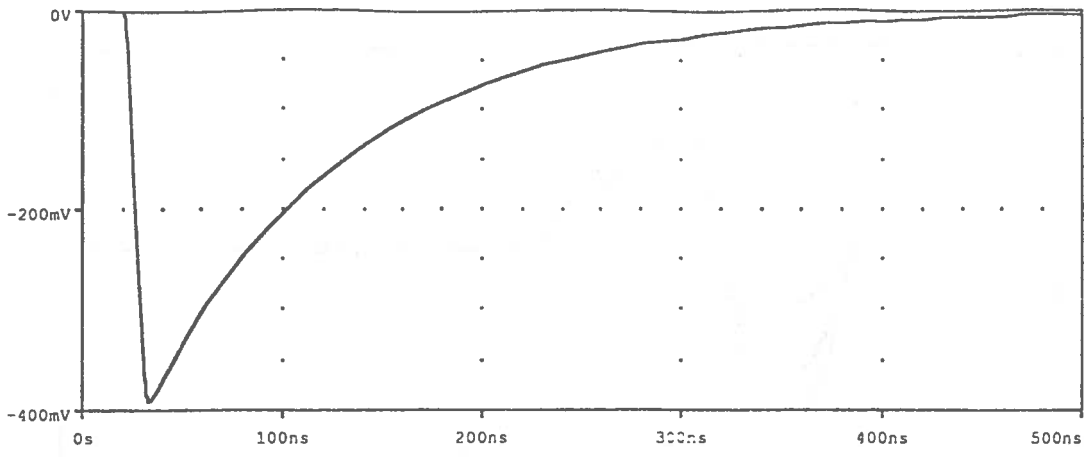


Fig. 7a: HPA output with $g_m = 0.8 \text{ mS}$.

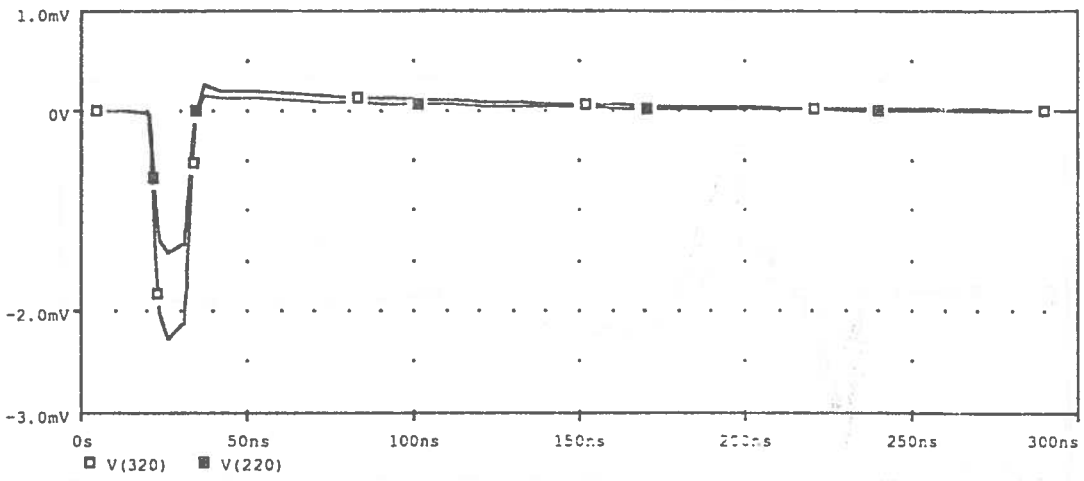


Fig. 7b: FNPA outputs with $g_m = 0.8 \text{ mS}$.

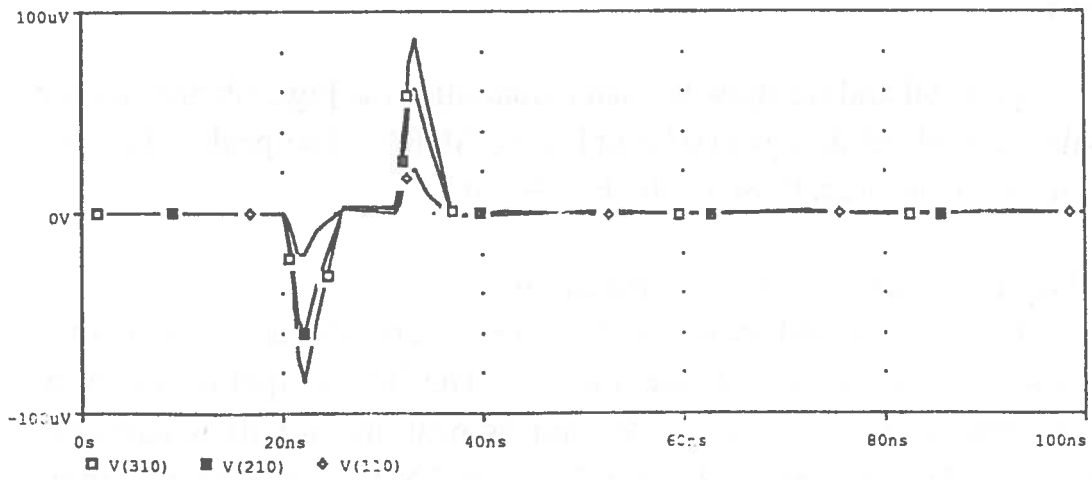


Fig. 7c: SNPA outputs with $g_m = 0.8 \text{ mS}$.

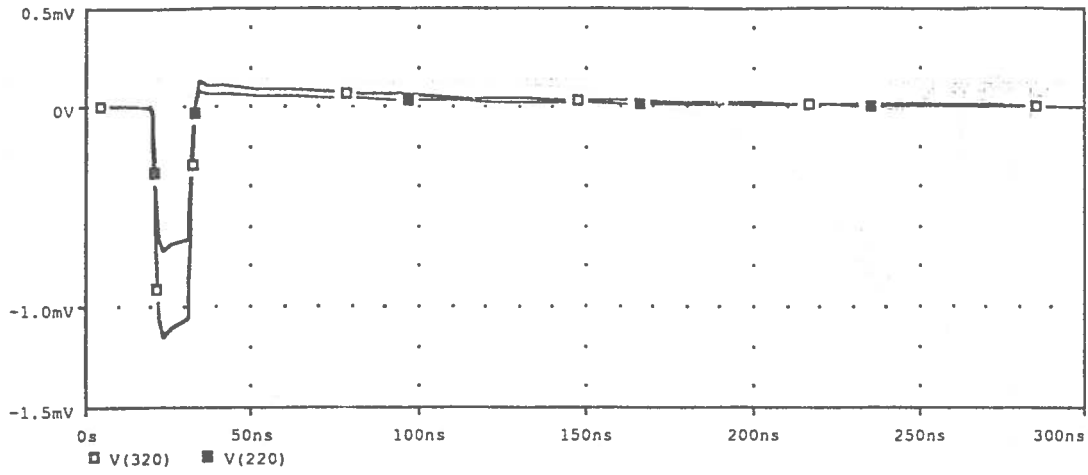


Fig. 8a: FNPA outputs with $g_m = 1.6$ mS.

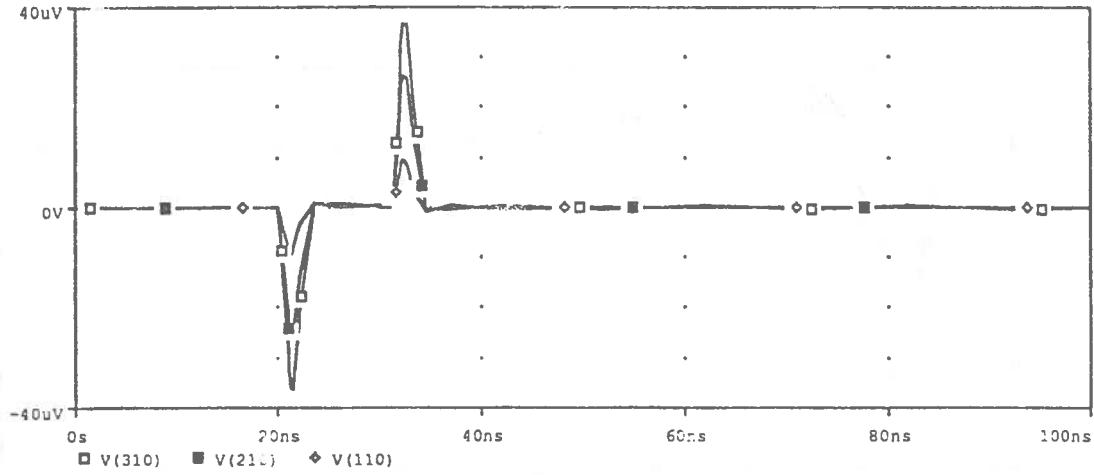


Fig. 8b: SNPA outputs with $g_m = 1.6$ mS.

Simul.	Side	Gap	Cj	Cip	Cdiag	CD	B	Cl	gm	Zi	Rf	Cf
§ 3.2	90	10	2.8	8.0	2.0	42.8	0.105	48.3	0.2	24 k	10 M	10
§ 3.3	90	10	2.8	8.0	2.0	42.8	0.105	48.3	0.8	6 k	10 M	10
§ 3.3	90	10	2.8	8.0	2.0	42.8	0.105	48.3	1.6	3 k	10 M	10
§ 3.4	90	10	2.8	8.0	2.0	42.8	0.055	45.4	0.2	45 k	10 M	5
§ 3.4	90	10	2.8	8.0	2.0	42.8	0.189	54.7	0.2	14 k	10 M	20
§ 3.5	35	5	0.4	3.8	5.5	37.6	0.117	43.2	0.2	22 k	10 M	10
§ 3.5	70	10	1.7	6.2	5.2	47.3	0.096	52.8	0.2	26 k	10 M	10
§ 3.5	150	20	7.9	11.3	3.0	65.1	0.070	70.4	0.2	35 k	10 M	10
§ 3.5	300	30	31.5	20.6	2.0	121.9	0.039	127.1	0.2	64 k	10 M	10

Table 1: Sets of parameters used for the simulations of Section 3. Side and gap are quoted in μm , capacitances in fF, g_m in mS and impedances in Ω .

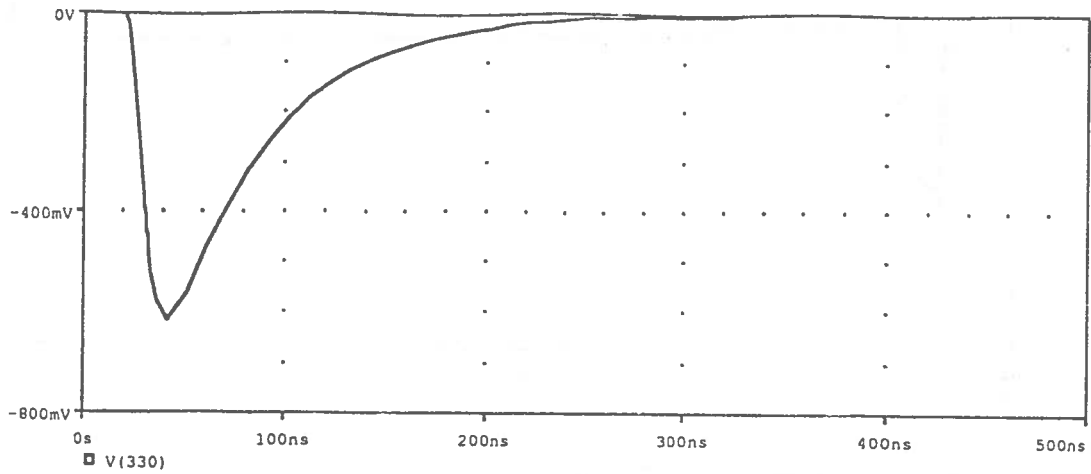


Fig. 9a: HPA output with $g_m = 0.2 \text{ mS}$ and $C_f = 5 \text{ fF}$.

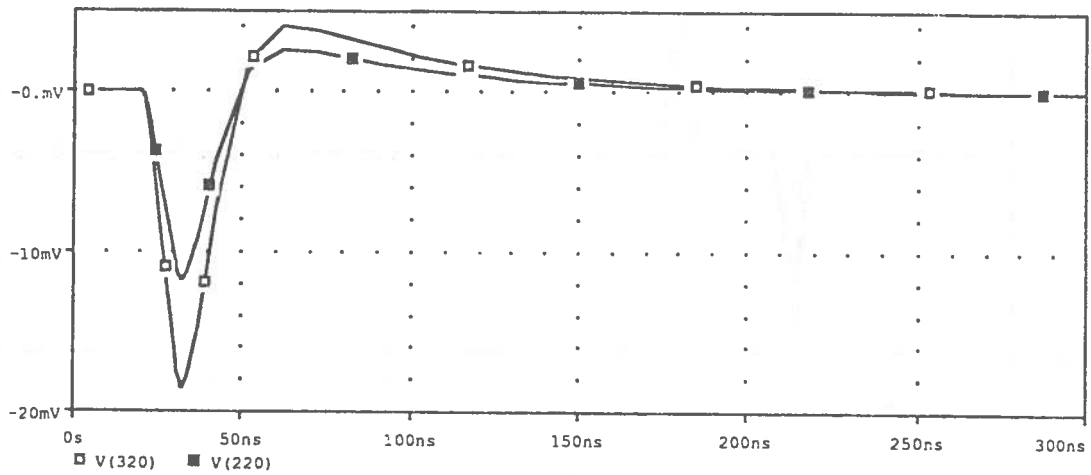


Fig. 9b: FNPA outputs with $g_m = 0.2 \text{ mS}$ and $C_f = 5 \text{ fF}$.

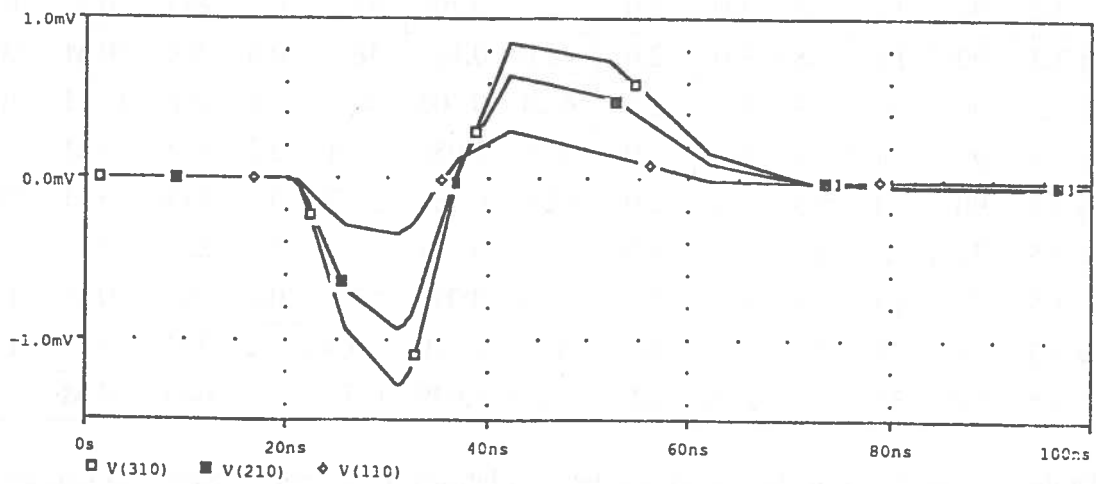


Fig. 9c: SNPA outputs with $g_m = 0.2 \text{ mS}$ and $C_f = 5 \text{ fF}$.

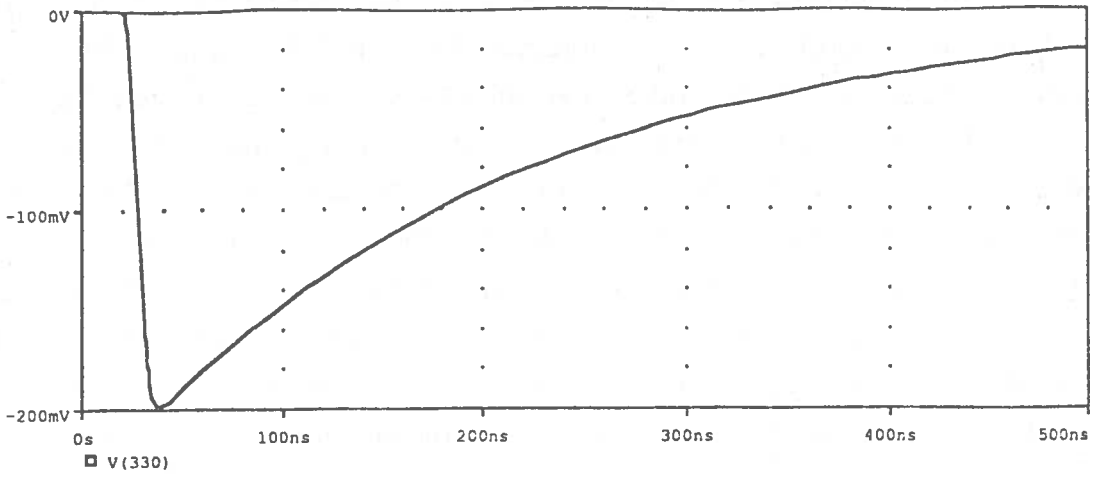


Fig. 10a: HPA output with $g_m = 0.2 \text{ mS}$ and $C_f = 20 \text{ fF}$.

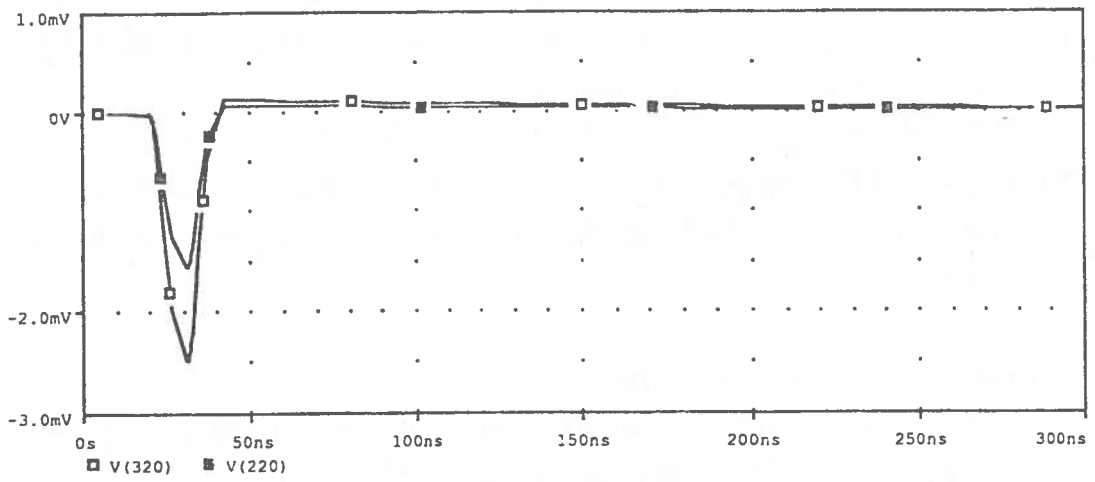


Fig. 10b: FNPA outputs with $g_m = 0.2 \text{ mS}$ and $C_f = 20 \text{ fF}$.

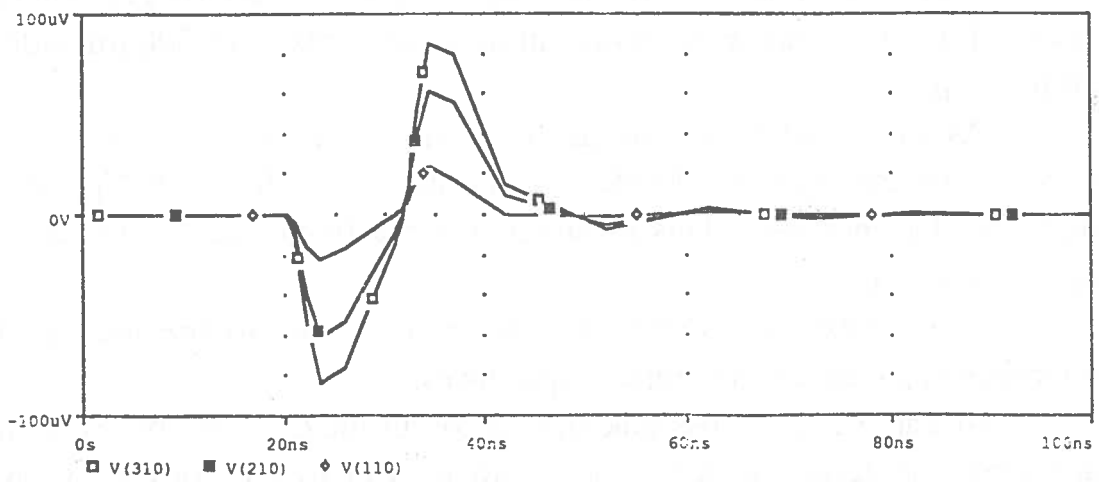


Fig. 10c: SNPA outputs with $g_m = 0.2 \text{ mS}$ and $C_f = 20 \text{ fF}$.

In a second simulation, g_m has been taken to 1.6 mS. No substantial difference can be appreciated on the HPA output. Again, a clear reduction of FNPA and SNPA outputs is seen (Figs. 8a and 8b).

It can be concluded that the cross-talk signals approximately scale linearly with Z_i . Moreover, the slight increase of the HPA output when increasing g_m is due to the fact that the integration time becomes more and more smaller than the RC time constant to the neighbours. It is clear that g_m cannot be increased too much because the overall integration time will, at a certain point, become smaller than the signal duration determined by the charge collection mechanism in the detector.

3.4 Effects of C_f variation

We started halving C_f to 5 fF. Figs. 9a-c show the HPA, FNPA and SNPA outputs respectively. As it can be seen, the decay time constant is halved while the peak amplitudes are roughly doubled when compared with the reference situation.

We then doubled C_f to 20 fF. Figs. 10a-c show again the HPA, FNPA and SNPA outputs respectively. It is apparent that while the decay time constant is doubled, the peak amplitudes are roughly halved, as expected.

3.5 Effects of geometry variation

We first considered square pixels of 35 μm side, 5 μm gap. HPA, FNPA and SNPA outputs are shown in Figs. 11a-c.

Figs. 12a-c show the results about pixels having 70 μm side, 10 μm gap.

Figs. 13a-c refer to pixels having 150 μm side, 20 μm gap while, finally, Figs. 14a-c show the results in the case of pixels of 300 μm side, 30 μm gap.

As far as HPA outputs are concerned, we note a progressive decrease of the peak amplitude; this is due to the fact that C_D , and therefore C_I , increases. This means that, for a fixed g_m , τ_{in} increases (see formulas (i) and (iv)).

The FNPA and SNPA outputs increase due to the increased interpixel capacitances and input impedances.

In Table 2, the cross-talk signals for all the cases of this Section are shown in terms of percentage with respect to the corresponding HPA output.

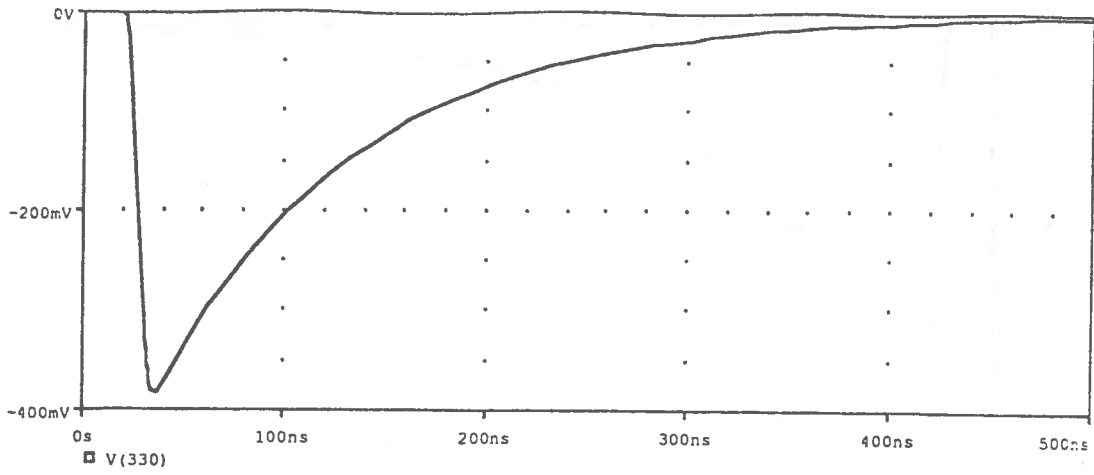


Fig. 11a: HPA output for pixels having 35 μm side, 5 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

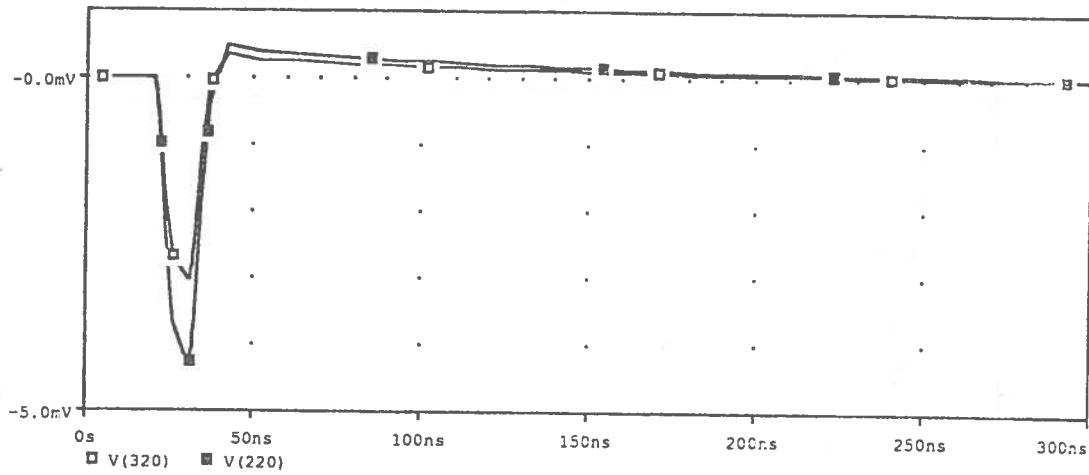


Fig. 11b: FNPA outputs for pixels having 35 μm side, 5 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

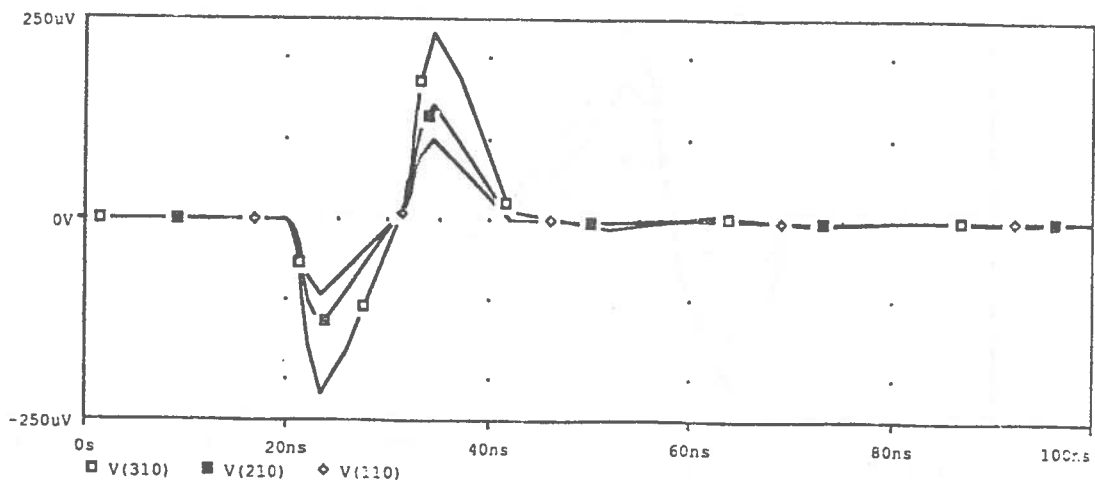


Fig. 11c: SNPA outputs for pixels having 35 μm side, 5 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

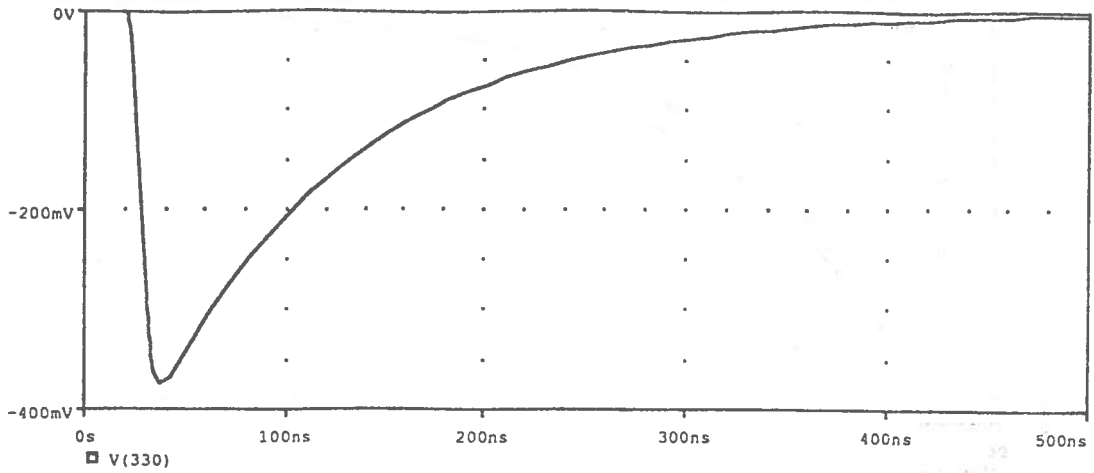


Fig. 12a: HPA output for pixels having 70 μm side, 10 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

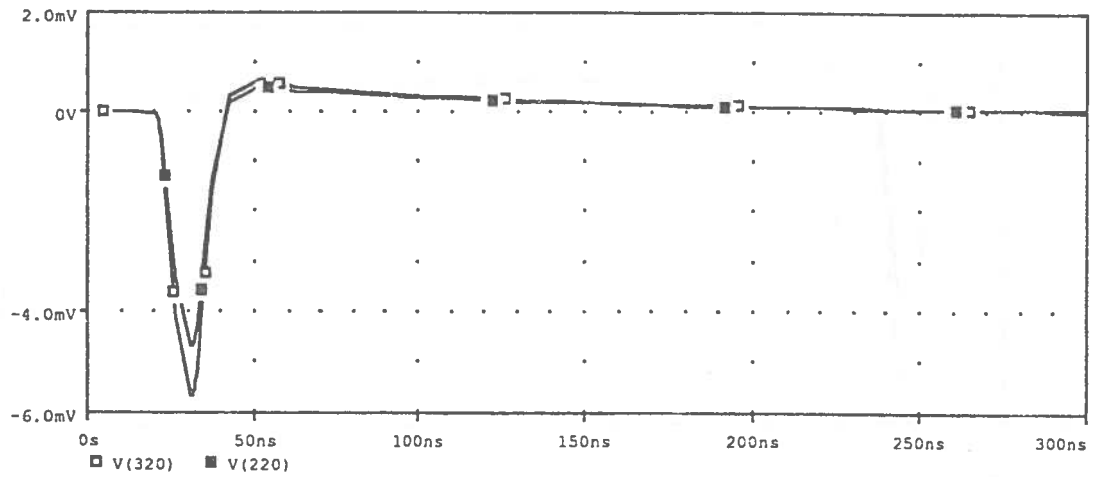


Fig. 12b: FNPA outputs for pixels having 70 μm side, 10 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

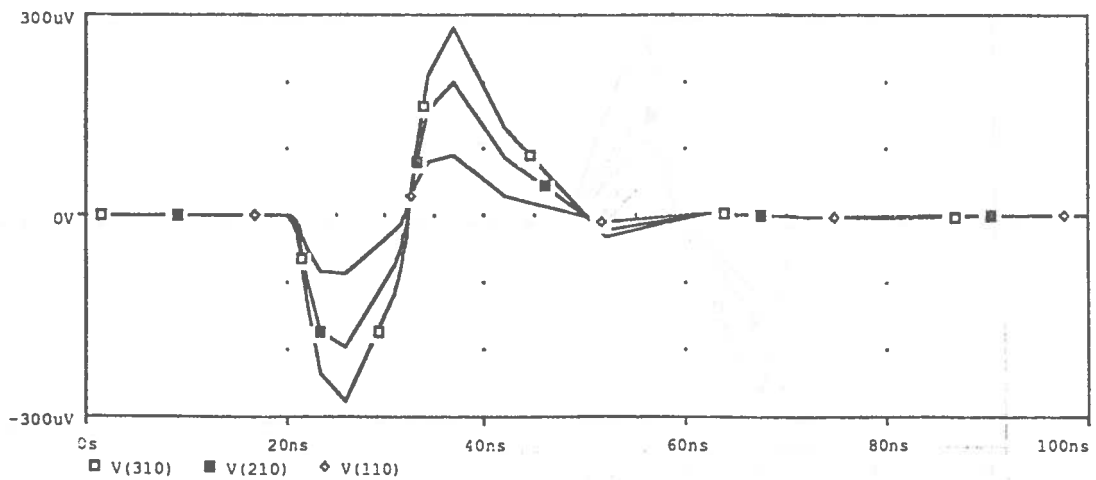


Fig. 12c: SNPA outputs for pixels having 70 μm side, 10 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

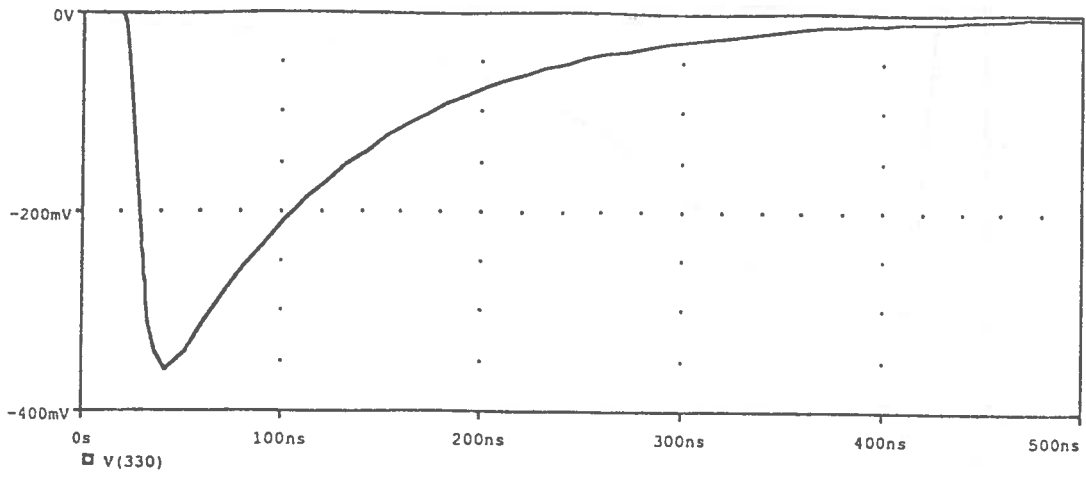


Fig. 13a: HPA output for pixels having 150 μm side, 20 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

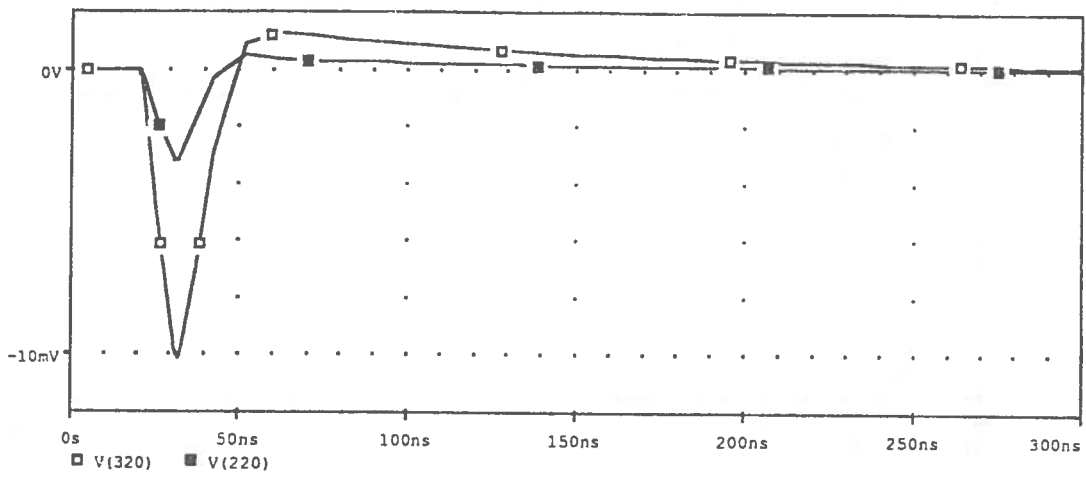


Fig. 13b: FNPA outputs for pixels having 150 μm side, 20 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

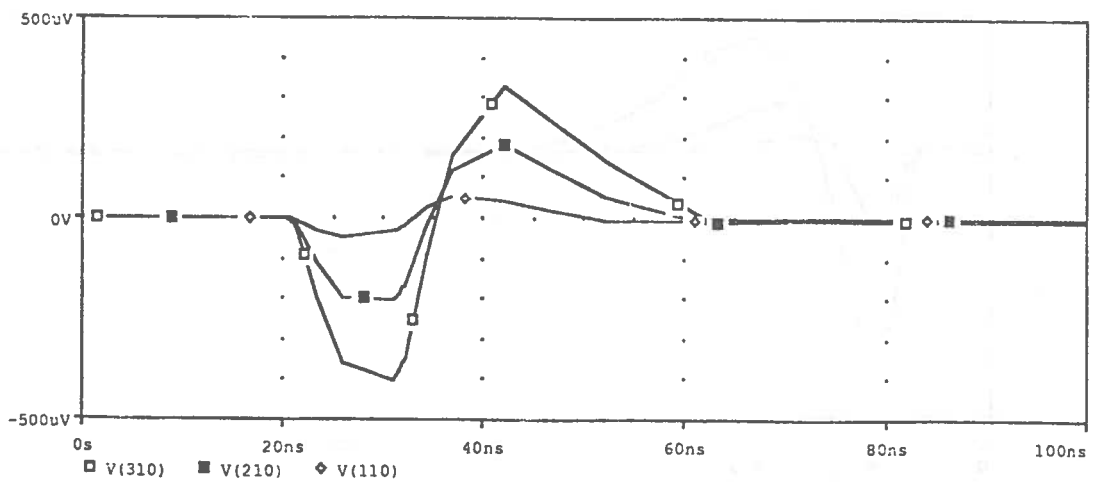


Fig. 13c: SNPA outputs for pixels having 150 μm side, 20 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

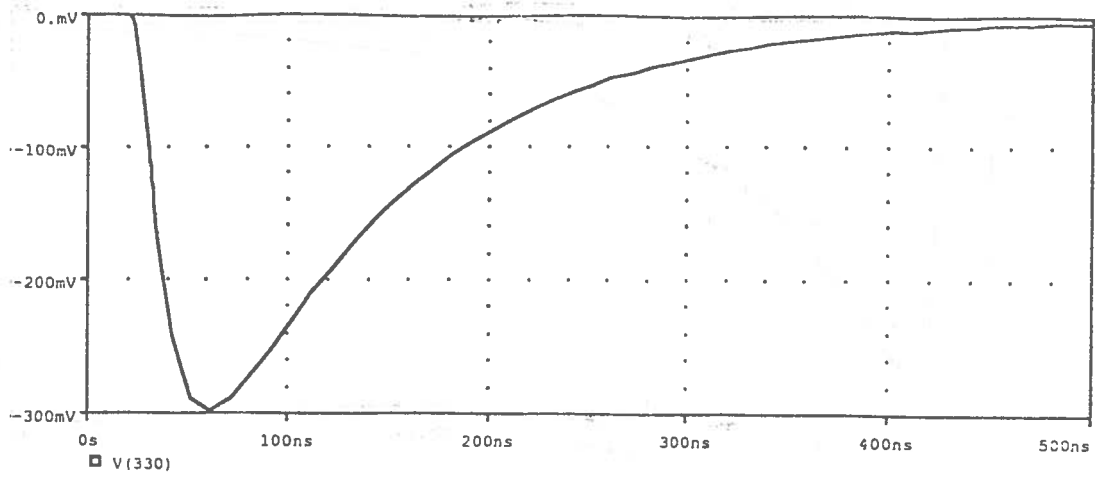


Fig. 14a: HPA output for pixels having 300 μm side, 30 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

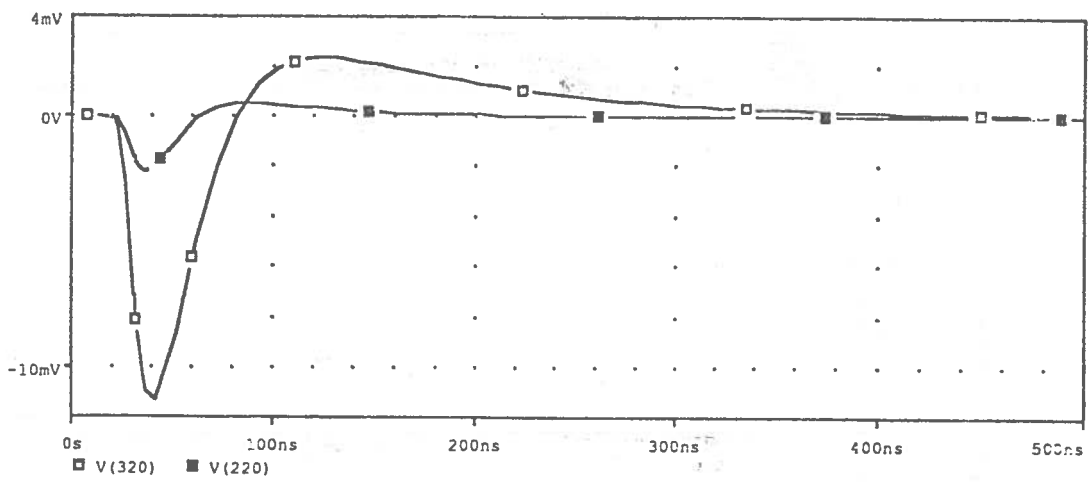


Fig. 14b: FNPA outputs for pixels having 300 μm side, 30 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

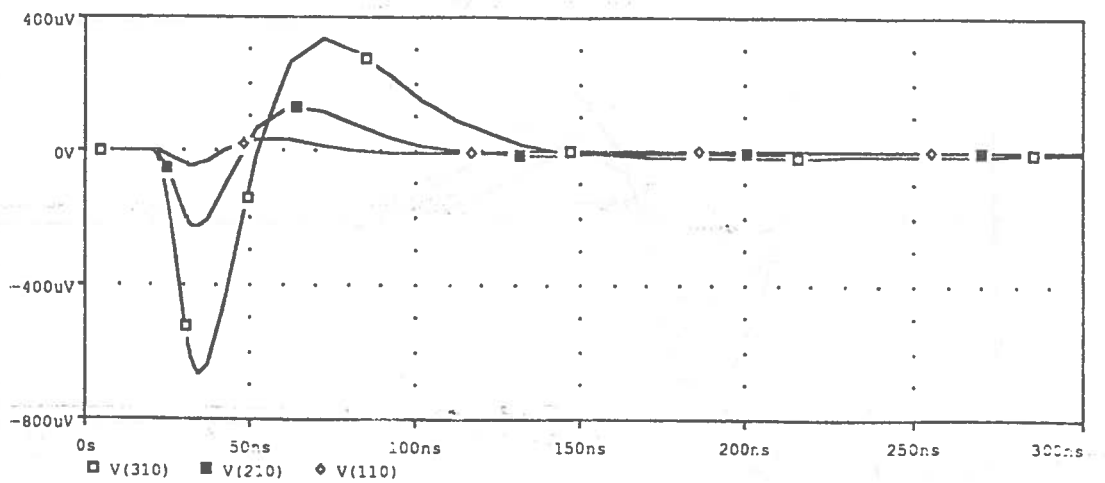


Fig. 14c: SNPA outputs for pixels having 300 μm side, 30 μm gap ($g_m = 0.2 \text{ mS}$ and $C_f = 10 \text{ fF}$).

Simul.	V(320)	V(220)	V(310)	V(210)	V(110)
§ 3.2	2.02%	1.27%	0.094%	0.068%	0.025%
§ 3.3	0.58%	0.37%	0.022%	0.016%	0.005%
§ 3.3	0.29%	0.18%	0.009%	0.006%	0.002%
§ 3.4	2.99%	1.88%	0.210%	0.150%	0.056%
§ 3.4	1.25%	0.77%	0.042%	0.030%	0.012%
§ 3.5	1.12%	0.79%	0.057%	0.032%	0.025%
§ 3.5	1.51%	1.24%	0.074%	0.052%	0.023%
§ 3.5	2.81%	0.88%	0.111%	0.060%	0.011%
§ 3.5	3.76%	0.71%	0.225%	0.076%	0.015%

Table 2: Summary of the FNPA outputs (V_{320} and V_{220}) and SNPA outputs (V_{310} , V_{210} and V_{110}) for the simulations of Section 3. The induced signal peak is expressed as percentage of the corresponding HPA output peak.

4. Possibility of capacitive charge division in pixel detectors

In the previous Sections, capacitive cross talk effects among neighbouring pixels have been considered as spurious signals appearing at the preamplifier inputs of pixels not directly involved by charge collection mechanisms. On the other hand, these effects may be usefully exploited with analogue readout. In fact, to accomplish HEP experiments requirements, high granularity, large area detectors are needed to allow precise charged particle tracking. This implies a very large number of readout channels; for instance, in the future LHC experiment CMS, about 80 millions analogue pixel channels are foreseen [17]. A well known method to reduce this number, paying the price of worsening the double track resolution, is given by analogue capacitive charge division [18]. This technique has been extensively used, for instance, with silicon microstrip detectors. For capacitive charge division to be effective, however, several conditions have to be met [19]:

1. for uniform charge collection, the intermediate electrodes have to be kept at a potential close to that of the readout electrodes;

2. to avoid resistive cross-talk, the impedance between readout elements has to be significantly larger than the dynamic input impedance of the front-end electronics;
3. to avoid signal losses, the inter-electrode capacitance has to be big when compared to the junction capacitance of the single electrode.

This method allows a substantial reduction of the whole detector cost and power consumption. The need of a smaller cooling system can also be an advantage for microvertex detectors where often very little room is available.

Moreover, in pixel detectors, the integration of complex readout electronics in each VLSI cell (with the available technology), together with the interconnection technique limits (bump bonding), make the possibility of decreasing the pixel side to a few tens of μm quite problematic. By exploiting capacitive coupling, it is possible to "decouple" the VLSI cell dimension from the pixel size, thus reading out small diodes with relatively large cells (Fig. 15). This would also avoid to push the technology limit too far.

To accomplish points 1 and 2, it would be necessary to bias the intermediate diodes via properly designed bias resistors; this could be done either integrating these resistors on the detector substrate (e.g. with a polysilicon step in the process) and linking them to the nearest

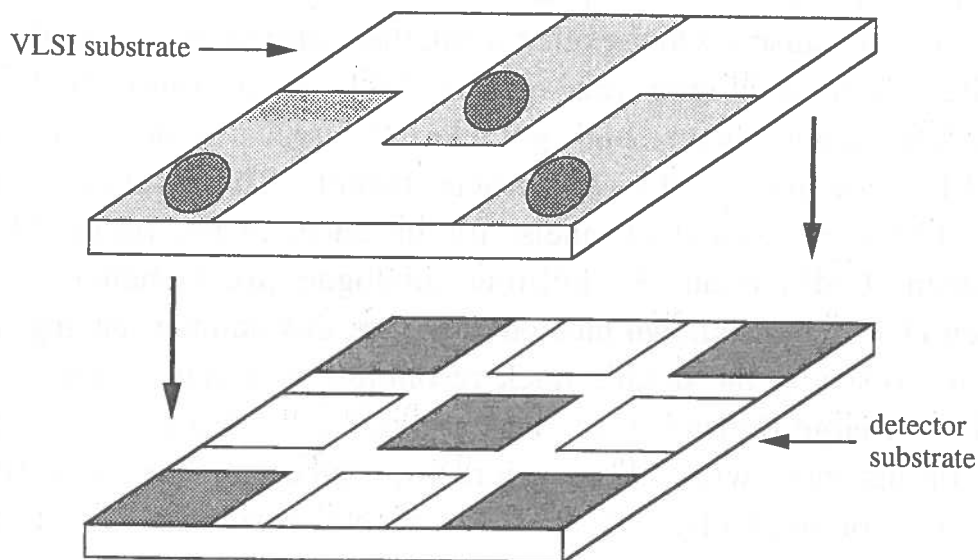


Fig: 15: Conceptual illustration of the possible decoupling of the VLSI cell and diode sizes allowed by capacitive charge division readout. The read out pixels are shown in grey as the bonding pads on the VLSI cells. In this example the electronics cell area is two times the diode one. The bias resistors for the intermediate pixels are not shown.

readout pixels, or placing them at the level of the VLSI chip. Both of these approaches present advantages and drawbacks; with polysilicon bias resistors on the detector substrate the number of bump-bondings is reduced, because only the readout pixels have to be connected to the VLSI cells. On the other hand, the detector fabrication is both more complicated and expensive. By integrating the bias resistors in the electronics substrate, the simplicity of the detector is maintained at the price of bonding all the pixels (readout and intermediate) and "wasting" some space on the VLSI chip for the bonding pads and bias resistors of the intermediate pixels.

In the foregoing discussion, a chessboard-like readout scheme is proposed, allowing a reduction of the total number of electronic channels by a factor of 2. Moreover, to enhance the coupling effects (point 3), the interpixel capacitances have been chosen to be larger than the ones obtainable simply by the geometry [11]; this is possible with a direct integration of coupling capacitances among pixels on the detector substrate [20].

5. Simulation of a chessboard-like readout

5.1 DC bias of intermediate pixels

A simulation was performed in order to investigate the proper DC bias for the unbonded pixels. With reference to Fig. 2, only the resistive network has been taken into account. A depletion voltage ramp from 55 V to 65 V was applied between the backplane and the pixels kept at ground potential by the preamplifier inputs. Fig. 16 shows the effective potential difference polarising the pixels for 10 M Ω interpixel resistances (R_{diag} was left to 100 G Ω). As it can be seen no practical difference is noticed and this is found to hold up to 1 G Ω . In fact, any disuniformity is expected to be of the order of $R_{\text{ip}}/R_{\text{bulk}}$. So, when the interpixel resistance is small with respect to the bulk one, a uniform DC bias is obtained for all the pixels, thus leading to the uniformity of electric field lines in the detector bulk. This is of fundamental importance to avoid any charge collection disuniformity.

Moreover, the interpixel resistance must be chosen large enough to prevent resistive charge division from dominating while sufficiently small to avoid bias disuniformities in the (very likely) case of some pixels having large leakage currents. In our simulations, for simplicity,

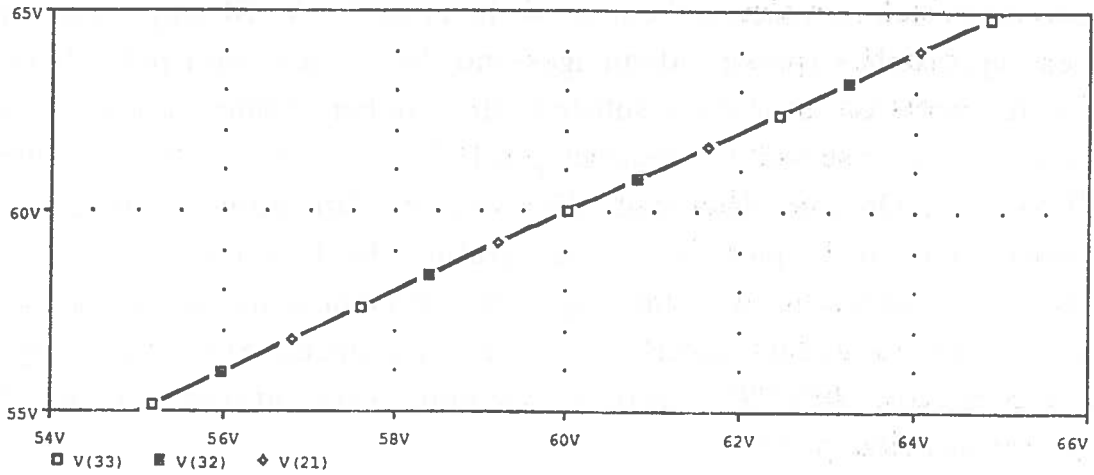


Fig. 16: Effective depletion voltage appearing at the central pixel (supposed to be connected to a preamplifier) and at its first neighbour, V(32) and its second neighbour, V(21) both not connected in the chessboard-like readout scheme. By symmetry, all intermediate pixels are considered. The bias resistors have a value of $10 \text{ M}\Omega$.

we have assumed all the pixels to draw the same leakage current and interpixel resistance of $30 \text{ M}\Omega$. Thus, in the chessboard-like readout scheme, the resistance between two adjacent amplifiers is close to $60 \text{ M}\Omega$ and, assuming C_j of about 3 fF ($90 \mu\text{m}$ pixel side), we have a RC of about 200 ns , substantially larger than the shaping times foreseen at the future LHC experiments; this ensures that resistive charge division is negligible [21].

5.2 Simulation scheme

The simulation program works as the reference one of Subsection 3.1 with three main differences: g_m has been increased to 0.8 mS and C_f to 15 fF to take into account the increased detector capacitance (because of the increased interpixel capacitances) and the total detector capacitance is no longer given by (vi), but by the following:

$$C_D = C_j + 4C_{\text{diag}} + 2C_{\text{ipx}}^* + 2C_{\text{ipy}}^* \quad (\text{vii})$$

where

$$C_{\text{ipx}}^* = C_{\text{ipx}}(C_{\text{ipx}} + 2C_{\text{ipy}} + C_j) / (2C_{\text{ipx}} + 2C_{\text{ipy}} + C_j) \quad (\text{viii})$$

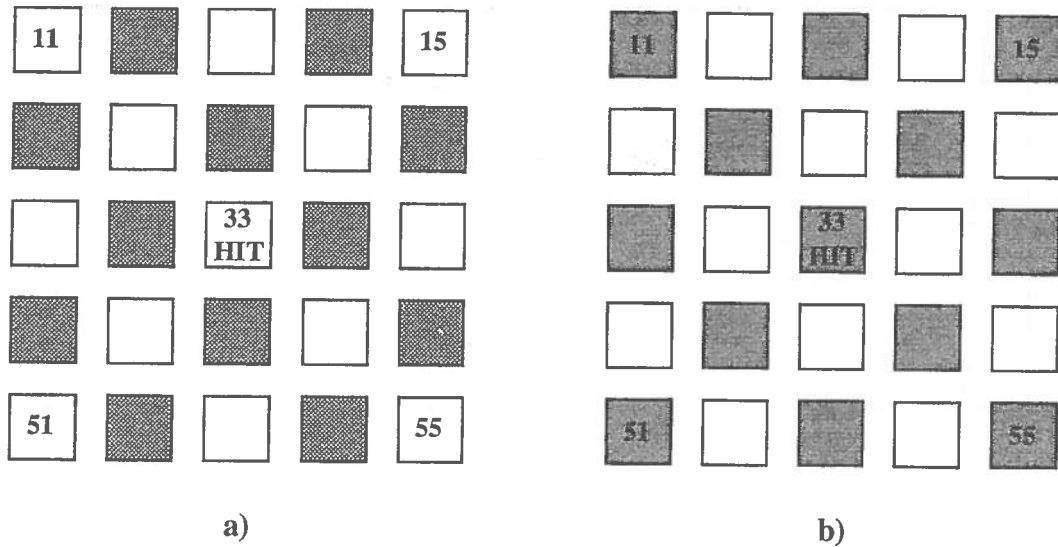


Fig. 17: The two possible situations occurring with a chessboard-like readout scheme. a) The hit pixel is not read out while b) it is also read out.

i.e. the series sum of C_{ipx} with $(C_{ipx}+2C_{ipy}+C_j)$, being this last quantity the parallel sum of the capacitances seen by each amplifier via C_{ipx} . C^*_{ipy} is obtained simply by interchanging the indexes.

Actually, two cases must be considered: in the first and most important one, the hit pixel is not directly bonded to a preamplifier while, in the second one, the hit pixel is read out (see Fig. 17).

5.3 Results in the first case

We considered pixels (90 μm side, 10 μm gap) having an interpixel capacitances along the axes of 25 fF (C_{diag} was kept at 5 fF, see Ref. [12]). This value has been chosen in order to have $C_{ip} \approx 10 C_j$. The purely geometrical interpixel capacitance would be only 8 fF (see Table 1). The results are shown in Figs. 18a-b. As it can be seen the induced signals on the FNPA is 60 mV while the SNPA outputs have a peak of about 3.75 mV.

5.4 Results in the second case

Now, the HPA output is shown in Fig. 19a. Its peak amplitude is 260 mV while the FNPA and SNPA outputs (shown in Fig. 19b) have peaks of 3.75 mV and 1.50 mV respectively.

Even without any quantitative noise consideration, it is evident that a signal close to the 23% (60 mV/260 mV) of the HPA output is not negligible and large enough to be detected with analogue readout.

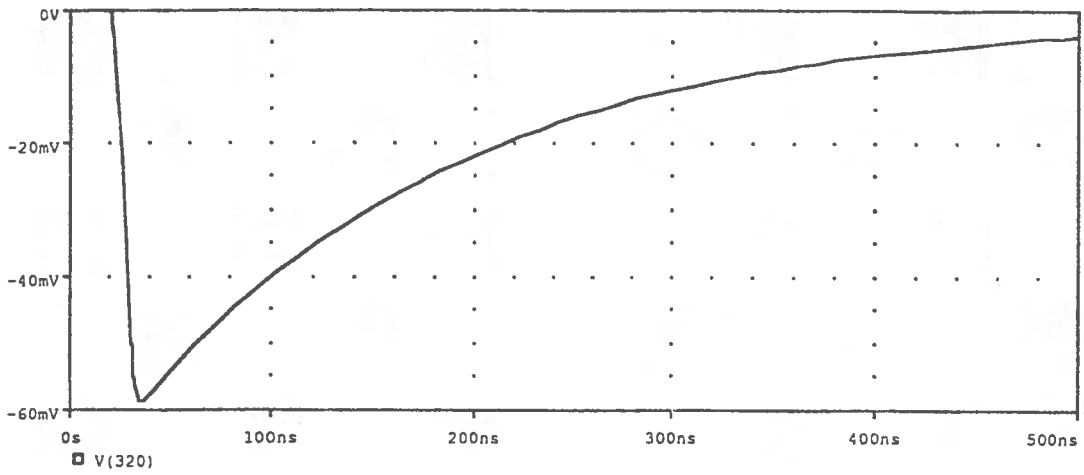


Fig. 18a: FNPA output in the case of central pixel hit but not read out.

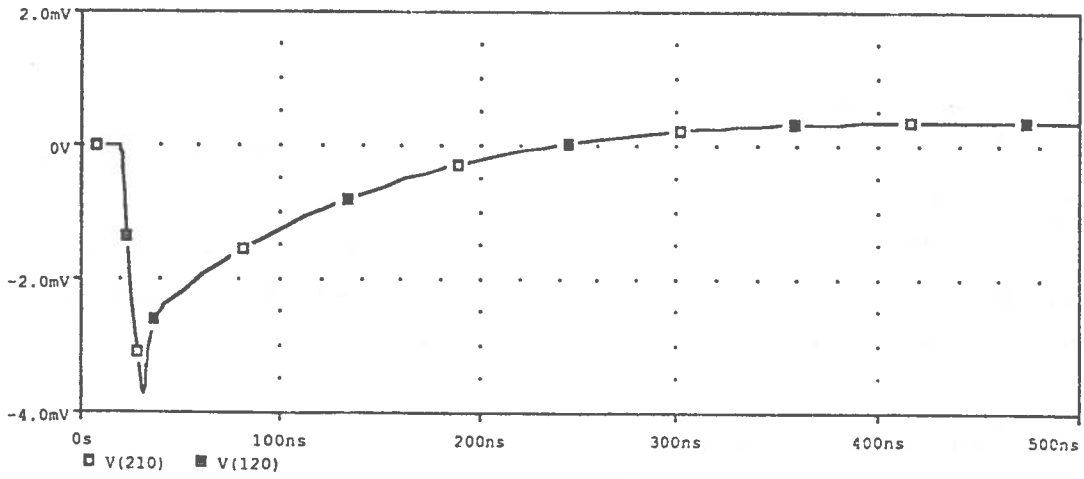


Fig. 18b: SNPA output in the case of central pixel hit but not read out. The two are identical by symmetry.

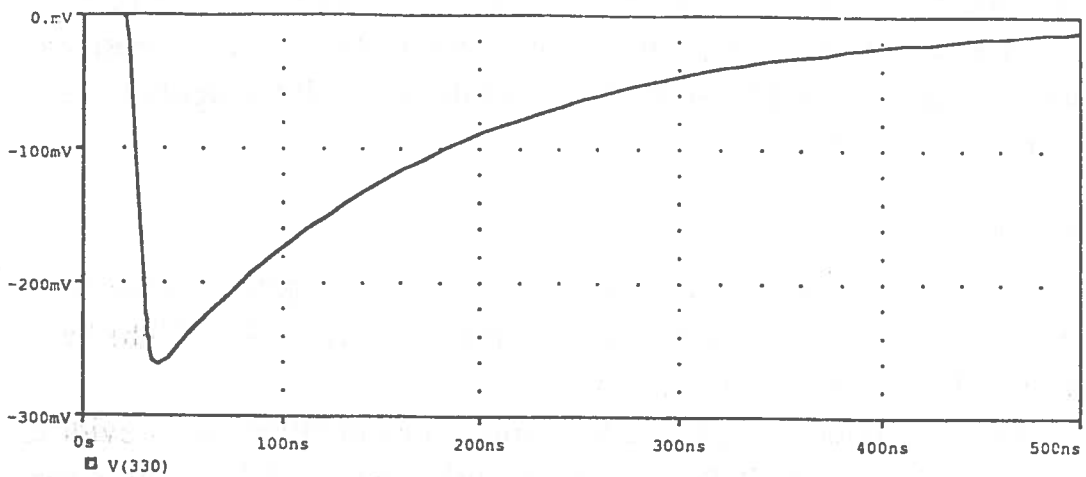


Fig. 19a: HPA output in the case of central pixel hit and read out.

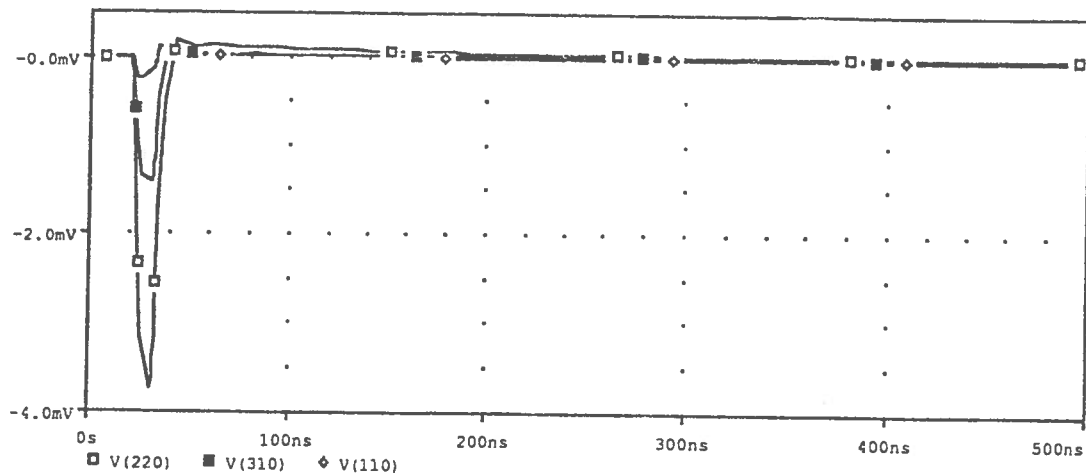


Fig. 19b: FNPA and SNPA outputs in the case of central pixel hit and read out.

6. Conclusions and perspectives

A detailed study of the capacitive cross-talk phenomena occurring in DC-coupled hybrid silicon pixel detectors has been done. The dependence of these effects on several critical detector and electronics parameters has been studied. It turns out that, with binary readout and a reasonable threshold, these effects are negligible while, if a low noise analogue electronics is employed, they can be easily detected.

This being the case, it has been shown that it is, in principle, possible to use capacitive coupling to effectively reduce the number of readout channels. Moreover this would allow to decouple the geometry of the diode from that of the VLSI cell. Of course, other readout schemes, with more intermediate pixels among the read out ones, are possible.

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The first part of the document discusses the importance of maintaining accurate records of all transactions. It emphasizes that every entry should be supported by a valid receipt or invoice. This ensures transparency and allows for easy verification of the data.

In the second section, the author details the various methods used to collect and analyze the data. This includes both manual and automated processes. The goal is to ensure that the information is both reliable and comprehensive.

The third part of the document focuses on the results of the analysis. It shows that there is a clear trend in the data, which suggests that the current strategy is effective. However, there are some areas where improvement is needed, particularly in terms of efficiency and cost reduction.

Finally, the document concludes with a series of recommendations for future action. These include implementing new software tools, training staff on best practices, and conducting regular audits to ensure ongoing compliance and accuracy.

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