ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Pavia

INFN/TC–94/03
1 Marzo 1994

S. Altieri, O. Barnaba, P. Bruschi, F. Fossati, A. Lanza and T. Pinelli:

A REMOTE CONTROLLED POLARIZER FOR SILICON DETECTORS

Servizio Documentazione
dei Laboratori Nazionali di Frascati

INFN - Istituto Nazionale di Fisica Nucleare
Sezione di Pavia

INFN/TC-94/03
1 Marzo 1994

A REMOTE CONTROLLED POLARIZER FOR SILICON DETECTORS

S. Altieri, O. Barnaba, P. Bruschi, F. Fossati, A. Lanza and T. Pinelli
Dipartimento di Fisica Nucleare e Teorica and I.N.F.N. Sezione di Pavia, via A. Bassi, 6
27100 Pavia, Italy

A remote controlled system to maintain polarization voltage across a silicon detector within a user defined window is described. The system compensates for the radiation damage induced voltage drop with a resistor in series to the detector circuit, so that the resistor voltage decreases with the polarization voltage. This Z80 microprocessor based system links with the host computer by a RS-232 serial port. The resolution of the system is less than 0.2 V .

1. – INTRODUCTION

An experiment is running in our laboratory at L.E.N.A., University of Pavia, to study eventual fission fragment decays with emission of charged particles. Fission fragments are exotic nuclei discretely far from the natural stability line, then further properties of nuclear matter could be evidenced by an extensive analysis of their rare decay modes[1].

The experimental apparatus, whose setup is sketched in Fig. 1, presents the following performance: identification and energy measurement of the released particle, possibility of evaluating the parent fragment mass and meanlife within a range from few ns up to some μs.

The fragments are provided by a 50 μCi ^{252}Cf source giving an intensity of about 100 fragments/s on both F1 and F2 detectors. Due to such a low rate of production of the observable nuclei, very long running times are required to reach statistically significant results: we planned to run 24 hours per day for one entire year at least.

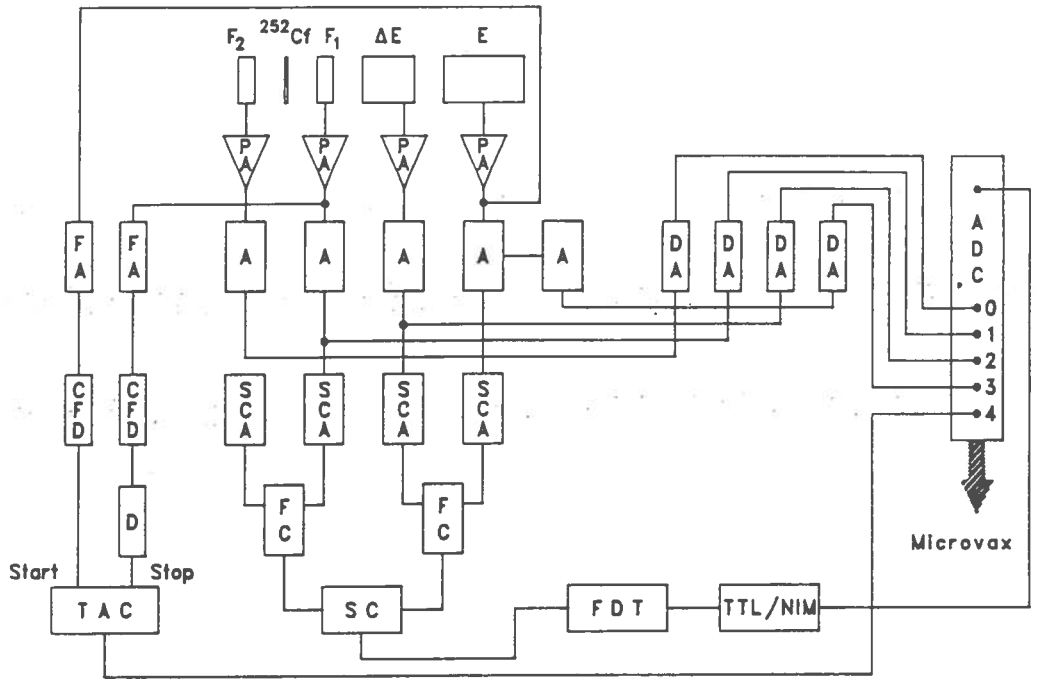

Fig. 1 - Experimental apparatus:
F1, ΔE = totally deplated surface barrier silicon detectors
F2, E = partially deplated surface barrier silicon detectors
PA = preamplifiers
A = amplifiers
FA = fast amplifiers
CFD = constant fraction discriminators
SCA = single channel analyzers
D = delay
TAC = time to amplitude converter
FC = fast coincidence
SC = slow coincidence
FDT = fast delay trigger
DA = delay amplifier
ADC = analog to digital converter

Being this the situation, one of the most delicate problems consists in the necessity of keeping both fragment detectors polarized at a predetermined voltage despite of the fast radiation damage caused by fission fragments. It is our experience that in 15 days the fragment detector resolution is seriously deteriorated as the reverse current reaches values around 5-6 μA.

Then, in order to realize a continuous check and adjustment of detector bias, we decided to design a simple, not expensive device capable of an automatic regulation of the voltage at values inside a predetermined interval.

2. – GENERAL DESCRIPTION

The basic idea to maintain the detector polarization voltage constant is to connect in series between the power supply and the detector a resistor R_x with variable value, as drawn in Fig. 2. This value depends on the increase of the current flowing in the circuit.

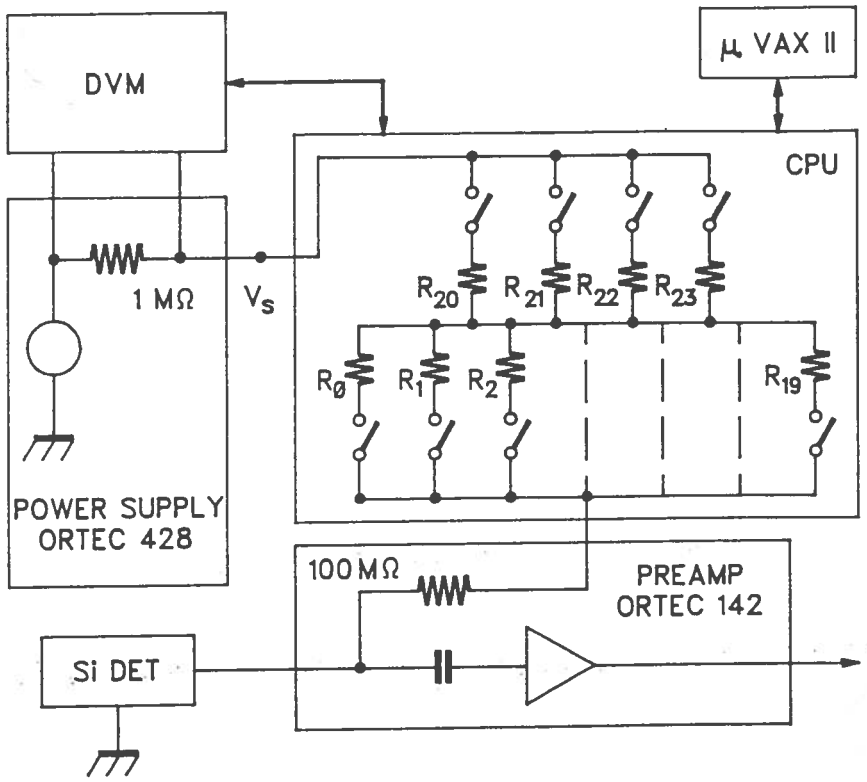

Fig. 2 - Block diagram of the system.

The global system is composed of a manually variable power supply unit (Ortec Mod. 428[2]), a digital multimeter (DVM Fluke 8050A[3]), a preamplifier (Ortec Mod. 142[4]) and a NIM module containing the system CPU and the related electronics. The host computer is a Microvax II.

The power supply unit can range from 0 to 1kV, and the flowing current is monitored by means of a 1MΩ sensing resistor inside it . The DVM has $4\frac{1}{2}$ digits, and it is set to 20 V full-scale to measure the voltage drop on the sensing resistor; the display value gives the current intensity in μA. We have modified the DVM, adding an external connector, in order to read-out the digitized value shown by the display: the available signals on this connector are the 5 bit data bus (4 bits plus the decimal point), the 5 data strobes (one for each digit), and the power supplies. Because of the reverse voltage used to supply the CMOS display drivers into the DVM (-5V), optical couplers between these signals and the NIM module are required.

The NIM module is the heart of the system. It contains the CPU, a 4 MHz Z80 microprocessor, the UART, for communications with the host computer through a RS-232 serial port, and the precision resistors for plugging in the detector circuit.

The CPU has 4 kbytes of Eprom (from 000 to FFF) and 1 kbyte of RAM (from 8000 to 83FF), and reads the DVM data, after their demultiplexing, through an 8255 PIO. Since the sign and the decimal point are not used and the last digit is only partial, the DVM data bits are only 17. Their read-out begins on the rising edge of the strobe signal of the least significant digit, interrupting the CPU via the maskable interrupt input, but also the read-out via polling is possible, due to the existence of an Interrupt Register mapped in the CPU I/O space.
The system requires some parameters for properly working, and although they are normally supplied by the host computer, it is possible to set them manually through 10 rotary microswitches on the front panel which are read by the CPU.

The choice of the system running mode, either remote or manually controlled, is done by means of a switch put on the rear panel: in the remote mode all parameters and Reset and Start signals are supplied by the host computer; the CPU reads the parameters through the microswitches, being Reset and Start signals generated via pushbuttons, in the manual mode.

The plugged in resistors are 24 in total: the last 4 are put in series to the other 20, in such a way as to get 80 resistor values, so the insertion of 2 resistors at the same time instead of 1 is required. They are driven by the CPU (mapped in the memory space) through reed relays.

Finally, the communications between the CPU and the host computer are managed by a 2681 UART; its internal registers are loaded by the CPU during booting.

3. – SYSTEM WORKING PROCEDURES

The system performs 4 principal tasks: the bootstrap, the DVM reading, the host command waiting (when the system is in remote mode) and the computation of the formulas to maintain the correct polarization voltage.

During the bootstrap phase the CPU connects the highest resistor value (really 2 resistors in series) in the detector circuit and tests the status bit in the Status Register to determine whether the system is in remote or in manual mode; in the first case the CPU loads the

parameters via software; the parameters are loaded by the external microswitches when the manual mode is set.

At the end of the bootstrap phase the CPU converts in the state of waiting for the host commands or the Start signal in the remote and manual modes respectively .

The DVM reading and the following polarization control can occur just after the Start signal, in both modes. This because the Start routine enables the maskable interrupt of the CPU, and the reading occurs at an approximate rate of 2 Hz.

During the reading and the polarization control phases the CPU can never be interrupted, whereas during the waiting time the host interrupt gets the highest priority with respect to the DVM interrupt: the Interrupt Register informs the CPU about the origin of the interrupt .

The polarization control is executed by calculating the maximum and minimum currents flowing in the circuit when the polarization voltage of the detector is at the smallest and largest value respectively. These values depend on the detector in use being seen by the user as system parameters.

The calculations are performed according to the following relations:

$$I_{max} = \frac{V_s - V_{pmin}}{R_n + 101} \qquad (1)$$

$$I_{min} = \frac{V_s - V_{pmax} - V_{of}}{R_n + 101} \qquad (2)$$

where V_s is the power supply voltage, V_{pmin} and V_{pmax} are the minimum and the maximum polarization voltages, and V_{of} is a small voltage necessary to create a hysteresis and avoid oscillations when the system changes the plugged in resistor; at present V_{of} is set to 2 V. R_n is the total resistor value connected in the circuit; to this value the input resistor of the preamplifier and the sensing resistor of the power supply (101 MΩ) are added (see Fig. 2). By expressing the voltages in Volt and R_n in MΩ, I_{max} and I_{min} are expressed in μA.

V_s, V_{pmin} and V_{pmax} represent the above mentioned system parameters. V_{of} cannot be changed via software: for simplicity, it can be changed only with an Eprom reprogramming. The maximum acceptable values for the parameters are:

$$V_s = 999 \text{ V} \qquad V_{pmin} = 99 \text{ V} \qquad V_{pmax} = 99 \text{ V}$$

During the bootstrap phase these 3 parameters are loaded with their default values:

$$V_s = 999 \text{ V} \qquad V_{pmin} = 25 \text{ V} \qquad V_{pmax} = 30 \text{ V}$$

In order to safeguard the detector, these default values were determined in such a way that I_{max} never exceeds the largest possible value in the circuit when the detector gets its lowest value of polarization.

The system configuration starts at the maximum resistance condition, being R_1 and R_{21} connected in series. The system evolution is determined by a periodic interrupt signal that, at a generic time when a given R_n resistance is loaded, starts the CPU check and regulation cycle. Such a cycle includes the following steps:

i) I_{max} and I_{min} calculation.

ii) Comparison between I_{max} and the current value read by DVM.

iii) If I_{max} is lower than the DVM value, the R_{n+1} resistance, having a value lower than R_n, is loaded.

iv) If I_{max} is larger than the DVM value, a further comparison is made between I_{min} and the same DVM value.

v) If I_{min} is larger than the DVM reading, then the resistor R_{n-1}, of a higher value with respect to R_n, is connected.

vi) If I_{min} is lower than the DVM reading, the CPU does not change the resistor configuration and remains in waiting for the next interrupt.

When a new resistor is connected according the above procedure, the CPU waits for 20 seconds before starting a new cycle. This is to avoid a too frequent resistance variation of the system.

4. – SELECTION CRITERIA FOR RESISTOR VALUES

The equations (1) and (2) permit the calculation of the resistor values when the parameters V_s, V_{pmin} and V_{pmax} are chosen.

The silicon detector current can roughly range from 0.2 μA to 5-6 μA. The minimum plugged in resistance is obviously the short-circuit, and in this condition the minimum total resistor value in the circuit is 101 MΩ. With V_{pmin} = 25 V and I_{max} = 5 μA, from equation (1) we have V_s = 530 V, that can be rounded to 500 V for simplicity; on the other hand from the equation (2), with V_{pmax} = 30 V and I_{min} = 0.2 μA, we obtain R_{ntot} = 2340 MΩ, that would correspond to a plugged in resistor value of 2239 MΩ.

The use of such a value is not practical and the stray resistance of the substrate is no longer negligible; moreover the resistors to be connected become too many (some hundreds). To improve the operative situation we decided to hand regulate by steps the Vs value in such a way that a limited number of variations allows the system to work in satisfactory conditions during the detector lifetime. V_s value must be manually changed each time the maximum current is reached. To cover the 500 V range, five V_s variations are sufficient. Then, being 15 days the mean life of a typical detector, the frequency of the manual regulations is limited to 10 per month. In order to realize a completely automatic device, we plan to design a simple solution where the proper voltage scale is selected by a resistive voltage divider controlled by the CPU.

To reach an adequate precision, each resistor is realized by a series of four units, three of them being standard 5% tolerance resistors and one a trimmer for the fine tuning of the value.

The resulting total value of each resistor has been measured and trimmed with a high precision electrometer, capable of measuring up to 10^{16} Ω.

The value of each resistor was determined by using equations (1) and (2) in a serial sequence. First of all, from (1), with $R_n = 0$, $V_s = V_{smax} = 500$ V and $V_{pmin} = 25$ V, I_{max} is determined; substituting this current value in (2), with the desidered V_{pmax} (30 V in our case), R_1 is calculated. Then from (1) with $R_n = R_1$ we get the maximum current flowing in the circuit, being R_1 connected. R_1 is the resistor value for which the circuit current corresponds to I_{max} when the polarization voltage is minimum (V_{pmin}) and to I_{min} when the polarization voltage is maximum (V_{pmax}). Substituting the current value calculated with (1) in (2) we obtain R_2, and so on.

When a variation of V_{pmin} and V_{pmax} is necessary and the 5 V gap remains unchanged, the resistor values calculated are still valid, if V_s is increased or decreased by the difference between the new V_{pmin} and 25 V. When the gap must be changed, then a new calculation of the resistor values is necessary.

As above mentioned, the resistors have been subdivided into 2 groups, one of 20 and the other of 4 resistors. The resistance plugged in the circuit is given by the sum of 2 physical resistors, one in the first and one in the second group; then the possible values are 80. By the calculation procedure just described, all the 20 values of the first group resistors can be determined: the 21st plugged in resistance has the value given by the second resistor of the second group (being the first equal to zero, obviously). After that we can only calculate I_{min} and I_{max} for the predetermined resistors, excluding the 41st calculation cycle, that gives the value of the third resistor in the second group, and the 61st cycle that makes possible the determination of the last resistor in the second group.

The 24 resistor values having been calculated, it is necessary to find the V_s values capable of covering the entire current range from about 0.2 μA to about 5 μA; the number of V_s steps with the relative values is achieved by imposing that the last I_{max} value in a given V_s step is equal to the initial I_{min} value in the next one having an increased V_s.

In Fig. 3 the calculated I_{max} and I_{min} shapes as a function of R_n for the 5 V_s values are drawn. The two curves clearly show the four jumps between adjacent values (at the points 80, 160, 240 and 320), and, with less evidence, the three minor jumps inside a single V_s step. For clarity, the first of the largest jumps is enlarged in Fig. 4.

We can obtain the theoretical curve of the current from the equations (1) and (2). In fact, extracting R_n from (2), substituting it into (1) and repeating n times this procedure, we obtain:

$$I_n = I_0\left(\frac{V_s - V_{pmin}}{V_s - V_{pmax} - V_{of}}\right)^n \qquad (3)$$

where I_0 is the point 0 current.

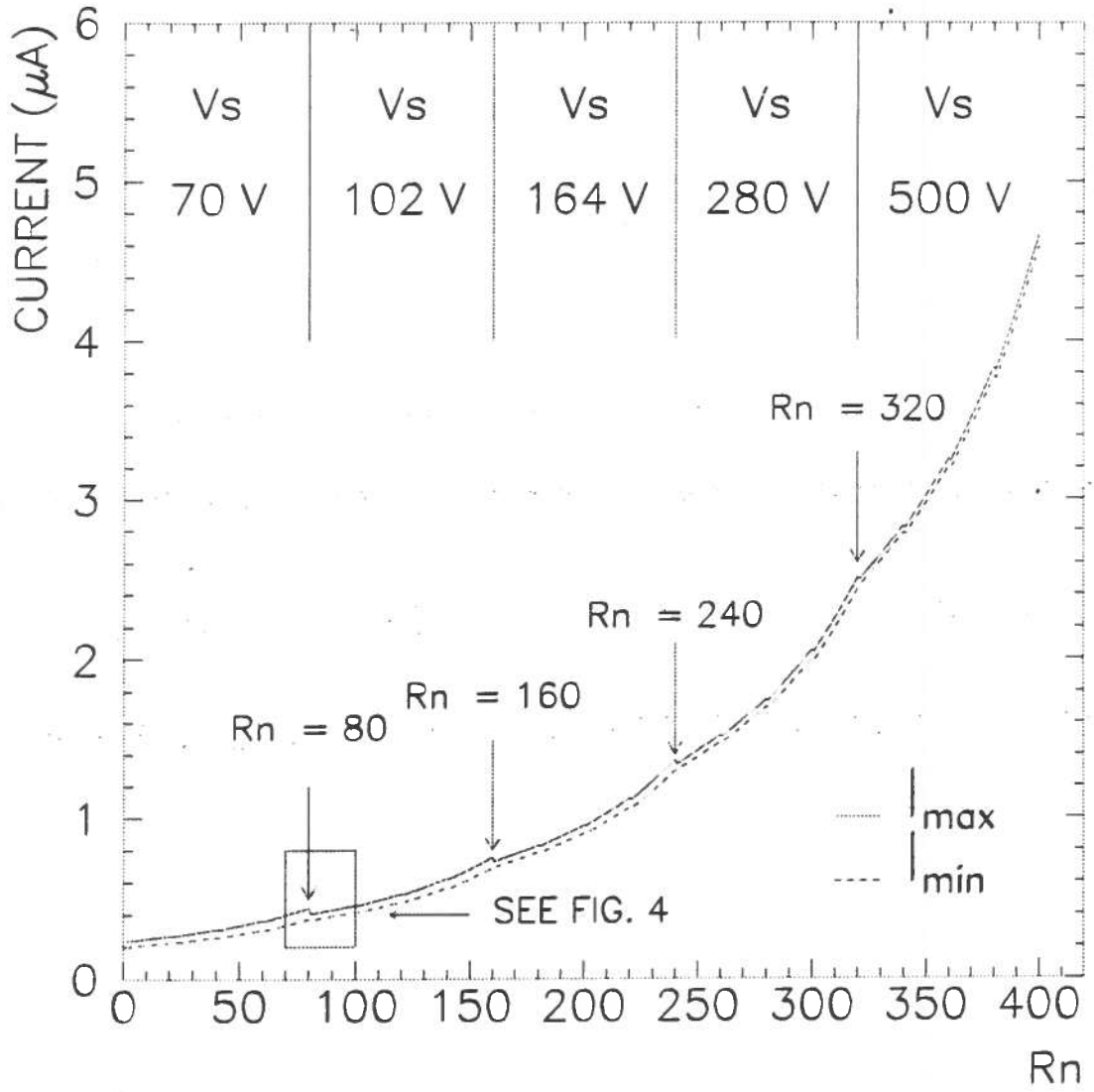

Fig. 3 - I_{min} and I_{max} vs number of plugged in resistor. The values in abscissa represent the index n of R_n and are shown in progressive order for all the 5 ranges of V_s (80 resistors for each V_s value).

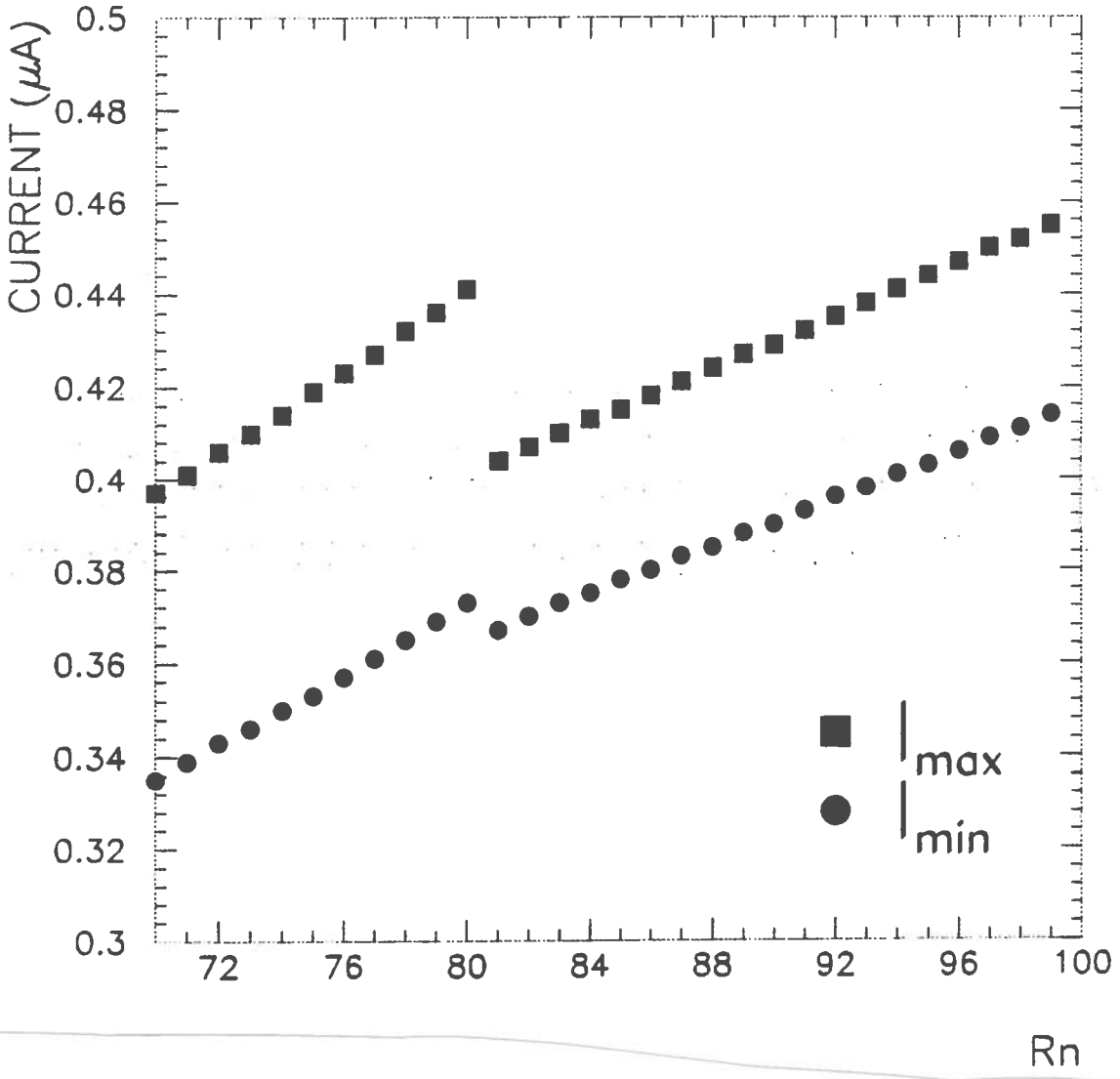

Fig. 4 - Enlargement of the Fig. 3 near the jump between the first and second V_s range.

5. – SOFTWARE PROTOCOL AND INTERFACE

The link between the CPU and the host computer occurs with the exchange of fixed length words: they can be 1, 2, 5 or 7 bytes long, in accordance with the fact that the word can be a host command acknowledge, a host command, a CPU data, and a host command with data. Since the host computer always adds a line feed character and a carriage return character before and after sending the message respectively, the real word length is extended to 3, 4, 7 or 9 bytes. The CPU also adds the same 2 characters in the same positions when it transmits a message to the host.

The host computer sends to the CPU either commands or commands followed by data, while the CPU sends data or only acknowledges to the host.

The link is always started by the host, that sends a command or a command with data; then it waits for the acknowledge from the CPU and eventually for a data word.

The host commands are subdivided into two groups: write commands and read commands. They are listed in Table I. We can note that write and read commands always begin by W and R characters respectively.

Table I – Host read and write commands along with their function.

Write commands	Function
WS <data>	Writes power supply voltage
WL <data> <data>	Writes minimum and maximum polarization voltages
WC <data>	Writes maximum current
WU <data>	Writes minimum current
WM <data>	Writes DVM current value (for debug purpose)
WR <data>	Writes address of the resistor to be connected in the circuit
WT	Writes system Reset
WI	rites system Start
Read commands	**Function**
RS	Reads power supply voltage
RL	Reads minimum and maximum polarization voltages
RC	Reads maximum calculated current
RU	Reads minimum calculated current
RM	Reads DVM current value
RR	Reads address of connected resistor
RA	Reads system status remote/manual

A command consists of two characters. When these characters are correct, in the sense that they belong to the coded table, the CPU identifies them. Then the five data are read according to the command itself. The CPU sends to the host the character V or E in case of positive or negative check of the received command. In the first case, the CPU successively sends the requested data to the host, in the last case the CPU waits for a new host command.

The program running on Microvax II is written in Fortran and is menu structured. The user can choose between a single reading or writing command and a batch command that reads sequentially the power supply voltage, the DVM current, the values of the plugged in resistors, and finally calculates the detector polarization voltage.

During the run the polarization voltage is monitored with a batch program that reads all useful data at predetermined intervals.

6. – PERFORMANCE AND CONCLUSIONS

The realized system allows the on-line control of the polarization voltage of a silicon detector in a very effective way. Because of the DVM full-scale value set to 20 V, the sensitivity of the flowing current measure is 10^{-9} A. From the equation (1) we can obtain the voltage resolution of the system with $R_n = 0$ and with $R_n = R_{nmax} = 88.5$ MΩ:

$$\Delta V_s = I_n(R_n + 101) + V_{pmin} - [I_{n-1}(R_n + 101) + V_{pmin}] = \Delta I(R_n + 101) \quad (4)$$

With $R_n = 0$, $\Delta V_s = 0.1$ V, whereas with $R_n = 88.5$ MΩ, $\Delta V_s = 0.19$ V.

By comparing with the most popular H.V. systems remotely controlled, we observe that a better resolution is obtained by our device.

The system is easily controlled by whatever type of computer, assuming that a serial port is available and the host program follows the above described link protocol. Moreover it is inherently reliable in case of failure or power-down.

Such a system can solve the problem of an accurate control of the apparatus response in long run experiments, where very low event rates and fast damage of the detectors are expected.

ACKNOWLEDGEMENTS

We are indebted with Prof. M. Cambiaghi for his relevant suggestions and with Mr. G. Bonaschi for the quality of drawing.

REFERENCES

(1) K.P. Jackson et al, *Phys. Let. B 33*, 281 (1970)
H.J. Rose and G.A.Johnes, *Nature 307*, 245 (1984)
J.C. Hardy, *Science 227*, N. 4690, 991 (1985)

(2) EG&G Ortec 428 Operating and Service Manual

(3) Fluke 8050A User's Manual

(4) EG&G Ortec 142 Operating and Service Manual