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A PC BASED SILICON DATA ACQUISITION SYSTEM

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Abstract

In this paper, we describe a user-friendly data acquisition system hosted by a Personal Computer for testing the Silicon Microvertex Detector (SMD) by controlling the programmable SVX-H silicon detector readout chips. The hardware set up is based on SRS/SDA CAMAC modules. The DAQ program is a menu and panel driven package running under LabWindows. Data are finally processed on a VAX computer system.

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1. INTRODUCTION

A data acquisition system based on PC 486 aimed to test the high precision double-side Silicon Microvertex Detectors of the L3 experiment at CERN [1] during its assembly period has been developed in the Perugia INFN Section. Hybrids, converters and half ladders of the L3-SMD can be tested using this system to check its digital and analog characteristics. The DAQ system contains two acquisition chains with the purpose to read out both the p-side and n-side of the Si detectors. It is designed to replace a previous system hosted by a micro VAX computer [2].

This paper is organized as follows: In section 2 we give a brief description of the front-end readout SVX chip used in SMD; in section 3 we explain the hardware setup of the data acquisition system; in section 4 we describe the details of the DAQ software; in section 5 we describe the data analysis procedure and present some results.

2. THE SVX CHIP

The SVX is a full custom VLSI chip developed at Lawrence Berkeley Laboratory for silicon microstrip detector readout [3, 4]. The IC is comprised of the an analog and a digital section. The analog section of each SVX chip includes 128 channels of a high gain charge amplifier followed by a stage of sample and hold, threshold storage, comparator, comparator latch, those are operated by opening and closing switches. The digital section contains an 8 bit bi-direction Digital Bus and some digital control lines. When operating the chip, a threshold is stored, incoming signals are then compared to the threshold to establish which channels have received a hit. When the SVX is read out, the readout sequence only switches to those channels above the threshold (Sparse readout mode).

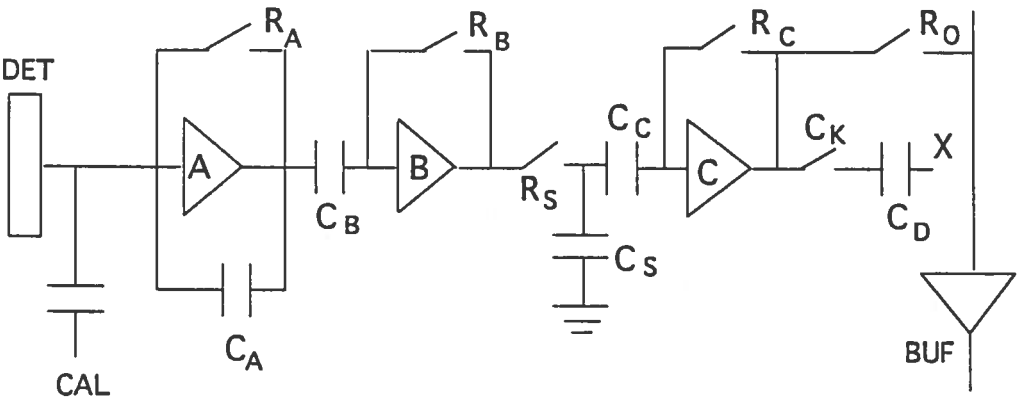

Figure 1. Analog circuit of a single channel

During the process, the analog signal is placed on the analog out line while the two corresponding digital addresses (chip ID and channel address) appear on the Digital Bus. Another readout mode (Latch all mode) is to read out the information of all channels regardless of whether or not they are above the threshold. Fig.1 shows a logical layout of a single analog channel.

The sequences (which is called "microcode" or "pattern") to control the opening and closing of the switches of the analog circuit are generated by a CAMAC module SRS (SVX Readout Sequencer). Two main sampling schemes can be used to operate the SVX chip. In the Double correlated Sample and Hold, the output signal of each channel is the voltage difference measured before and after the beam crossing within a fixed integration time Δt. In the Quadruple correlated Sample and Hold, two Double S & H are performed with equal time before and after the beam crossing. The difference is taken as the output.

3. THE SYSTEM SETUP

The system setup is shown schematically in Fig. 2.

The system setup can be subdivided in five parts:

1. Three CAMAC modules: the SRS (SVX Readout Sequencer module), the SDA(SVX Data Accumulator module), and the DAC module, are the main system components [5,6,7]. The SRS module contains a 2910 programmable sequencer that generates patterns of signals to operate the devices under test. The microcode programs for the sequencer are developed, compiled on PC and downloaded into the SRS via CAMAC. The SDA module includes an 8 bit flash ADC to acquire, digitize the SVX analog out, and a set of parallel local memories to accept the ADC value as well as the associated chip ID/channel address; The DAC module is used to inject charges on the SVX threshold/calibration line.

2. To drive signals from/to the SVX chips, we use: "converter" boards, a "receiver" CAMAC module, and an "optoboard". Signals coming from the SVX chips are transformed in differential TTL mode by a "converter" board and then sent to the CAMAC system via a "receiver" module. For decoupling the grounds between the two DAQ chains reading the p- and the n- sides, an optoelectronic board ("optoboard") is used to make the DAQ chain of the n-side be operated at V_{bias} level [8].

3. Interface cards: The communication between host computer PC and CAMAC crate is a GPIB controlled system, where we use a GPIB PC2/2A card as PC interface [9], and use a GPIB/CAMAC interface module Kinetic System 3988 as CAMAC controller [10], which supports data transfer rates up to 600 Kilobytes per second.

4. Processors and software: Data acquisition is hosted by a PC 486 and requires at least 4 megabytes of RAM memory. Data analysis is done on VAX system. The two computers are linked via local network.

5. Power supplies: Two CAEN made Programmable Floating Power Supplies are used in the system to power the two DAQ chains [11].

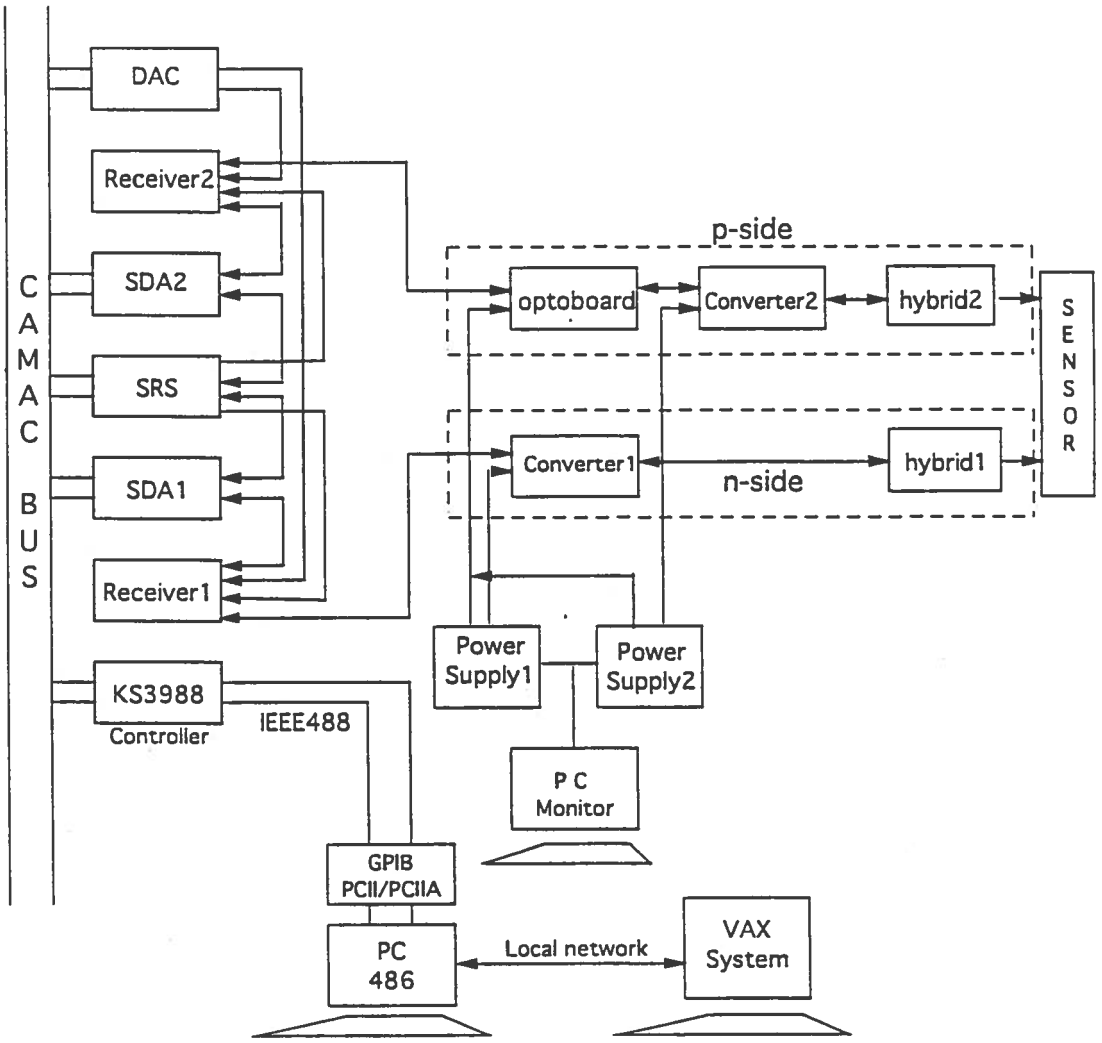

Figure 2. Scheme of the data acquisition system setup

4. THE DAQ SOFTWARE

The DAQ software consists of two packages: the microcode programs, the data acquisition program(DAQ).

Several microcode (or pattern) programs, which are organized in the specific format described in ref. [12], have been developed for different devices under test and different test purposes. They are: Digital Check to check the chip ID/channel address of each channel; Double Calibration and Noise test to measure the gain and noise of each channel using the Double correlated Sample and Hold mode; Quadruple Calibration and Noise test to measure the gain and noise of each channel using Quadruple correlated Sample and Hold

mode; Sparse Readout test to examine the sparse readout feature separately in Double-Negative (DN), Double-Positive (DP), Quadruple-Negative (QN) and Quadruple-Positive (QP) modes. These microcode programs operate as follow: DAQ program compiles the microcode, downloads it into the SRS, and starts its running. When the SRS sets the SDA's LAM, the host computer acquires the data, and resets the LAM, thus starts another cycle. Also another two SVX control patterns called Scope Pattern have been written to produce repeated analog out readouts.

The DAQ program, written in C, is a menu and panel driven package. It is developed under the support of Labwindows [9], which contains a powerful GPIB 488 and 488.2 library that makes it easy to communicate with the GPIB devices in our setup. The program can be run on PC and its compatible system. Due to the 640 kilobytes limits of DOS, the DAQ program can only be run under the Labwindows environment, which extends the program access space up to 16 megabytes. During the DAQ running period, panels status for addressing the setup and setting the test parameters are saved and can be recalled making the DAQ operation much easier.

The DAQ program includes two main functions: run SMD_Control to test SMD units; run System Test to diagnose the hardware and software or debug SRS microcode.

When running SMD_Control, DAQ executes the following tests:

1) Run scope pattern One scope pattern is downloaded into SRS and starts running. Since scope patterns are developed without the SDA LAM setting and resetting, the analog out is repeated. In this case one can observe the analog out shape and measure the voltage level with an oscilloscope.

2) Analog calibration check Different charges can be injected into the calibration line of SVX chips by writing different data to the DAC module. When one starts the scope pattern and applies different charge injections, one sees the analog out level (or LCD number in the front panel of SDA) which varies with the dac voltage value's change. The more positive the chosen voltage value, the lower is the output level (or LCD number). In this way one checks if the SVX calibration feature operates correctly.

3) Digital check This function of SMD_Control allows the check of the chip ID and channel address of each channel. Several check cycles are needed for this test. All channels with mismatched chip ID and channel address are displayed and recorded.

4) Double calibration and noise test This function is developed to measure the SVX gain, pedestal and noise in the Double S & H data acquisition pattern. Several acquisition cycles selected by the user are performed for each measurement over all the channels. For the gain measurement, DAQ executes several steps with different dac voltage injecting, and saves the mean readout values of each step, then a linear fit is performed for each channel. The noise measurement is done without charge injection into the calibration line. The mean pedestal value and noise value of each channel is calculated after all

acquisition cycles have been completed. During the data collection, the ADC readout vs channel number could be plotted on the screen, and the picture also can be saved and later printed out. An example of the chip baseline is shown in Fig. 3.

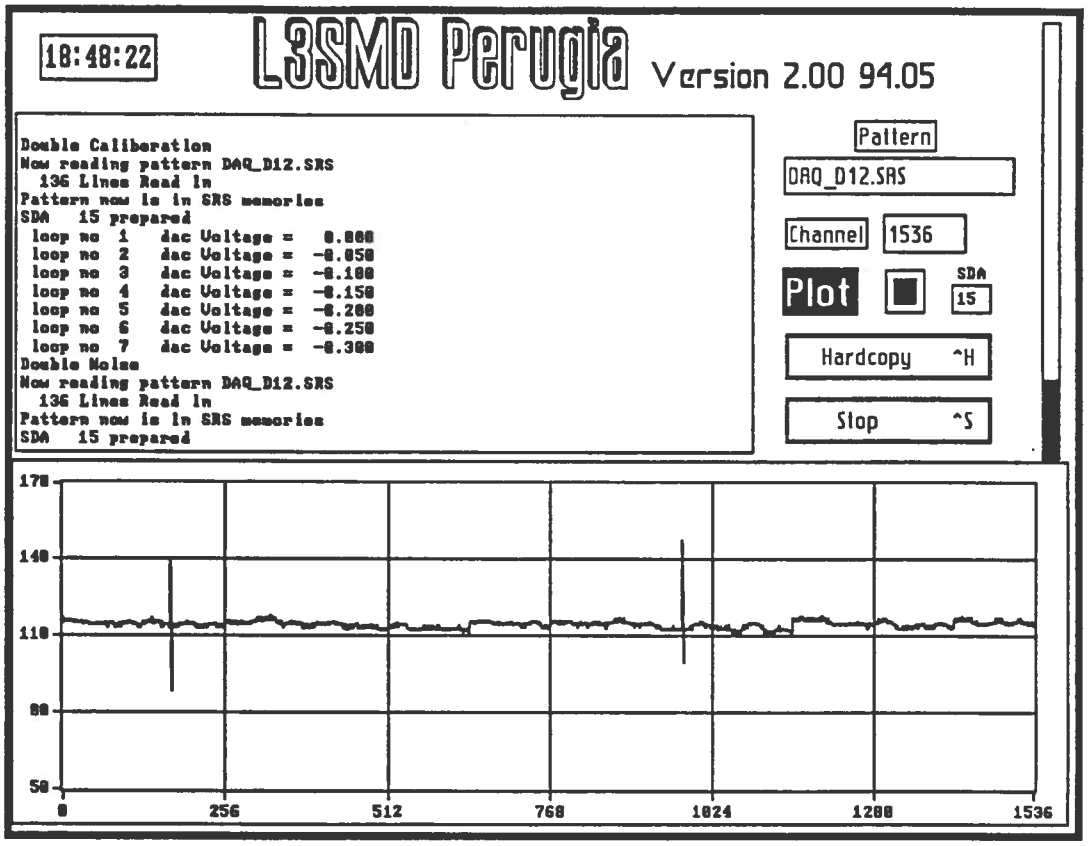

Figure 3. An example of the data acquisition display (1536 channels readout)

5) Quadruple calibration and noise test This function performs the same test over the devices under test as function (4) except the Quadruple S & H patterns are used for this measurement.

6) Sparse readout One of the four sparse scanning mode (DN,DP,QN,QP) can be selected to test the sparse readout feature of the SVX chips. The sparse readout test is done in the following way. First one selects the upper and lower threshold voltage for the sparse window and then set the scanning steps of the window and also the acquisition cycles for each steps. When the sparse pattern has been loaded and starts running, a threshold value is set. The chip ID/channel address of the latched channels (above the threshold) are read in, and the efficiency and the spread of the transition for each chip are calculated. The results of each step are displayed and saved when the selected acquisition cycles are completed. Finally, after all steps has been passed, DAQ gives the threshold corresponding to 10% channels latched of each chip, and the threshold corresponding to 90% channels latched of each chip. Fig.4 shows an example of the result of a sparse scan measurement.

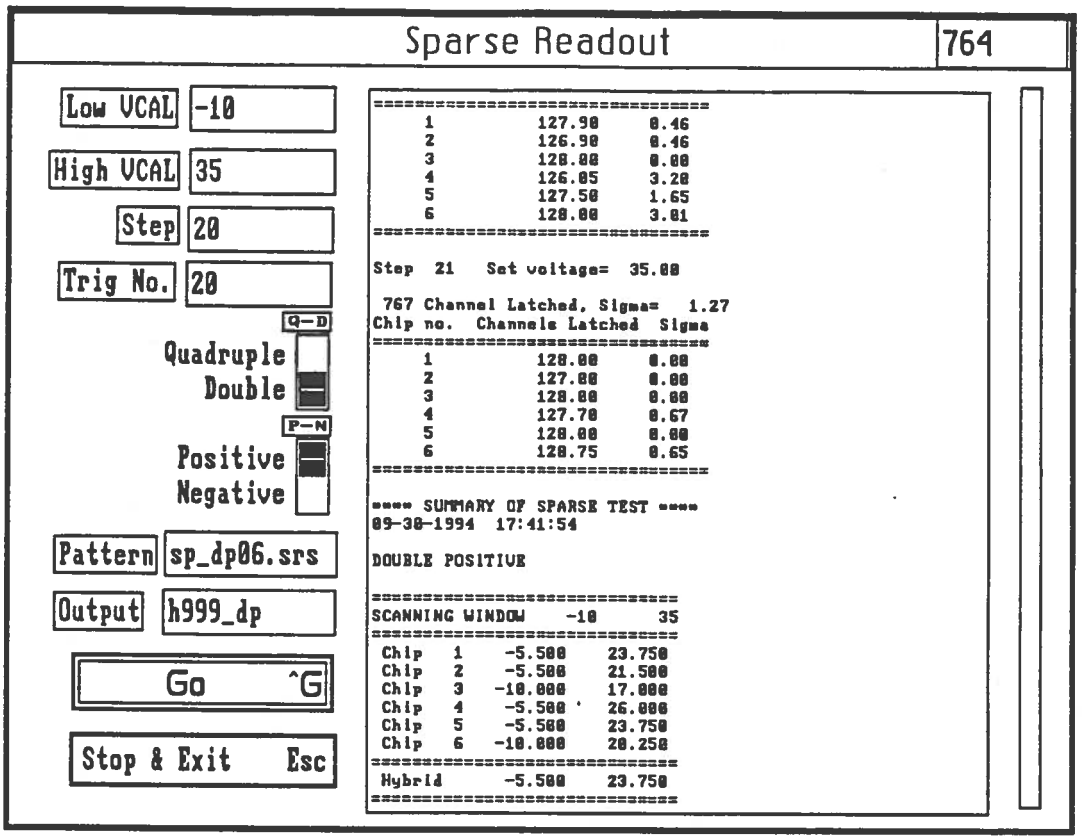

Figure 4. Picture of a sparse scanning

When running one of the System Test functions, the following operations can be selected to be executed:

1) Load a pattern This operation allows you to read a microcode program to PC-RAM, compile it, and write into the pattern buffer in binary format so that it could be downloaded to SRS.

2) Download to SRS This operation downloads the pattern in the pattern buffer to SRS memories.

3) Initialize SRS memories It writes 00 to all the SRS memories.

4) Initialize SDA memories It clears up all SDA memories.

5) Read SRS memories Executing this operation, the three SRS memories of the selected addresses are read out and displayed in binary and hexadecimal format. This feature allows you to check if the pattern is successfully downloaded to SRS.

6) Test SRS memories DAQ writes 0000 and FFFF(hexadecimal) to all the 3 SRS memories and reads it back, then compares the two values.

7) Configuration the hardware This operation allows you to address the CAMAC modules (SRS, SDAs, DAC, etc.).

8) Camac Talk This feature allows to execute CAMAC instructions immediately. A CAMAC operation can be structured by setting appropriate values of N (Slot Number), A (Address), F (Function), and a input data if needed. The return value, if exists, will be displayed.

9) Run data acquisition This operation uses the SRS pattern to collect data over the SVX chips under test for several cycles, and the ADC readout vs channel number can be plotted on the screen. This operation allows you to check if the pattern can work well.

5. DATA ANALYSIS

When a normal test, which includes digital check, double calibration & noise tests, and quadruple calibration & noise tests, has been done by running DAQ, the results are saved for each channel. These data are then transferred to VAX system via local network. On VAX, we run a log program to produce the final test report and create a database. In the report, noisy channels, channels with bad gain and dead channels are listed; mean pedestal, gain, noise, etc. for each chip are calculated by removing the bad channels. Further analysis based on the new database then is done by running a PAW procedure, and the distribution histograms of the gain, pedestal, noise, and difference noise for each chip are produced. Presently only the results of double sample calibration & noise test are used in our analysis. Fig.5 shows a result of a hybrid test.

In the analysis of sparse test data, the efficiency histograms of each chip and the full hybrid (each hybrid is equipped with 6 SVX chips) are produced. Fig.6 gives an example of the efficiency histograms of a sparse scan on a hybrid.

6. CONCLUSION

We have described the CAMAC-PC based data acquisition system to test the SMD SVX-frontend as well as the data analysis procedure. All DAQ functions described in this note have been successfully tested in Perugia. Converters and hybrids have been tested under the new environment and the analysis has been done on VAX. The results are consistent with the results obtained with the earlier micro VAX-based data acquisition system.

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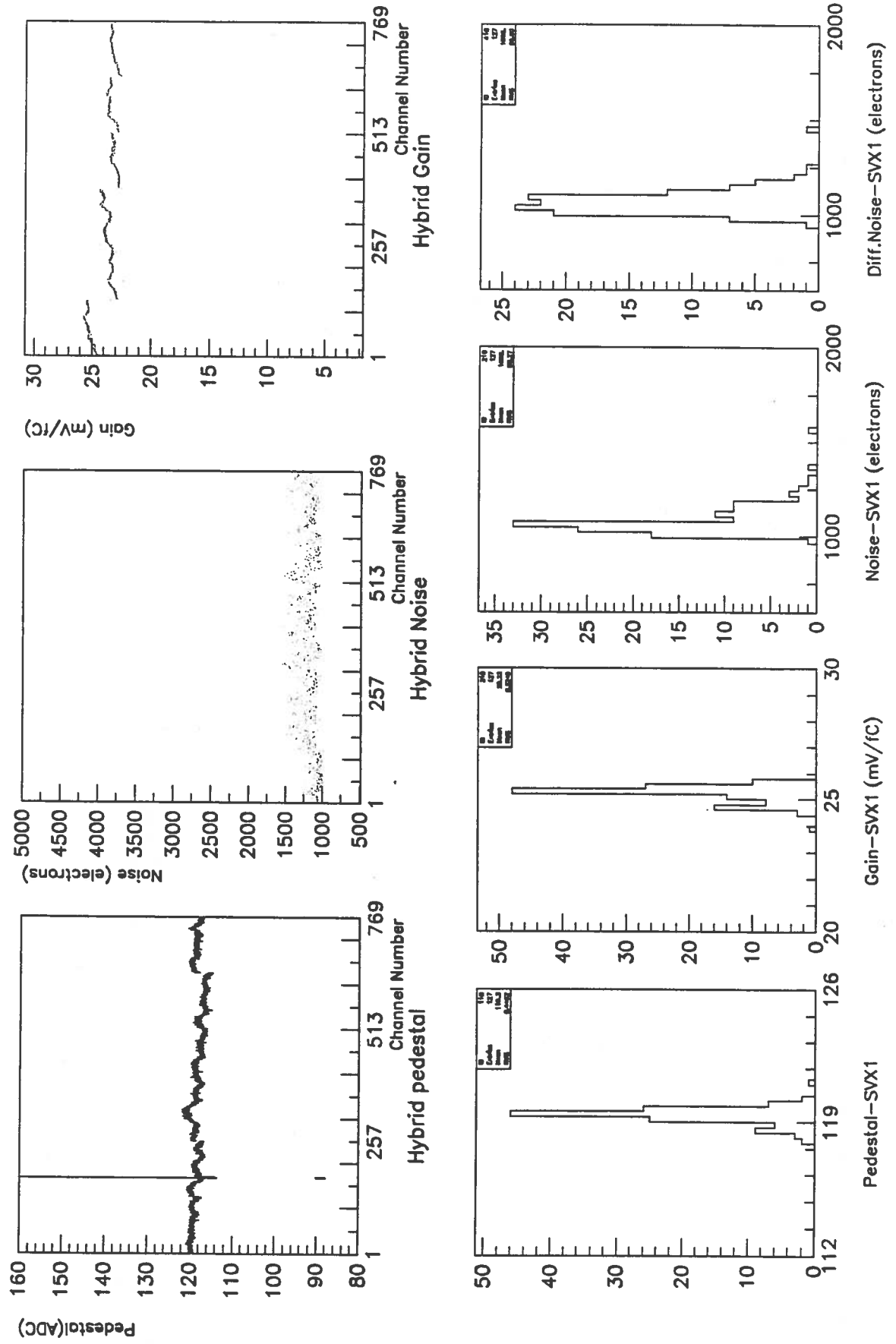

Figure 5. Result of a hybrid test

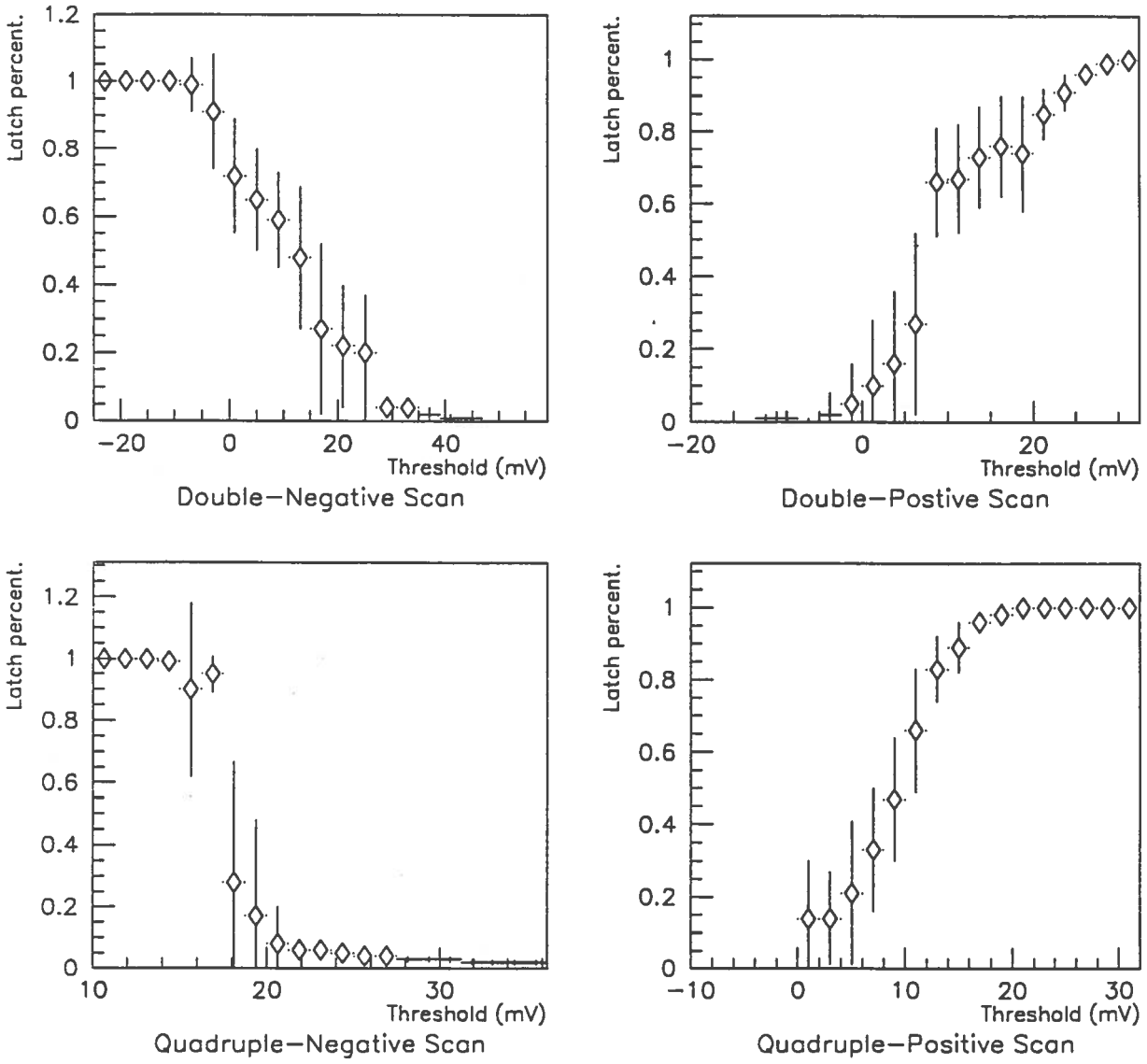

Figure 6. Result of a sparse scan on a hybrid