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JUNCTION AND INTERSTRIP CAPACITANCE OF SILICON MICROSTRIP DETECTORS

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ABSTRACT

Several measurements of junction (C_j) and interstrip (C_{is}) capacitance of silicon microstrip detectors have been performed. These quantities play an important role in determining the noise and cross talk characteristics of the detectors, since they dominate the capacitive load at the preamplifier input. Thus, the knowledge of the capacitive network among neighbouring strips is of fundamental importance for the detector and VLSI readout electronics design and performance, especially for the optimization of the signal-to-noise ratio.

1. Introduction.

Load capacitance is the most significant parameter determining the noise level of charge-sensitive readout electronics[1]. This is the total capacitance presented by the detector at the preamplifier input. For the case of silicon microstrip detectors, the significant contributions are those from the other strips on the detector surface and also from the backplane. The relative importance of these two contributions depends on the detector characteristics: implant and metal strip pitch and width, capacitive or direct coupling to the readout electronics, type of doping, etc. As a general statement, one can say that if the strip pitch is much smaller than the detector thickness, the interstrip capacitance C_{is} between two adjacent strips is much greater than the junction capacitance C_j of the single strip to the backplane (figure 1). We measured the capacitance of a single strip to its neighbouring strips and to the backplane on two microstrip detectors having 200 μm pitch and 300 μm thickness. The results are presented in the following sections.

2. Samples description.

We used for the measurements two microstrip detectors manufactured by Canberra[1]. The detectors (identical) are dc-coupled and have 52 strips each, with a pitch of 200 μm. The detector thickness is 300 μm. In figure 2 one can see the geometry of one detector (seen from above) and figure 3 shows the layout of the terminal part of the strips. As can be seen, the p^+ implant width is 160 μm and the gap between neighbouring strips is 40 μm (thus giving a pitch of 200 μm, as stated above). The strip length is 10 mm.
In order to simulate the detector operation in real experimental conditions, where every strip is held at a well defined potential through an amplifier, we used the stitchbonding technique to connect together all the strips except those to be measured; in this way, both the junction capacitance of the single strip and the capacitance of one strip with respect to the others could be measured [2].

3. Junction capacitance measurements.

The circuit employed is shown in figure 4. We used a Keithley 590 CV Analyser; the measuring signal sent by the instrument output had a frequency either of 100 kHz or 1 MHz and an amplitude of 15 mV rms. Data were taken at 100 kHz, but no significant differences were observed at 1 MHz. The strip under measurement is biased keeping the

[1] Canberra Semiconductors, Belgium.

backplane at positive voltage with respect to the CV Analyser input.
When measuring low level capacitances, special attention must be paid to reduce parasitic effects. All the measurements were performed with a probe station placed inside a metallic box which acted as a Faraday's cage. The devices under test were connected to the CV Analyser with BNC coaxial cables of equal length, kept as short as possible. Moreover, a subtraction of the parasitic capacitances (i.e. cable capacitance and capacitance between the probe contacting the measured strip and all the other strips) was performed. This was done using the "open circuit correction" feature of the instrument; this consists in raising the probe needle of the central strip at a fixed height and leaving all the rest equal. The parasitic capacitance so measured is automatically taken by the instrument as the reference value ("zero") for the next measurements. The probe tip's height was large enough to avoid any accidental contact with the underlying strip but, on the other hand, small enough to correctly evaluate the parasitic capacitance of the tip with respect to the neighbouring strips.
The typical measured junction capacitance is shown in figure 5. The curve clearly shows good agreement with the well known $1/\sqrt{V}$ dependence expected for a step-graded p^+-n junction.
Using the simple parallel plate capacitor model, a junction capacitance of 0.55 pF is calculated at total depletion for strips of these dimensions. The measured value (0.75 pF at full depletion) is in very good agreement with this prediction.

4. Interstrip capacitance measurements.

The circuit we used is shown in figure 6. The stray capacitance subtraction method was the same of section 3. On the detector labelled "DET1" 51 strips were stitchbonded and one central was left out. On the other test structure ("DET2") only 1, 2, 3 and 4 strips on each side of 4 different central strips were connected together. In this way we could evaluate the contribution of the farther strips and its relative importance with respect to that of the two closest strips.
The value of the interstrip capacitance has been previously estimated by means of a simple empirical model. In this model the total interstrip capacitance is evaluated as the sum of two (parallel) capacitors, each one between the central strip and one of the nearest two. At the depletion voltage, all the bulk is depleted except the p^+ implantations, where mobile charges are still present. Therefore, each strip side can be regarded as a charged wire, with a diameter given by the implantation depth (figure 7). Thus, recalling the formula giving the capacitance

between two charged wires of length L, diameter d and separated by a distance g, the total interstrip capacitance C_{istot} at the depletion voltage is given by [3]:

$$C_{istot} = 2C_{is} = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln[\frac{g}{d} + \sqrt{(\frac{g}{d})^2 - 1}]}$$

The implantation depth d (defined as the depth at which the hole concentration equals the electron bulk concentration) was known to be 0.5 μm. Of course, this simple model only aimed at giving a rough estimation of the interstrip capacitance, to be compared with the measurements. In particular, in the model the capacitances between non neighbouring strips are neglected and the validity of this approximation had to be verified. The total interstrip capacitance calculated with this model was $C_{istot(model)} \approx 1.28$ pF, so that $C_{is(model)} \approx 0.64$ pF, i.e. virtually equal to the value of the junction capacitance, and this was not surprising given the fact that in these test structures the pitch was comparable with the detector thickness.
The results of the interstrip capacitance measurements are plotted in figure 8 versus the number of strips connected. The value given by the model is also shown for comparison. It is apparent from this plot that more than 90 % of the total interstrip capacitance is contributed by the two closest neighbours and that the contribution of the strips beyond the fourth one is completely negligible.
Moreover, the measurements show that the empirical model, though oversimplified, allows nevertheless to take into account the 80 % of the total measured interstrip capacitance, thus providing a simple formula for a fast but sufficiently accurate evaluation of this fundamental parameter.

5. Conclusions.

Junction and interstrip capacitances have been measured on test structures of dc-coupled microstrip detectors. It has been found that, for detectors with this geometry (300 μm thick, 200 μm strip pitch, 160 μm strip width and 10 mm strip length) the interstrip capacitance and the junction capacitance have practically equal values and that more than 90 % of the total interstrip capacitance (i.e. the total capacitance of one strip to all the other strips) is contributed by the two closest strips (one on each side of the measured strip). Therefore, one can conclude that

the total load capacitance (for this type of detector) presented by one strip to the readout electronics is, to a very good approximation, simply given by $C_{load} \approx 2C_{is} + C_j \approx 2.1$ pF.
Moreover, a simple empirical model to evaluate the interstrip capacitance has been developed. Its predictions are in good agreement with the experimental results.

Acknowledgements.

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References.

[1] E. Gatti and P. F. Manfredi, "Processing the signals from solid state detectors in high energy physics", Nuovo Cimento, vol. 9, 1986.

[2] S. Masciocchi et al., "Capacitance measurements on silicon microstrip detectors", Proceedings of the 1992 IEEE NSS, Orlando (USA).

[3] E. Hallen, "Electromagnetic Theory", Chapman & Hall, London, 1962, p. 53.

Figure captions.

Figure 1. Schematic representation of a microstrip detector as a capacitive network. The interstrip (C_{is}) and junction (C_j) capacitances are shown.

Figure 2. Top view of one test structure used in the measurements. The overall dimensions are 11.4 x 11.4 mm^2 and there are 52 strips at 200 μm pitch. The strip length is 10 mm.

Figure 3. Layout of the terminal part of the strips. The relevant dimensions are indicated.

Figure 4. Circuit employed for the measurements of C_j. The CV Analyser ground is in common with the bias supply ground.

Figure 5. C_j vs. bias voltage data. The value at full depletion (0.75 pF) is in substantial agreement with the value calculated using the simple parallel plate capacitor model (0.55 pF).

Figure 6. Circuit employed for the measurements of C_{is}.

Figure 7. Schematic cross section of two neighbouring strips. The most important geometric parameters are defined; g and d represent respectively the gap between the strips and the implantation depth. The strip side length L is in the direction perpendicular to the drawing. The approximation used in the text (implantation side as a thin wire) is also shown.

Figure 8. Interstrip capacitance as a function of the number of strips connected on each side of the measured strip. The value predicted by the model (which considers only the two closest neighbours, one on each side of the measured strip) is also shown.

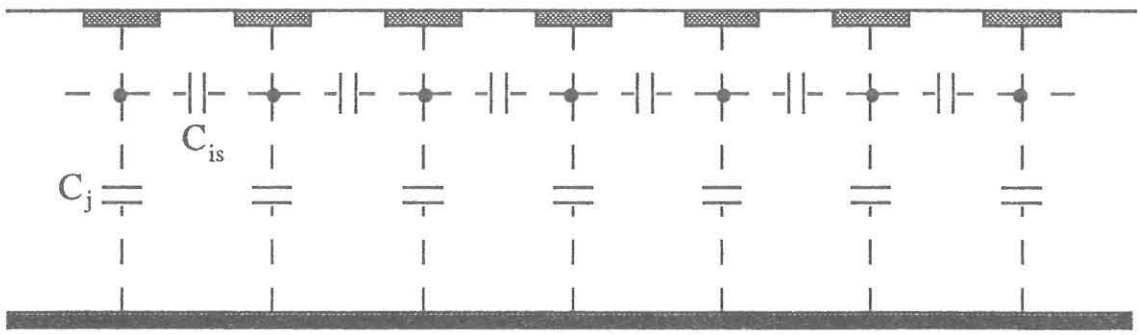

Fig. 1

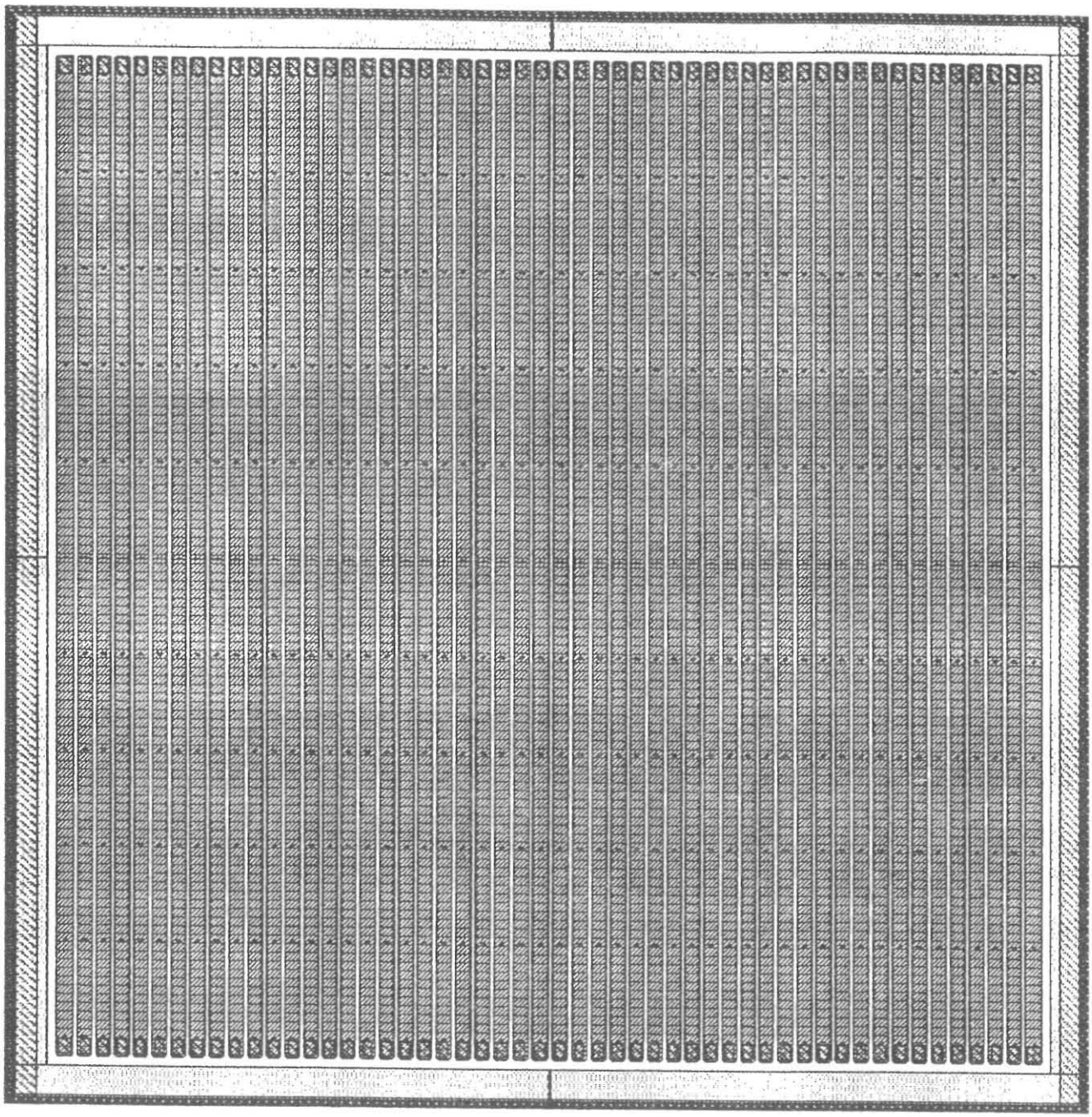

Fig. 2

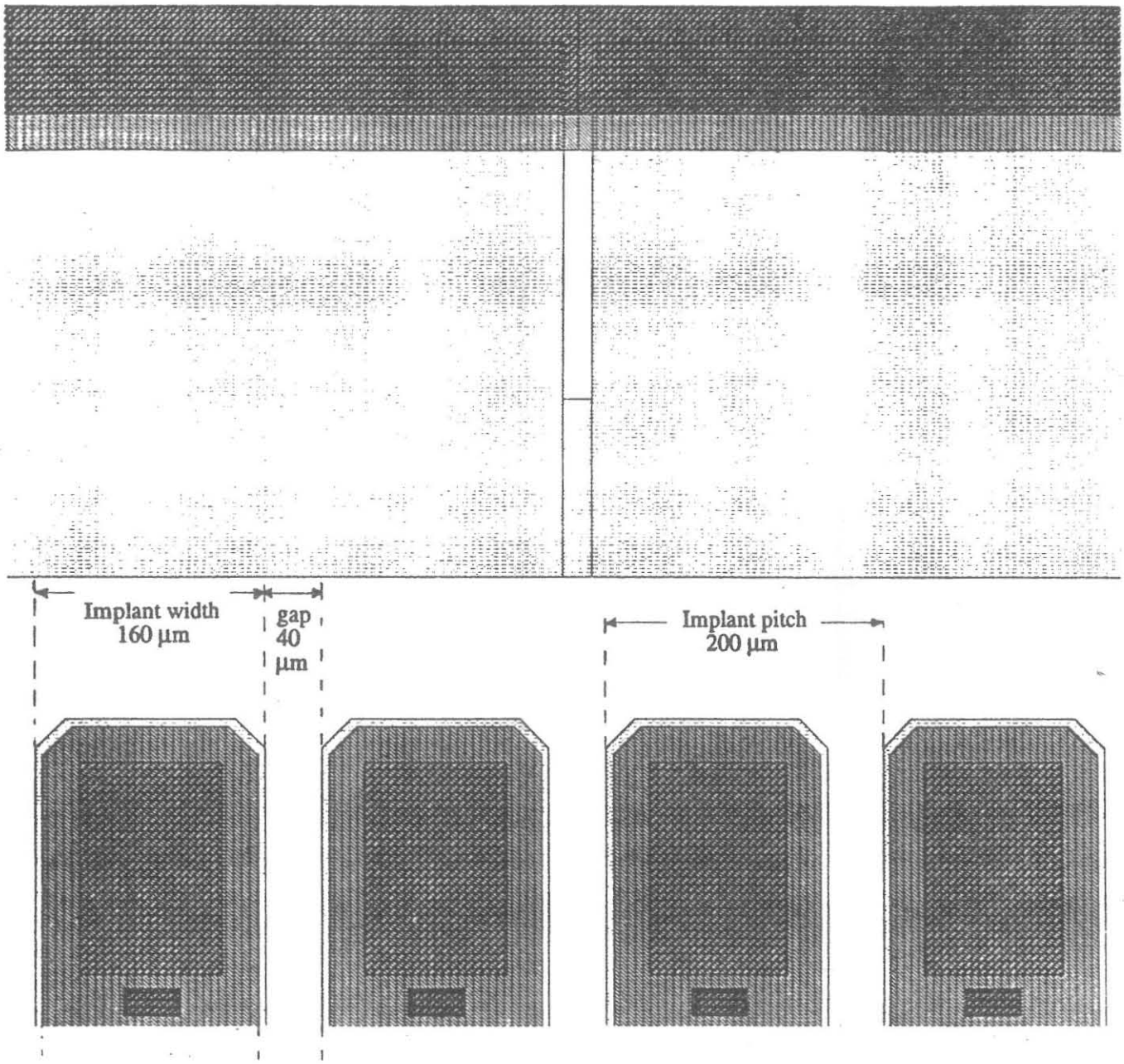

Fig. 3

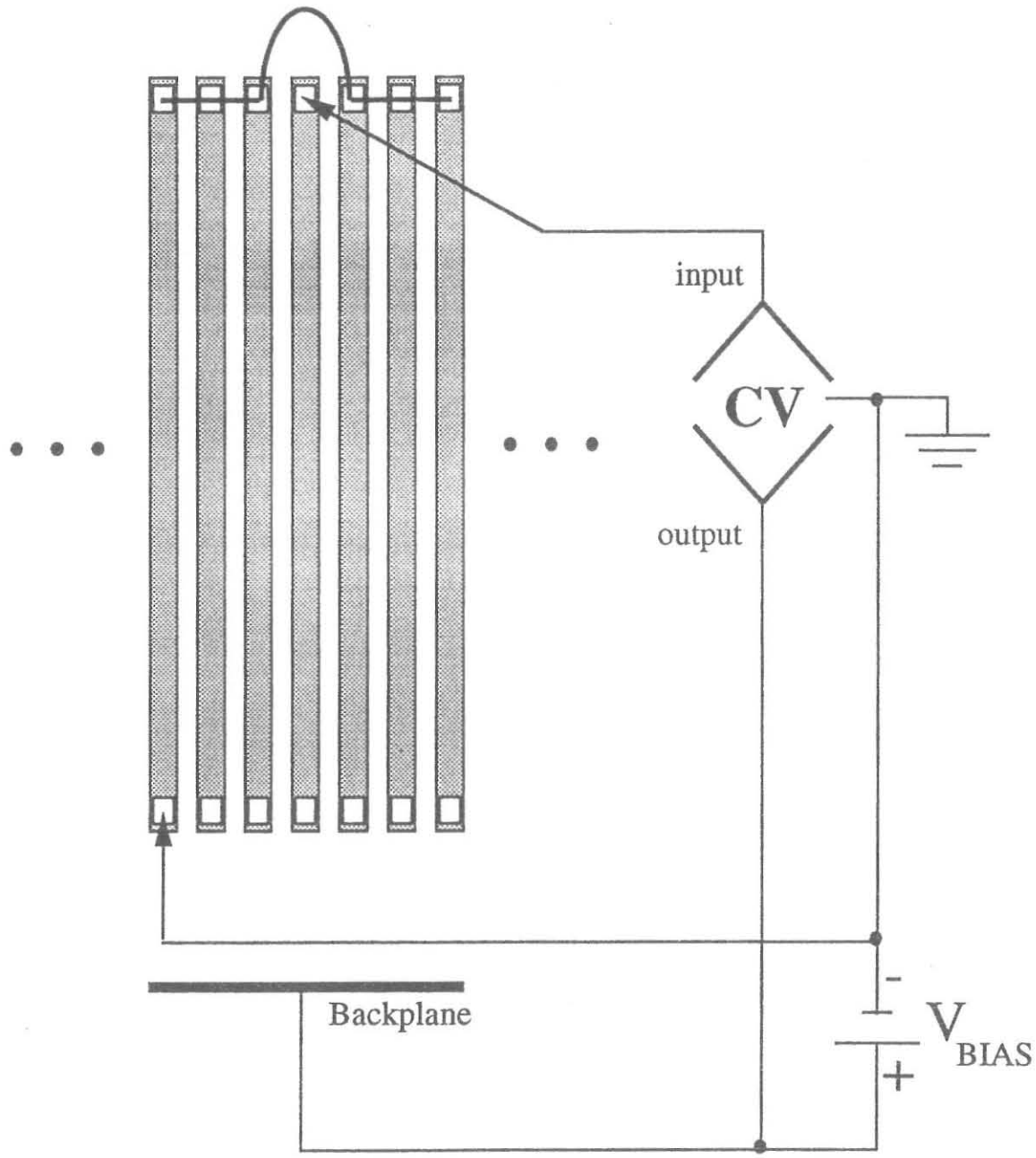

Fig. 4

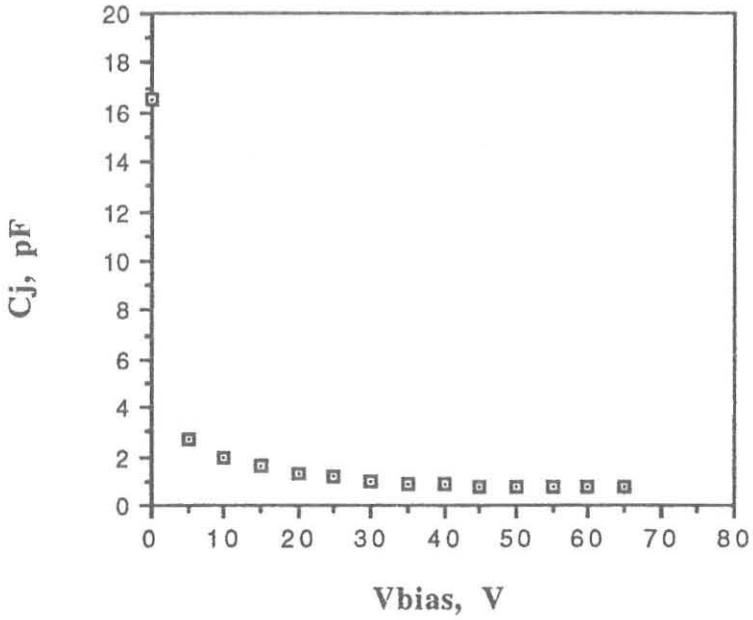

Fig. 5

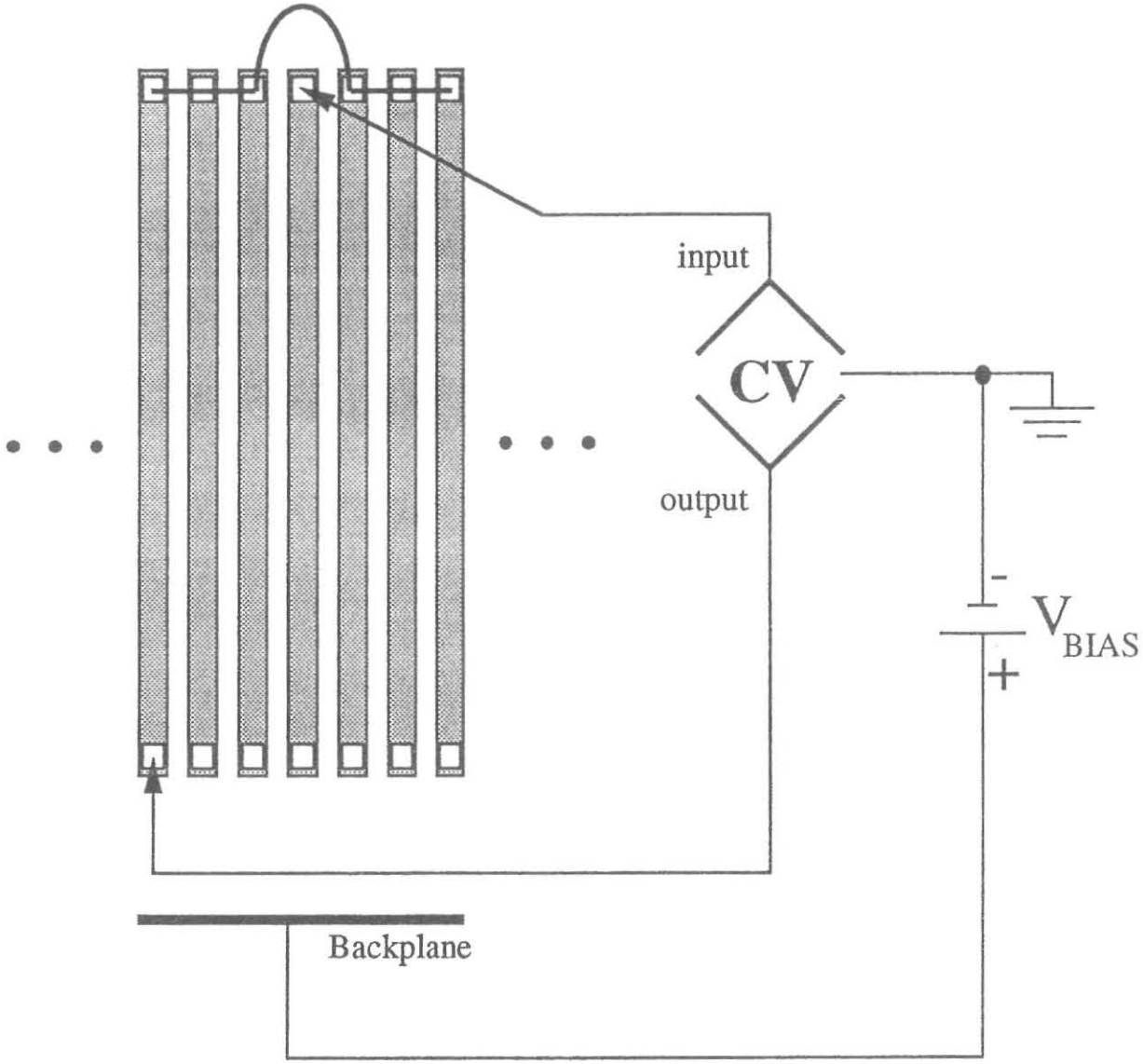

Fig. 6

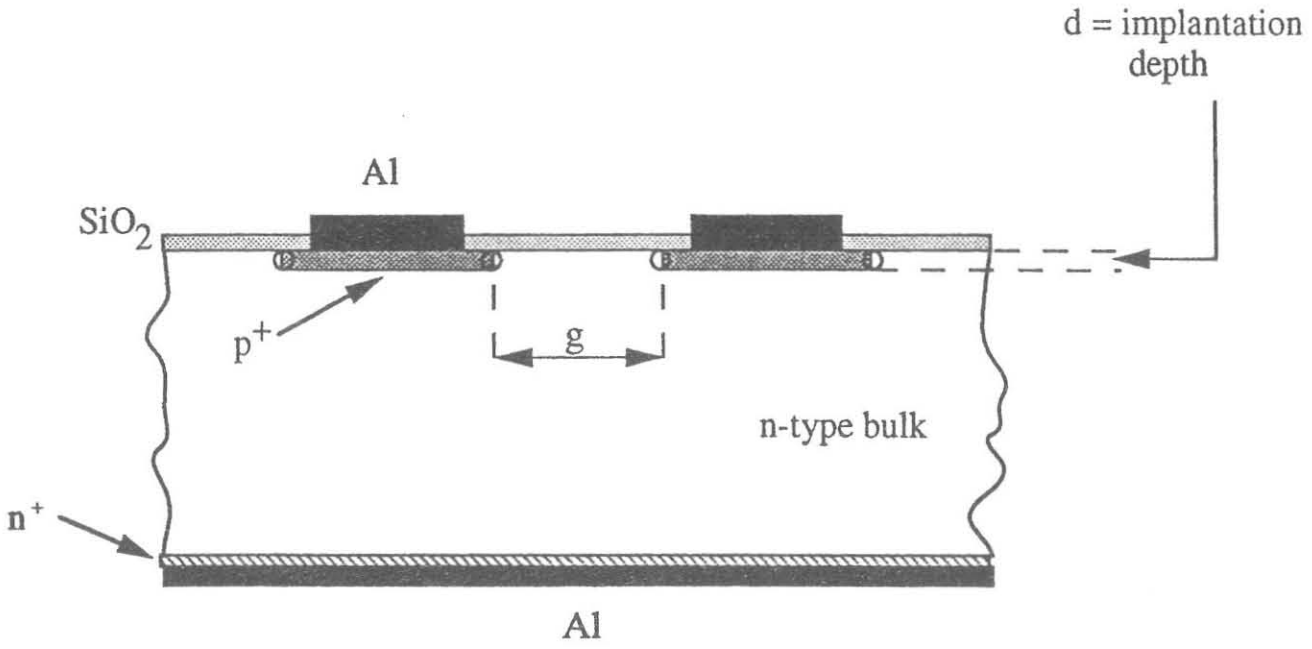

Fig. 7

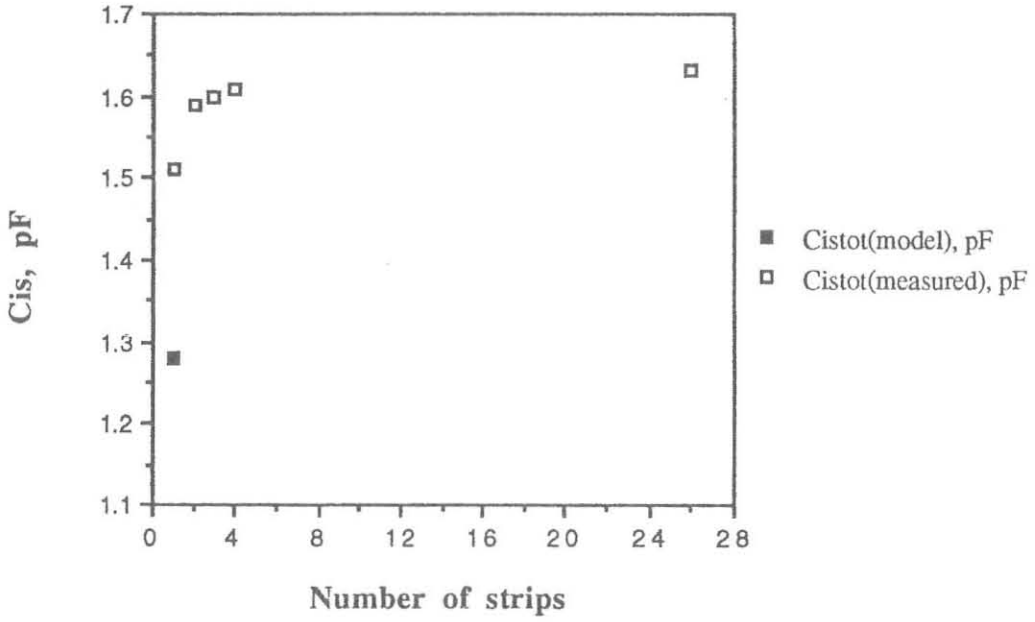
1.7
1.6
1.5
1.4
1.3
1.2
1.1
Cis, pF
0
4
8
12
16
20
24
28
Number of strips
Cistot(model), pF
Cistot(measured), pF

Fig. 8