ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Pavia

INFN/TC-91/09
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Servizio Documentazione
dei Laboratori Nazionali di Frascati

INFN - Istituto Nazionale di Fisica Nucleare
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The TRIGA board for a fast muon trigger for E771

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The muon trigger logic of experiment $E771$ at Fermilab is described, with emphasis on the design and development of the board dedicated to such a trigger. A Programmable Gate Arrays microchip has been implemented on the *TRIGA* board, to achieve a flexible kind of trigger. The use of a programmable trigger allows to optimize the signal to background ratio according to the working conditions of the muon detector.

1 Introduction

Fermilab experiment $E771$ will study heavy flavour physics[1] using the 800 GeV/c primary proton beam from the Tevatron at an intensity of up to 10^8 proton/sec, and running for five months starting in the summer of 1991 .

The primary objectives of $E771$ are the measurement of beauty total cross section, lifetimes and $B\overline{B}$ mixing by triggering on the muons generated in decays of the type $B \rightarrow J/\psi \rightarrow \mu\mu$ and $B \rightarrow \mu\nu+x$. These two physics processes can be tagged respectively by the presence of opposite sign dimuons coming from the same secondary decay vertex and by a single (or double, for the case of double semi-leptonic decay) high p_t muon.

To achieve the outlined results, it is of primary importance to use a fast trigger able not only to recognize the presence of one or more muons but also to select the muons with high transverse momentum.

The aim of the present note is to describe the $TRIGA$ board developed to perform such a first level trigger.

2 The muon detector

The $E771$ spectrometer (Fig. 1) consists of a foil target followed by a silicon microstrip vertex detector, tracking (proportional, drift and pad) chambers, an analysis magnet, scintillation counter hodoscopes, an EM calorimeter and a muon detector. The spectrometer's overall length is approximately 28 m and it has an angular acceptance for muons of ± 100 $mrad$ in the horizontal plane and ± 50 $mrad$ in the vertical plane.

The muon detector consists of three planes of Resistive Plate Counters (RPC)[2,3] embedded in thick layers of steel and concrete absorbers.

Each RPC plane is made of nine 2×1 m^2 standard modules covering a total area of 6×3 m^2. Each module is composed of two graphite electrodes separated by a 2 mm gap carrying across it a static electric field of about 40 kV/cm. The two electrodes are set on two phenolic polymer layers, 1 mm thick, with a volume resistivity of $10^{11\pm1}$ Ωcm. The 2 mm gap is filled with a mixture of argon (54 %), butane (42 %) and freon (4 %) at standard pressure flowing at $\sim$ 0.1 volumes per hour.

The signals are collected using a plane of $\sim$ 2000 copper pads, facing the high voltage electrode. The choice of a pad readout was made in order to have fast information on both the coordinates of the particle crossing the detector. The signals are then processed by an ad hoc readout system[4], which performs logic functions for triggering purposes.

3 The first level trigger

The $E771$ first level trigger is composed of two separate parts, level 1A and 1B, which operate independently and in parallel. Level 1A requires the detection of one or more muons defined as a triple coincidence among specific sets of pads belonging to the three RPC planes. The minimum energy required of a muon to penetrate the steel absorber and to produce a signal in the RPC's is 10 GeV in the central part of the detector and 6 GeV at wider angles. In contrast, the level 1B trigger[5,6] requires at least one muon with a p_t above a minimum threshold, detected as a four-fold coincidence between two pad chambers, the scintillation hodoscope and the first RPC plane. The description of level 1B trigger will be a subject of a different note.

The elementary unit for the pourpose of the level 1A trigger is the OR of four adjacent pads ($OR4$). A *superpad* is then defined as the OR of nine (3 by 3) $OR4$'s (Fig. 2). Muons are defined as the three-fold coincidence among an $OR4$ which fired in the first plane and the corresponding superpads in the projective geometry, belonging to the second and third planes.

To perform such a logic function, the $TRIGA$ board, using the Programmable Gate Arrays (PGA) Xilinx $XC2064$ microchip[7] as its main component, was designed and constructed.

Input to the $TRIGA$ board are the $OR4$ signals, coming from the RPC's readout boards, which are sent to the Xilinx chip to form superpads and triple coincidences. Each $TRIGA$ board handles 8 $OR4$'s coming from the first RPC plane, 24 from the second and 24 from the third (Fig. 3), and it generates 8 triple coincidence signals, for a total of 64 input/output lines.

Each RPC plane of 2048 pads contains 512 $OR4$ signals, which in turn correspond to 512 possible triple coincidences for the trigger. Since each $TRIGA$ board handles 8 coincidences, 64 trigger boards are needed to process all of the RPC signals. The 64 $TRIGA$ boards are located into four crates in the experimental hall.

The RPC plane has been conceptually subdivided into four horizontal bands, each one handled by a single crate (Fig. 4). In spite of the fact that the second and third

bands are smaller in surface, each band is handled by a full single crate since, due to the smaller pad size, the total number of channels in bands 2 and 3 is the same as in bands 1 and 4. With this configuration, the numerous signals of the second and third planes involved in different superpads, are distributed to different boards of the same band by means of a dedicated *BUS* on the backplane. The few signals shared between adjacent bands are transported by cables connected to the front of the crate.

The total time required for level 1A trigger to form the three-fold coincidences and to send them to the counting room is $\sim$ 390 *ns*. The additive factors contributing to this timing are listed in Tab. 1.

Table 1: Timing for level 1A trigger logic.

Cable from *RPC* pad to *RPC* readout board	20 ns
RPC readout board transition time	32 ns
Cable from *RPC* board to *TRIGA* board	90 ns
TRIGA board transition time	55 ns
Cable from *TRIGA* board to counting room	190 ns
Total time	387 ns

4 The TRIGA board

4.1 Trigger card schematic

The schematic of the trigger board is shown in Fig. 5a and b. The *OR*4 *TTL* input signals come from the *RPC* readout boards via twisted pair flat cables, which are connected to the *TRIGA* board by means of three sixteen pin connectors located in the front of the module, each connector receiving the signals from one *RPC* plane.

The connecting cables are made in three different lengths, to compensate for the time of flight of the muons between successive *RPC* planes.

From the input stage, the signals are sent to the *PGA* input pins. There are two *PGA* microchips on each card, providing the coincidences between the detector planes. The signals coming from the *PGA*'s are sent to Integrated Circuits 74*F*74 which generate

20 ns wide pulses synchronized with the beam radiofrequency (53 MHz).

The eight coincidences generated by the card, after TTL-ECL translation via the $MC10124$'s, are finally sent to the counting room by differential ECL lines.

4.2 Time spread study

Since in $E771$ the time difference between two consecutive buckets is about 20 ns, narrow coincidences need to be performed in order to recognize the bucket of the interaction. For such a reason it is very important to have low time spread between different signals.

The measured time spread due to the RPC readout board and to the PGA is shown in Fig. 6. There are however, additional contributions that affect the total time spread of the $TRIGA$ output. A list of the different jitters is given in Tab. 2.

Table 2: Contributions to the time spread

Different impact point on large pads	0.42	ns
Different impact point on the RPC wall	0.67	ns
Cable length uncertainty	1.25	ns
Time uncertainty within a bucket	3	ns
Different signal paths inside the readout board	1.5	ns
Different signal paths inside the $XC2064$ chip	5	ns

In order to reduce the total spread, the output lines have been synchronized using the beam radio frequency as a clock for the shapers located on the board.

There is another potential source of time spread, not listed in the previous table, which is due to the RPC HV. Usually the RPC modules work at different HV to reach the best efficiency. This implies a relative delay of about 1 ns every 100 $Volts$ of difference in the HV. It is possible to avoid this kind of jitter, working with all the RPC modules set at the same HV and adjusting the readout board threshold independently for each board.

5 Programmable Gate Array

The main component of the *TRIGA* board is the *CMOS XC*2064 microchip, a Programmable Gate Array manufactured by Xilinx, used to form superpads and triple coincidences. The most relevant feature of the *PGA* is its fully programmable architecture.

The general structure of the *XC*2064 is shown in Fig. 7. It is divided into three basic elements: input/output blocks, logic blocks and interconnections.

The I/O blocks connect the internal logic to the external package pin; they can be programmed either as input lines or as output buffers compatible with either *TTL* or *CMOS* levels.

Each logic block can perform any logic function of four variables or any two functions of three variables. The set of logic blocks is arranged in a matrix at the center of the device.

Programmable interconnections provide the paths to connect all the elements inside the chip.

Technical features of *XC*2064 are listed in Tab. 3.

Table 3: Technical features of the XC2064

Number of gates	1200	
Number of logic blocks	64	
Number of logic functions	128	
I/O lines	58	
RAM Memory	12	kbit
Clock Frequency	70	MHz

The 1A trigger logic exploits only partially the *PGA* resources. In fact, only 40 out of a total of 58 I/O pins, and 28 out of a total of 64 logic blocks have been used. The required time to perform the coincidence is about 55 *ns*.

In order to perform the required logic functions, the *PGA* needs to be programmed by a specific software package previously installed on a personal computer. The *PGA* program is downloaded on a Programmable Read Only Memory (*PROM*) and it can

be transferred on the PGA Random Access Memory (RAM) at power up in different ways. For our application, we chose the Serial Master Configuration, where the PGA is the active device which interrogates the $PROM$ and reads the data.

5.1 XC2064 Programming

The $DASH$ Graphic Editor[8] by Future Net, and $XACT$ Design Editor[9] by Xilinx have been used for the configuration of the logic functions by means of a macro symbol's library, including more than 100 logic elements. This package has been expanded by an optional TTL library that adds over 50 graphic symbols.

The Xilinx trigger logic, designed with $DASH$, and loaded on a PGA is shown in Fig. 8. Signals $B11$ to $B63$ and $C11$ to $C63$ coming from the second and third RPC plane respectively, form the superpads. The coincidences are made by $ANDing$ the superpads with the signals coming from the first plane ($A22$ to $A52$ on the drawing). As an example, the boolean equations that define the superpads and one of the coincidences are:

$$ORB22 = (B11 + B12 + B13) + (B21 + B22 + B23) + (B31 + B32 + B33)$$

$$ORC22 = (C11 + C12 + C13) + (C21 + C22 + C23) + (C31 + C32 + C33)$$

$$BP1 = ORB22 * ORC22 * A22$$

A chain of programs, operating on the schematic, checks interconnections, logic symbols, pin names and generates a file used by the $XACT$ Editor.

The Automatic Placement and Routing (APR) program optimizes the block placement and traces the interconnections as shown in Fig. 9. An editor included in the package has been used extensively to check the delay between different paths and to change some traces and blocks in order to equalize such delays. It is important to remark that the time delay, computed by the program for a trace, has to be thought as a maximum delay for that trace.

A logic simulator, $SILOS$, has been used to verify the timing via software, before loading the trigger program in the chip.

Two other programs, $MAKEBITS$ and $MAKEPROM$, finally convert the schematic into a bit file useful to be loaded in the $PROM$.

6 A programmable trigger

The achievement of a flexible kind of trigger is the most striking advantage of the use of a programmable gate array microchip as a basic component of the trigger card. According to the experimenters needs, the chip can be reprogrammed, and the resulting trigger logic can consequently be optimized to the performance and working conditions of the detector.

The requirement of a triple coincidence among the three *RPC* planes to recognize a muon implies that the overall efficiencies for single and dimuon trigger are η^3 and η^6 respectively , where η is the efficiency of a single *RPC* module. If η was to fall below 95% the choice of the triple coincidence, made to minimize the background, would imply a very low overall trigger efficiency. For instance, if $\eta = 95\%$, the single and dimuon trigger efficiencies are 85.7% and 73.5% respectively.

In order to recognize a muon, an alternative is to require a hit from the first *RPC* plane, and a second hit from either the second or the third plane. This requirement is looser than the previous one, and can be implemented only if the background level is tolerable. This last condition is not easily predictable for a very high intensity proton beam, and has to be verified on the floor, at the beginning of the run. The choice of a 2 out of 3 *RPC* coincidence presents, with respect to the 3 out of 3, the advantage of a higher trigger efficiency. Assuming $\eta = 95\%$ as before, the single and dimuon trigger efficiencies result to be respectively 94.8% and 89.9% for the 2 out of 3 choice. These last results have been obtained evaluating the probability for a combined inefficiency of the second and third *RPC* planes.

During the run, if needed, it will be possible to select the trigger configuration according to the measured background level. Only the use of a programmable trigger allows such an alternative, requiring just the downloading of a different program in the *PROM*.

7 Acknowledgements

We gratefully acknowledge the skill of O. Barnaba' and E. Imbres for their helpful and original contribution in assembling and testing the electronics. We would like to thank S. Bricola, E. D'Uscio, A. Freddi, T. Locatelli and A. Vicini of the mechanical shop of the INFN Sezione di Pavia and G. Fiore of the INFN Sezione of Lecce for helping in the installation of the system at Fermilab. We also thank Prof. S. Conetti for useful discussions.

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[3] R. Cardarelli *et al.*, Nucl. Instr. and Meth. A263 (1988) 20.

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[5] W. Selove, "A high rate trigger system for E771", University of Pennsylvania Report UPR-0147E, 1987.

[6] W. Selove, "Steps toward high-rate fixed-target B physics", University of Pennsylvania Report UPR-161E, 1988.

[7] Programmable Gate Arrays, A.M.D., 1989/1990 Data Book.

[8] *DASH* schematic designer, Future Net, 1987.

[9] *XACT* reference manual, Xilinx, 1989.

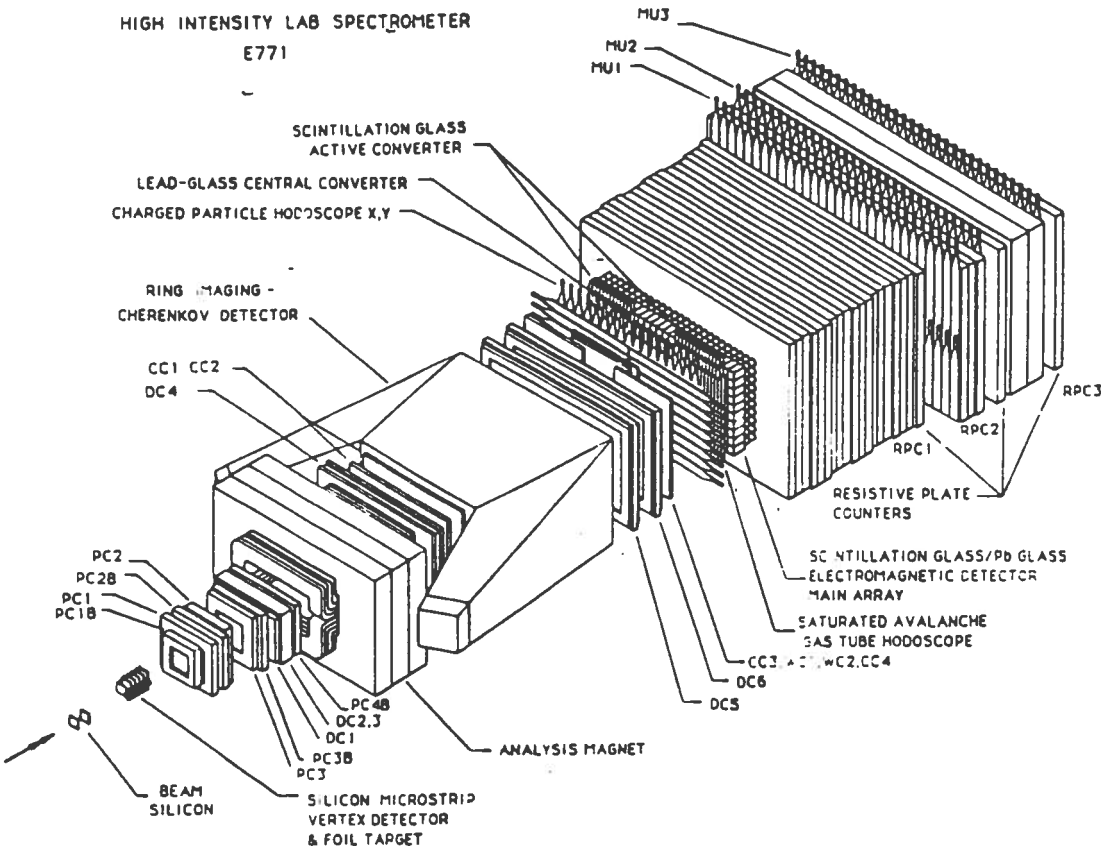


Figure 1: $E771$ spectrometer.

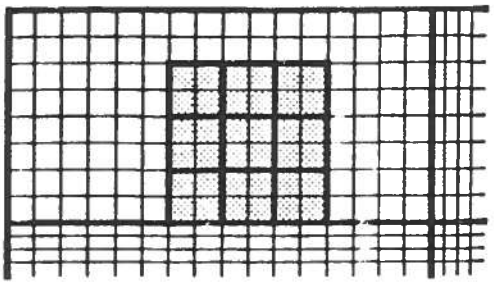


Figure 2: Superpad structure.

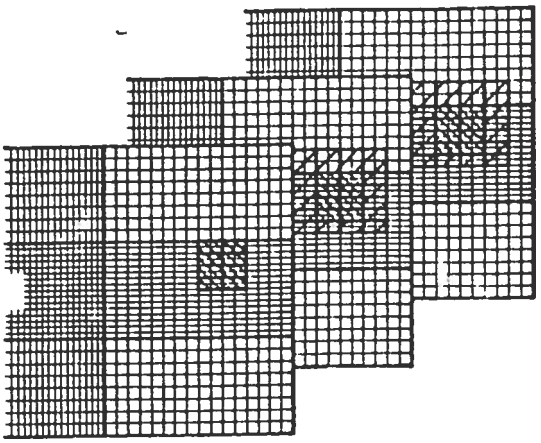


Figure 3: Coincidences handled by a single *TRIGA* board.

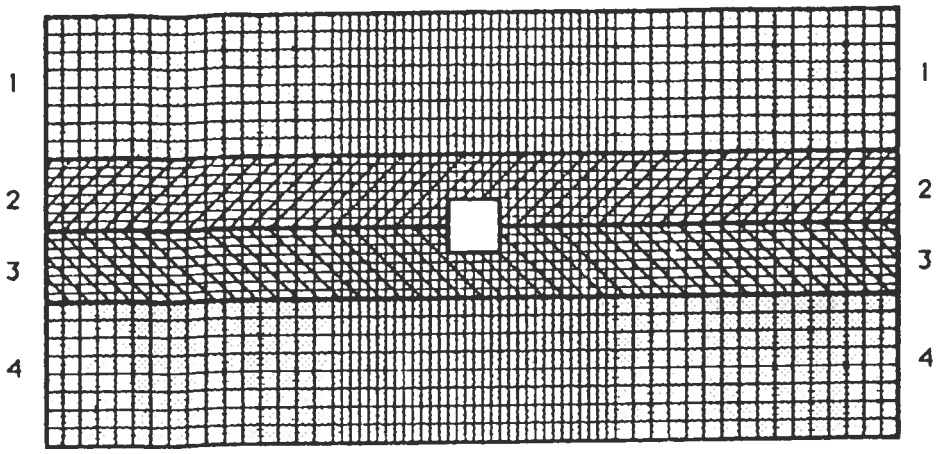
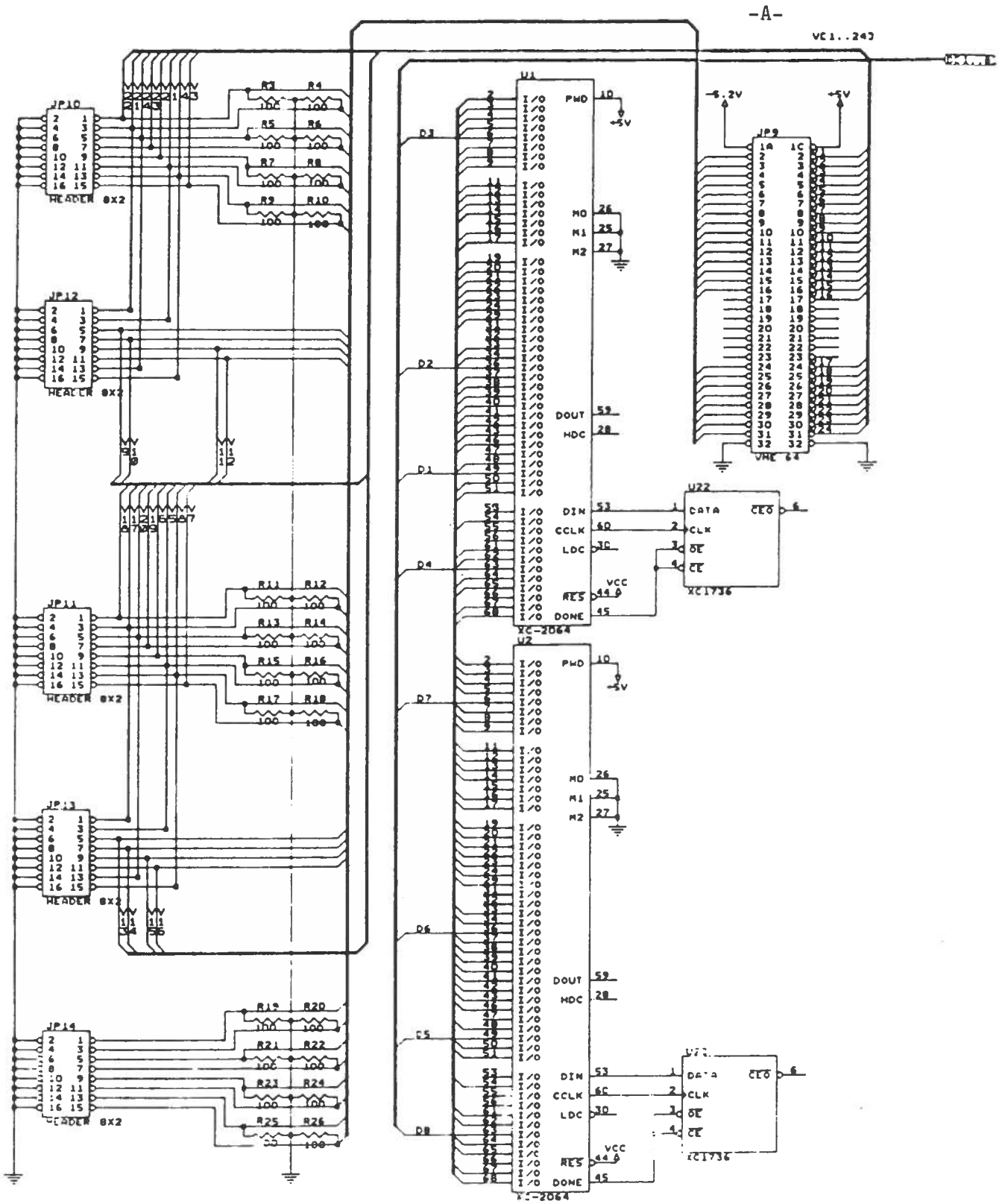
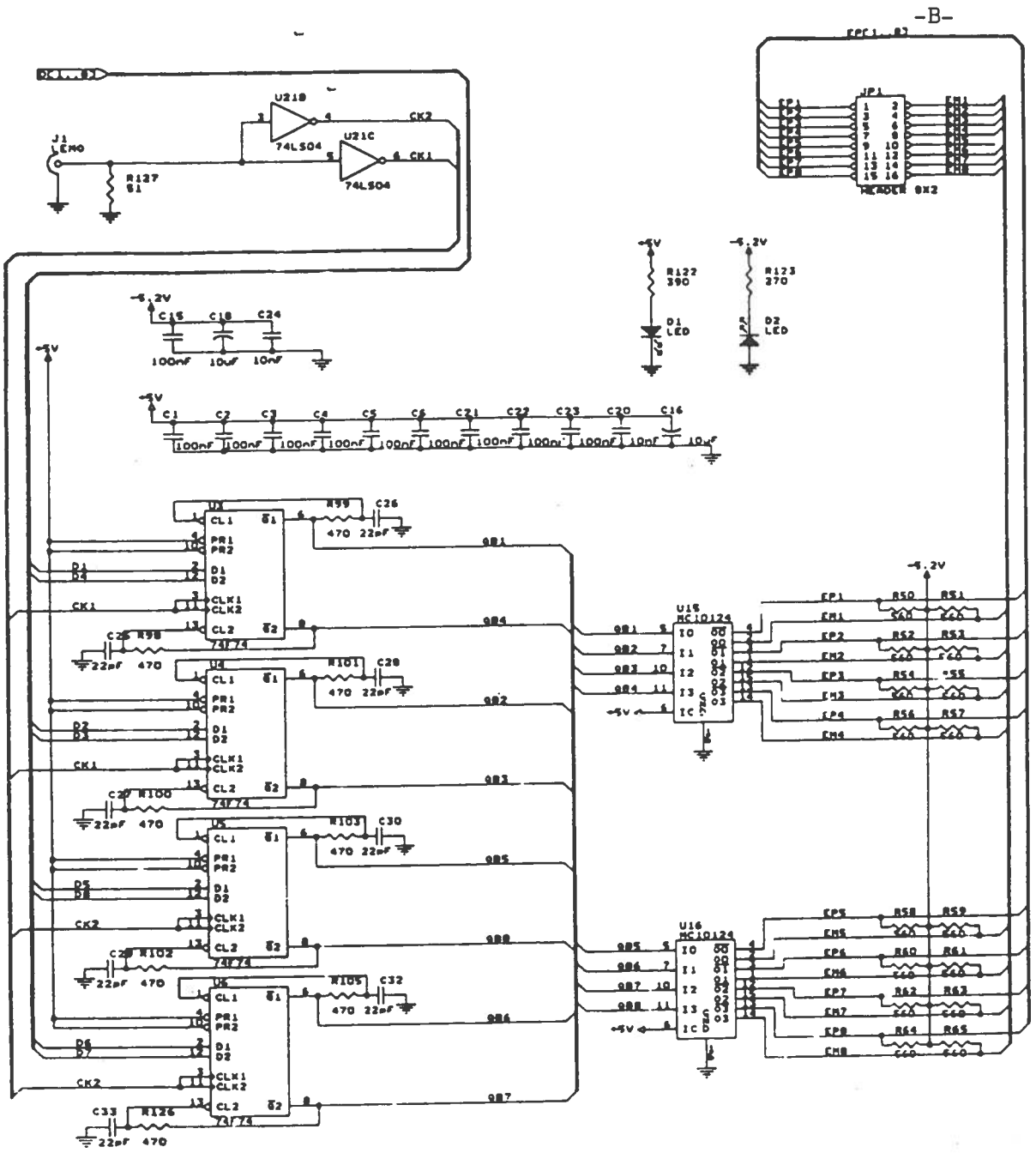


Figure 4: *RPC* horizontal bands.


-A-
VCC..243
-5.2V
+5V
JP10
JP11
JP12
JP13
JP14
HEADER 8X2
JP9
VME 64
U1
U2
XC-2064
U22
XC1736
PWD
MO
M1
M2
DOUT
HDC
DIN
CCLK
LDC
RES
DONE
DATA
CLK
CEO
OE
RESET
VCC
D1
D2
D3
D4
D5
D6
D7
D8



Figures 5a and 5b: *TRIGA* board schematic.

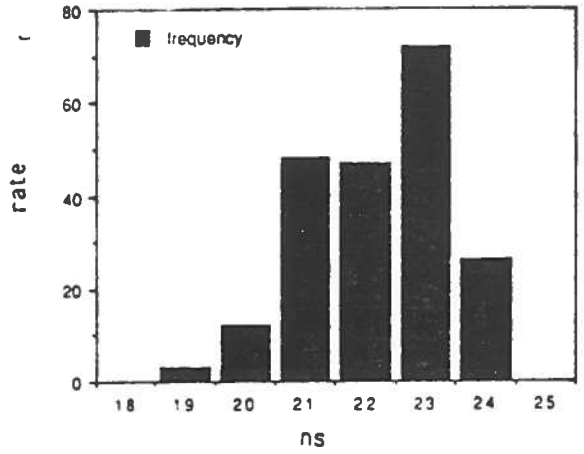


Figure 6: Measured time spread.

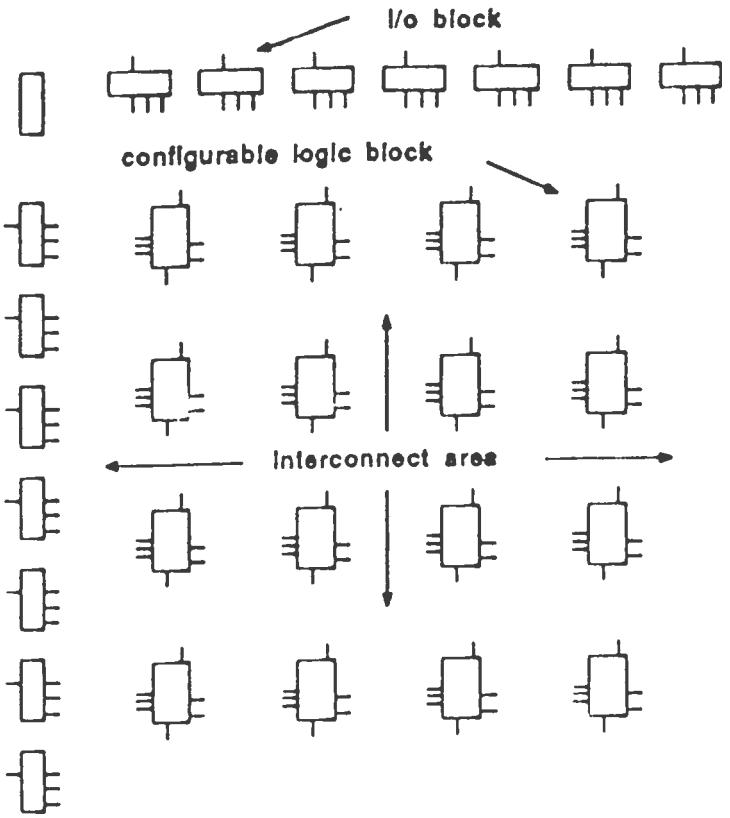


Figure 7: Structure of the $XC2064$ microchip.

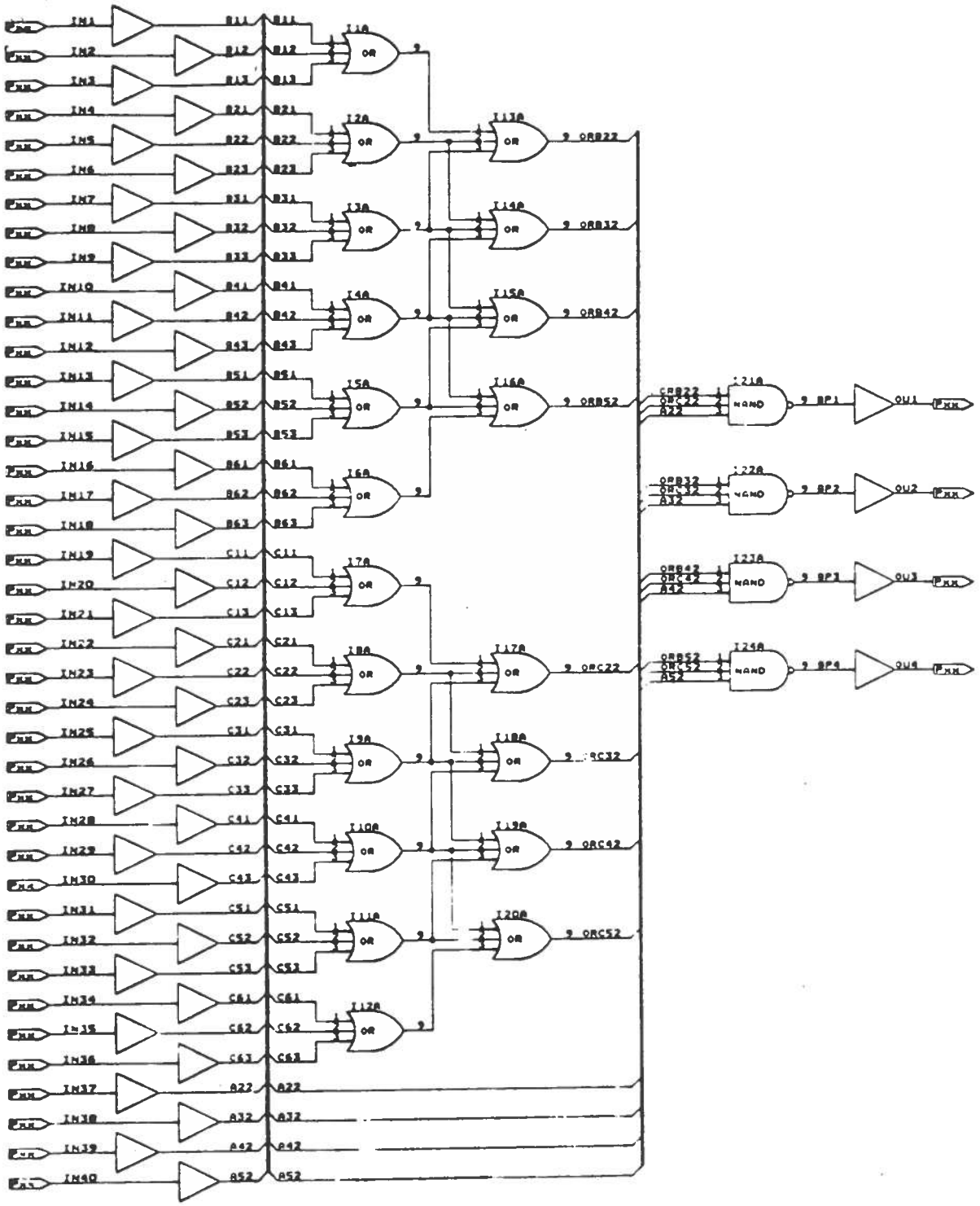


Figure 8: Trigger logic.

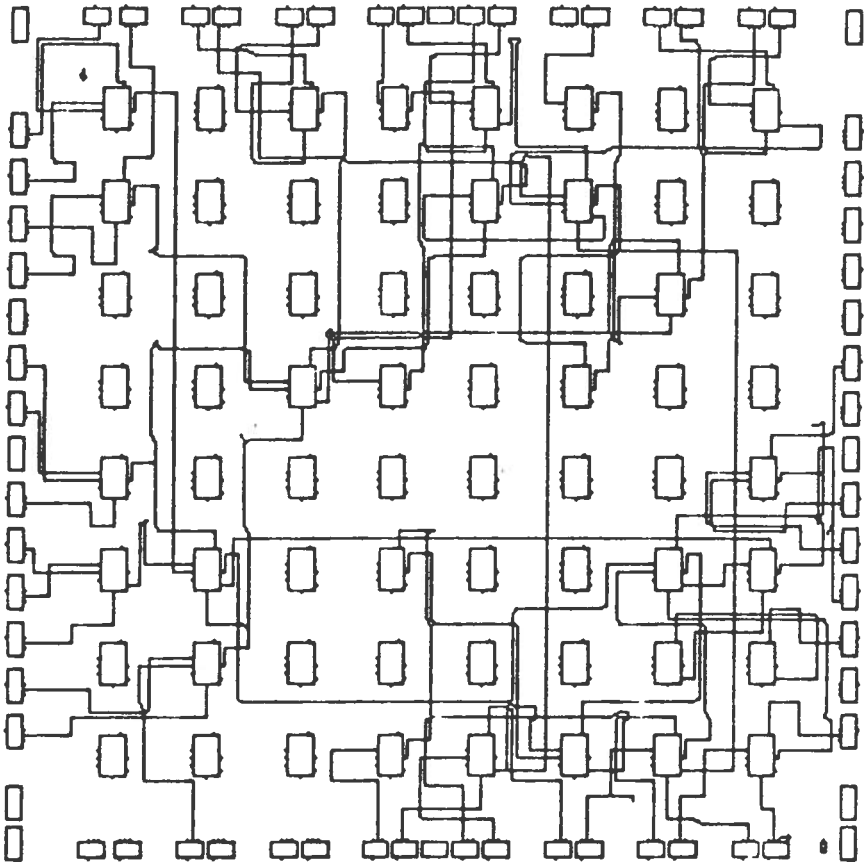


Figure 9: Blocks and traces used by the *PGA*.