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A FASTBUS MONITOR SYSTEM FOR THE DIGITAL STREAMER TUBES ELECTRONICS IN SLD

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ABSTRACT

The aim of this note is to describe the features of a fastbus module called wic read-back module (WRBM) that is going to be used as front-end electronics monitor system in the SLD limited streamer tube warm iron calorimeter and muon identifier. The wrbm is a module which will read-back and monitor some parameters and values downloaded by the Timing and Control Module (TCM) in the WIC/Strip Controllers (Splitter Boards).

1.INTRODUCTION

The digital front end electronics of the Warm Iron Calorimeter (WIC) in the SLD detector consist of approximately 90.000 digital strip redaut channels (one channel per strip). Signals from the strips are preamplified, discriminated, and digitally stored in a

custom electronics manufactured by SGS.

A controller board called Splitter Board provides the front-end SGS boards with power and threshold voltages. The Splitter Board contains also a programmable logic capable to perform a fast trigger using some special signals caming from the front-end. Each Splitter Board can handle up to ten planes of the apparatus. Control functions are also performed by this board, these include the sequence in which the planes of the apparatus are read-out, and the generation of some the control signal needed by the front-end electronics. 42 boards are needed for the whole system. The timing and the control for the Splitter Board operations are generated by a FASTBUS module called Timing and Control Module (TCM) which is synchronized with the 119 MHz LINAC main frequency.

Communications between the TCM and the Splitter Boards are performed using a serial 3 wire protocol (command, data, clock). For a detailed description of the Digital Data Acquisition of the SLD/WIC see Ref [1].

The need to monitor what has been downloaded by the TCM in the Splitter Boards led us to design a special Fastbus module (WIC Read Back Module). This module not only performs a read-back of the parameters downloaded in the controllers, but it is also useful to monitor the power supplies voltages, check there are no problem concerning coupling and verify that the TCM is sending the right sequence of command to the front-end electronics. These functions are very helpful especially in the delicate phase of the commissioning of the electronics.

The main functions that the WRBM performs are the following:

1. Read discriminator thresholds from the front-end SGS boards (almost 400 for the whole system).
2. Read SB's local trigger configuration.
3. Read SB's readout configurations (how many SGS boards per plane, and which planes participate in the data read-out).
4. Read SB's power supply voltages.
5. Check SB's control-cable connections and controllers.
6. Monitor the TCM command and data lines in order to check that the command sent is the right one.

2. SYSTEM ARCHITECTURE AND MODULE DESCRIPTION

The WRBM receives from its aux card the 4 sets of 3-wire-protocol (command, data and clock) cable coming from the TCM front panel connector. Onto its aux card, called WRBAUX, there are differential ECL to TTL line receivers and twelve programmable delays (one for each signal 0CM,0DT,0CK...3CM,3DT,3CK)to sincronize the data read-back. The WRBM is linked to SBs through intermediate boards called Fiber Optic Fan

Out (FOFO) (8 boards are needed for the whole system). The link has been realized using 16 fiber optic (8 are for redundancy)62.5/125μm multimode cables.

Each FOFO takes care up to 8 SB. It receives information in differential TTL, (EIA RS 422), converts, multiplex and sends it onto a fiber optic link to the Read Back module (see Fig.1).

Four different read-back input channels have been implemented in the module. Each channel takes care of two out of 8 subsystems. These channels are fully independent and could be individually enabled /disabled to the read-back operation by the FASTBUS. Each channel has 8K x 4 bit memory organized in 8 static Ram 1024 x 4 CY2148 by Cypress Semiconductor. It can be accessed by the FASTBUS after the operations have been completed in that channel.

The read-back operation is under the complete TCM control and it starts with the Start of the Read-Back command. This command and all the following will be ignored if the channels have not been previously enabled from the FASTBUS. The serial stream of input data in each bank of memory and the way FASTBUS accesses this memory are described in Fig.2.

The TCM End of Read-Back command generates a Service Request (if enabled from FASTBUS)to notify that the read-out is complete. Four different SR's(one for each channel)have been implemented in the standard CSR 20. The End of Read-Back command also disables the channel itself, preventing that a subsequent Start of Read-Back command restarts the process before the FASTBUS had got the chance to read the memory. The End of Read-Back will produce none of the upper actions if a valid Start of Read-Back command has not been previously received.

Fig.3 shows a block diagram with the functional blocks and their main connections. On the up left side is shown the link via AUX card with the TCM. The optic links block is the input caming from the detector. A description of the CSR's and the data memory is given in the following pages.

The FASTBUS interface has been implemented using two ADI (Fujitsu MB114F307 chips) the two chips will perform slightly different functions: for instance only the ADI low chip takes care of class N Broadcast detection, and compares the five GA lines with the corresponding AD lines to perform the Geografical Address check.

The module is a FASTBUS slave (ID=001F) and can be primary addressed in two modes:Geographical and Broadcast(case 1,2 and 5). The four banks of memory are mapped in Data Space and can be written and read from FASTBUS by block transfer and random data. Only after the Read-Back operation has been completed in that channel, the FASTBUS can access that particular bank of memory (also if the other channels are still running). SS error code 1 will be returned if the upper condition is not met.

3.TIMING AND CONTROL MODULE COMMANDS

The WRBM can execute the following TCM commands:

1. Start of Read-Back (opcode 01)
2. Data Loop-Back (opcode 11)
3. Read SB Planes Configuration (opcode 19)
4. Read SB Trigger Configuration (opcode 1B)
5. Read Thresholds and Power Supply Voltages (opcode 1D)
6. End of Read-Back (opcode 02)

All the upper commands with the exception of 1 and 6 are also interpreted by the Splitter Boards.

3.1 Start of Read-Back (opcode 01)

Command	—	——
Data	00001	

This command will be decoded by one WRBM channel if that particular channel has been previously enabled (setting the corresponding Enable channel bit in CSR 0). When this command is sent to one of the four sets of 3-wire cables, it activates that particular channel to the Read-Back operation and it sets also one bit (Rdbk Running) in the CSR 0 register. This bit will be cleared by the End of Read-Back command.

The four channels could be activated at the same time and data could be read-back in parallel from the four subsystems.

The command also clear the memory address counter register (CSR's 14÷17) relative to the channel.

It must be the first one that the TCM sends to the WRBM in order to start the operations, otherwise all the subsequent commands will be ignored.

It will be not decoded by the SB's.

3.2 Data Loop-Back (opcode 11)

Command	—	————————
Data	10001	$D_n, D_{n-1}, \ldots D_0$
Read-Back		$D_n, D_{n-1}, \ldots D_0$

This command puts the WRBM in Loop-Back mode. Bits $D_n, \ldots D_0$ following the command are sent by the TCM through its Data line to the selected SB, and from there back on the Read-Back line into the WRBM memory, closing the loop. This command should allow a simple test of SB controllers A and B and overall of control cable connections.

3.3 Read Planes Configuration (opcode 19)

Command —

Data 11001

Read-Back DT0 DT1 ... DT9

This command executes the read-back of a SB plane configuration.

10 (DT0...DT9)x8 bits are serially sent back and stored in memory.

Each set of 8 bit describes the configuration of one plane. The first 4 bits provide the plane number and the 4 less significant bits show how many SGS cards have been installed in that plane.

3.4 Read Trigger Configuration (opcode 1B)

Command —

Data 11011

Read-Back DT0 DT1 ... DT3

The first level trigger is done locally on the SB by requiring a majority of digital-or's from the planes serviced by the SB. This command reads-back 4(DT0 ...DT3)x8 bits of trigger configuration.

10 bits provide the plane selection, 10 the plane request, and 4 the majority logic and 8 bits are control flags.

3.5 Read Thresholds and Power Supply Voltages (opcode 1D)

Command —

Data 11101

Read-Back DT0 DT1 ... DT14

This command performs the read-out of 10 plane thresholds and of SB power supply voltages. 15 (DT0...DT14) 12 bits data stored in memory.

3.6 End of Read-Back (opcode 02)

Command —

Data 00010

This command indicates that the Read-Back operations has been completed. It should be the last command that the TCM sends to the WRBM. All the commands after it will be ignored. It performes a clear of the Read-Back Running bit in the CSR 0 register indicating to the FASTBUS that the Read-Back has now been completed.

This command will also produce a Service Request (if enabled) to FASTBUS setting a bit in the CSR 20.

The channel also will be automatically disabled after the reception of this command. It will not be decoded if a Start of Read-Back has not been previously received. It will not be decoded by the SB's.

4. CSR REGISTERS

- CSR 0 Module ID and various user control bits.
- CSR 7 Broadcast Class register.
- CSR 14÷17 Address Counter register.
- CSR 20 Service Request register.

The individual bits for the CSR registers are described below.

4.1 CSR 0

The assignment of bits in CSR 0 shall be as shown in the following table with the functions of the various bits as near written to each of them.

Bit	Write	Read
00	Set Error	Error
02	Run Test	Test Running
04	Enable SR	SR Enabled
05	not used	SR Set
06	Run Rdbk[0]	Rdbk[0]Running
07	Run Rdbk[1]	Rdbk[1]Running
08	Run Rdbk[2]	Rdbk[2]Running
09	Run Rdbk[3]	Rdbk[3]Running
10	Enable Chan[0]	Chan[0]Enabled
11	Enable Chan[1]	Chan[1]Enabled
12	Enable Chan[2]	Chan[2]Enabled
13	Enable Chan[3]	Chan[3]Enabled
16	Clear Error	ID
17	not used	ID
18	Halt Test	ID
19	not used	ID
20	Disable SR	ID
21	not used	ID
22	Halt Rdbk[0]	ID
23	Halt Rdbk[1]	ID

24	Halt Rdbk[2]	ID
25	Halt Rdbk[3]	ID
26	Disable Chan[0]	ID
27	Disable Chan[1]	ID
28	Disable Chan[2]	ID
29	Disable Chan[3]	ID
30	Reset	ID
31	not used	ID

4.2 CSR 7

This 16 bit register is used to specify the Broadcast classes to which the WRBM will respond. As told before this slave module can response to Broadcast operations, according case 1,2 and 5 through the bits field AD 07÷02.

4.3 CSR's 14÷17 (hex)

CSR's 14÷17 are four read/write 16-bit registers used to store the memory address counter. Each of them has been developed using two 74ALS867 in cascading configuration, in order to provide the total nibbles of valid data that have been respectively read-back by each channel.

4.4 CSR 20 (hex)

CSR 20 is the standard Service Request Register. It has been realized by eight 74LS112 and few gates in order to provide four different service requests according to the following table:

Bit	Write	Read
00	Enable SR[0]	SR[0]Enabled
01	Set SR[0]	SR[0]Set
02	Enable SR[1]	SR[1]Enabled
03	Set SR[1]	SR[1]Set
04	Enable SR[2]	SR[2]Enabled
05	Set SR[2]	SR[2]Set
06	Enable SR[3]	SR[3]Enabled
07	Set SR[3]	SR[3]Set
16	Disable SR[0]	not used
17	Clear[0]SR	not used
18	Disable SR[1]	not used
19	Clear[1]SR	not used
20	Disable SR[2]	not used

21	Clear[2]SR	not used
22	Disable SR[3]	not used
23	Clear[3]SR	not used

5. DATA SPACE

As said before, each of four channels contains data caming from two subsystem. Each memory channel could be written, from the TCM if has been previously enabled from FASTBUS setting bits 10,11,12 and 13 in CSR 0. It could be access from FASTBUS just after the end of read-back command has been sent from the TCM.

Data caming from the TCM (command, data) and read-back data caming from splitter boards through fan-out boards, are sampled and written in each bank of memory at the rising edge of TCM clock. If the fastbus will try to access the memory at that time a SS=1 will be received.

FASTBUS however can access a bank of memory that has not been yet locked from TCM or it must wait until the TCM has finished its task.

The memory consist of four banks of 8 static Ram 1024x4 mapped in the following way:

0	→3FFh	(Hex FASTBUS Address)	Channel 0
400h	→7FFh	(Hex FASTBUS Address)	Channel 1
800h	→BFFh	(Hex FASTBUS Address)	Channel 2
C00h	→FFFh	(Hex FASTBUS Address)	Channel 3

6. CONCLUSIONS

In this note the protocol of speech between the WRBM and the TCM in the WIC's frame has been described together with the splitter board main functiones that are going to be read and check from our module.

A WRBM's functional description, according to the FASTBUS point of view has been described too, in order to get a clear module view.

REFERENCES

[1] The digital data acquisition chain and the cosmic ray trigger system for the SLD warm iron calorimeter.

A.Benvenuti et al., Nucl.Instr. and Meth.A289(1990)577-583

[2] IEEE Standard Fastbus modular High-speed data acquisition and control system ANSI/IEEE Std 960-1986.

[3] Fastbus TCM, SLAC internal communications.

[4] Splitter board for streamer tube readout at the SLD.
N.Bacchetta et al., IEEE Trans.on Nucl.Sci.36:1657,1989

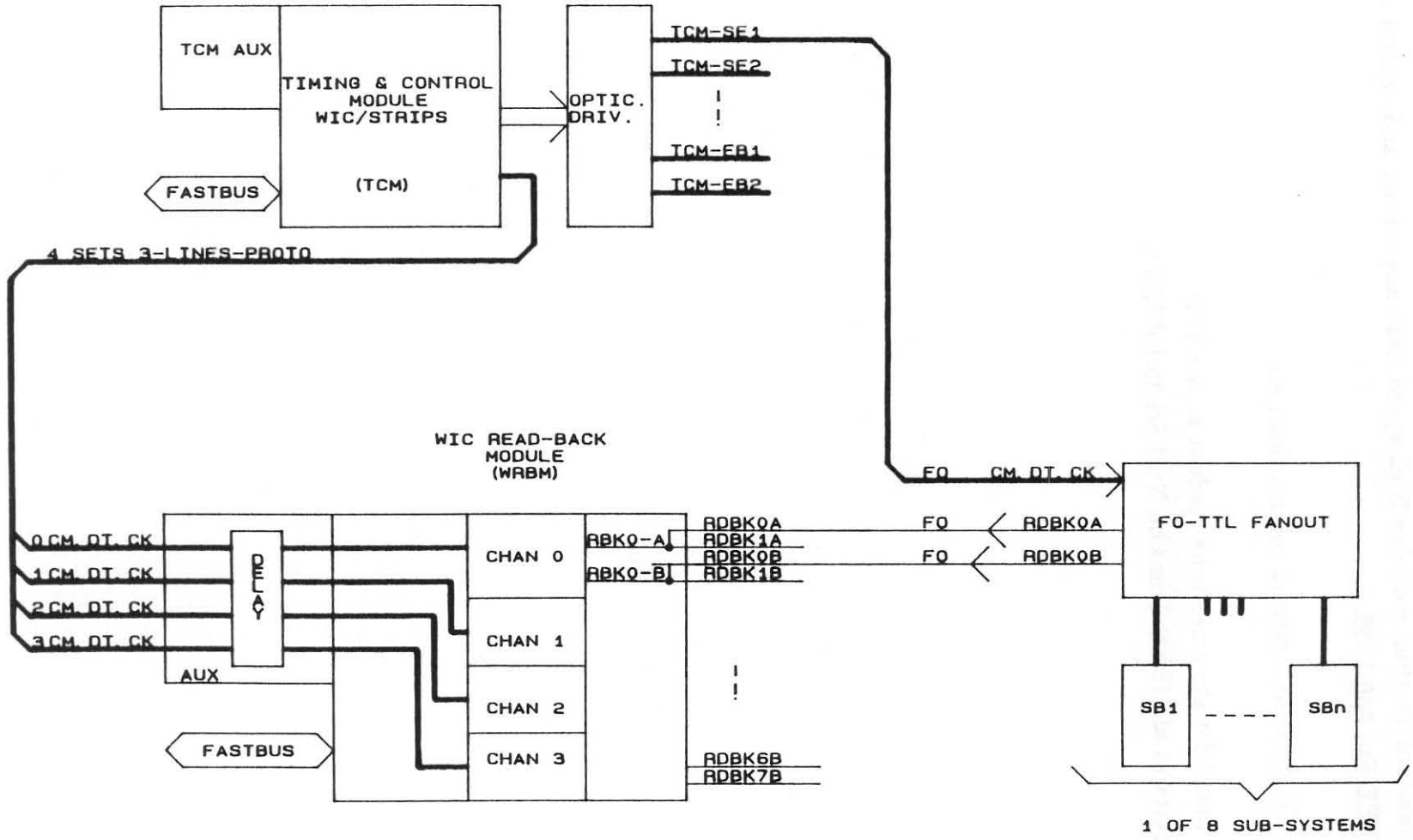

FIG 1. WIC READ-BACK SYSTEM

WIC READ-BACK SYSTEM

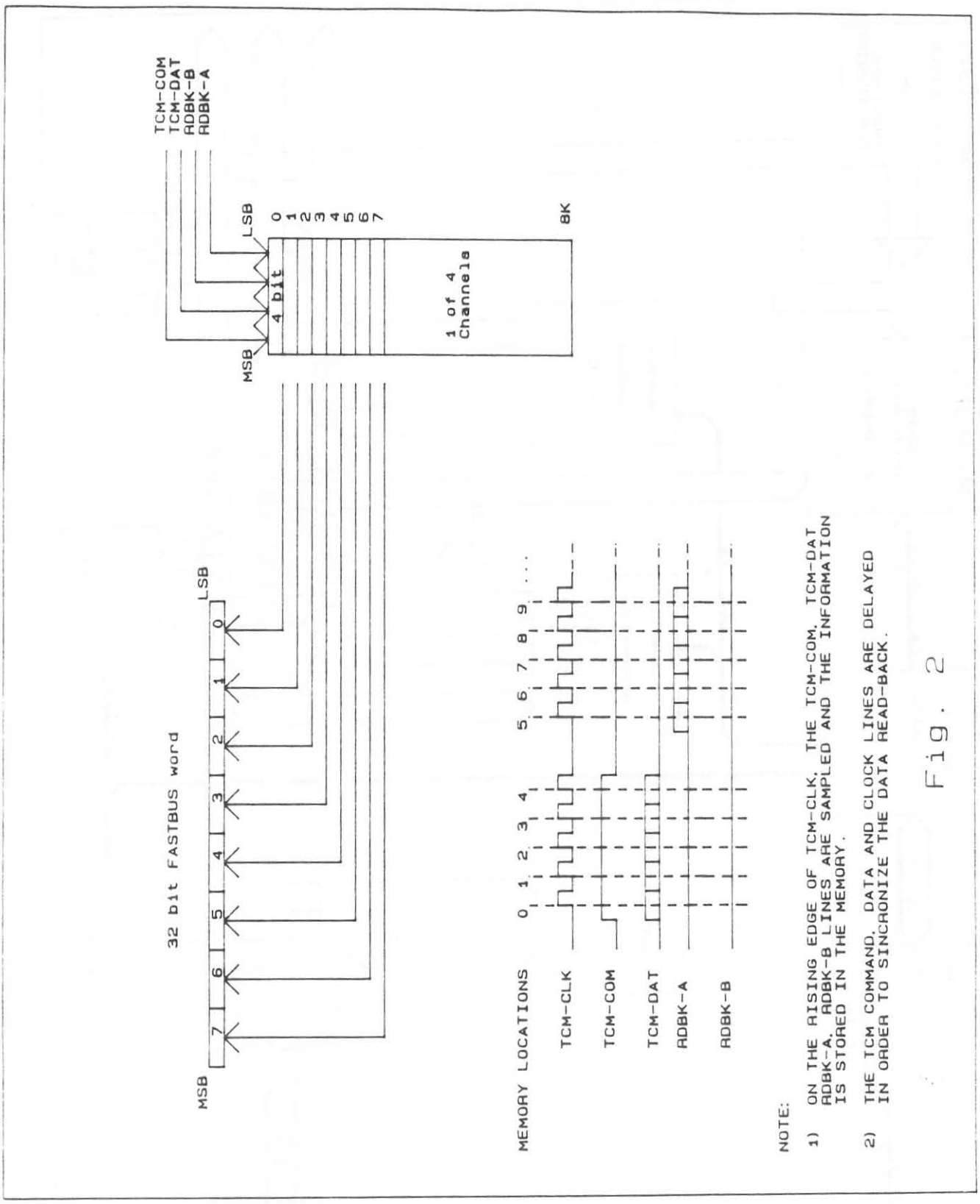

FIG 2. SERIAL STREAM OF IMPUT DATA IN MEMORY AND FASTBUS ACCESSES

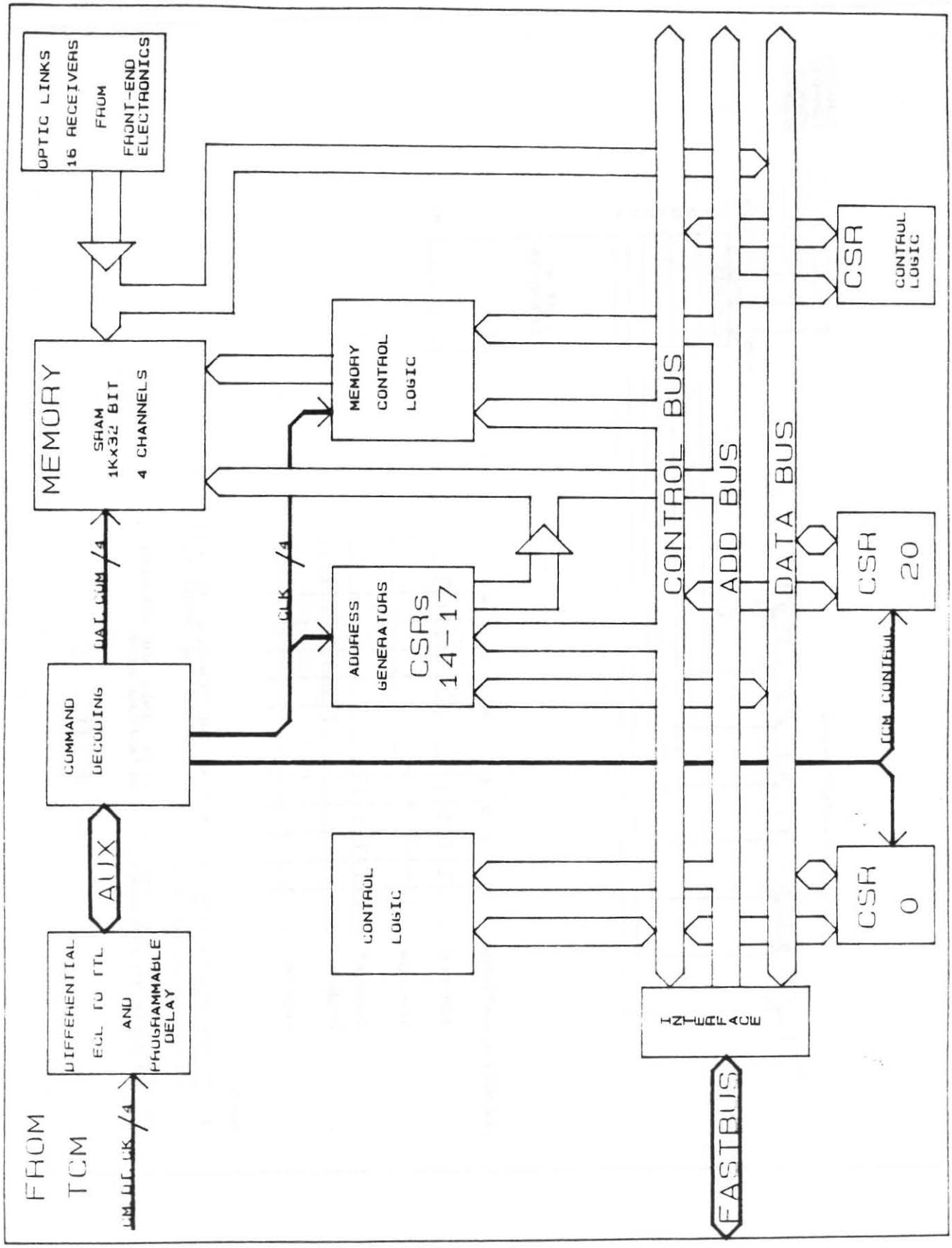

FIG 3. WRBM BLOCK DIAGRAM

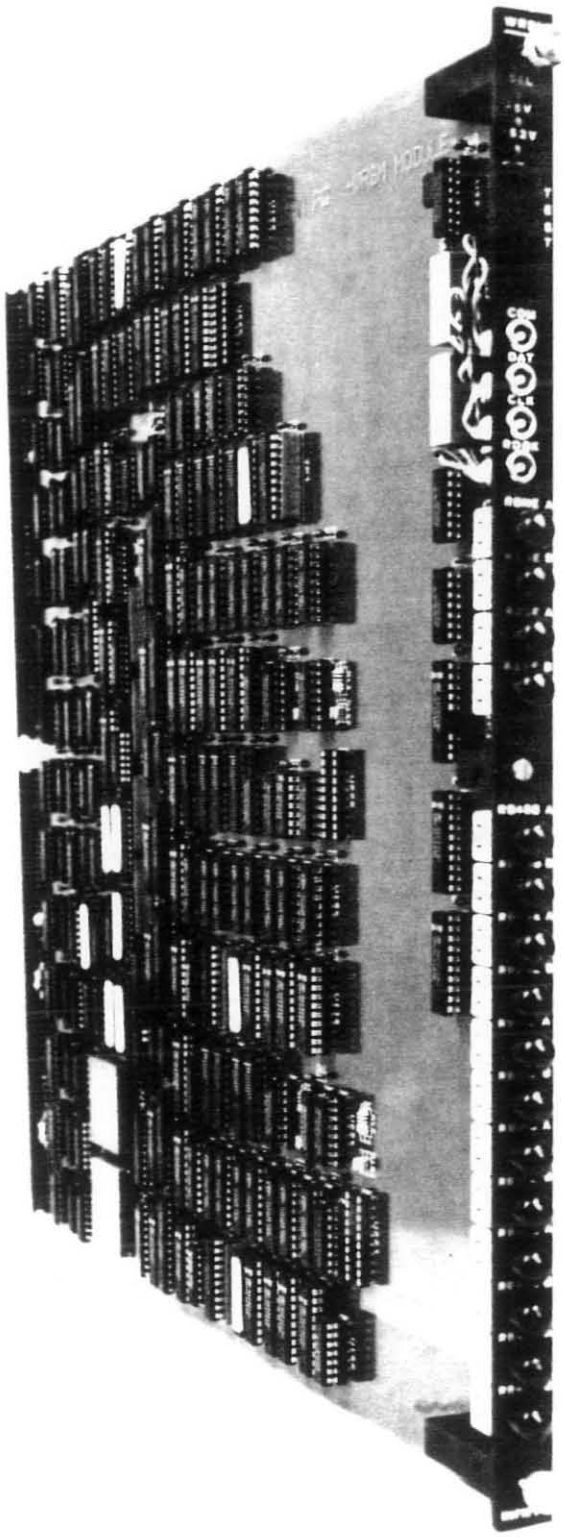

FIG 4. WRBM PHOTOGRAPH