

ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Padova

INFN/TC-88/28

7 Ottobre 1988

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**SPLITTER BOARD FOR STRIP READOUT OF THE WARM IRON
CALORIMETER AT SLD**

SPLITTER BOARD FOR STRIP READOUT OF THE WARM IRON CALORIMETER AT SLD

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1. - Introduction

A controller board, hereafter referred as Splitter Board, has been designed as a part of the read-out system[1] for strips in the Warm Iron Calorimeter of the SLD detector[2]. The strips are coupled to the plastic streamer tubes which instrument the iron flux-return structure of SLD. The readout system consists of 100,000 digital strips, one bit per strip. Signals from the strips are stored digitally on the detector using a system consisting of preamplifier, discriminator, and shift register latch packaged in a custom LSI manufactured by SGS[3]. These chips also provide a wired-OR signal, dig-or, which is used to form muon and cosmic trigger.

Groups of up to 12 boards are connected to form a daisy chain. Data from a maximum of 10 daisy chains are serially transferred to the Splitter Board where they are multiplexed onto an optical fiber.

The Splitter Board provides for the fanout of timing signals and also contains majority logic circuit to combine the wired-OR signals from the individual layers into a single signal to be used in downstream logic to form the muon or cosmic ray triggers. Control functions are also performed by the board. These include the sequence in which the daisy chains are readout and their length, threshold settings for the board discriminators, generation of control signals for the daisy chain and monitoring of the power voltages. Settings can be read-back via a serial cable.

2. - Module Description

The module connections and the logic diagram are shown in Fig. 1. The daisy chain distribute data clocks, threshold voltages, power and a test pattern. Serial data and dig-or also are received from these cables. In addition, the Splitter Board generates load and refresh signals for the discriminator gate width.

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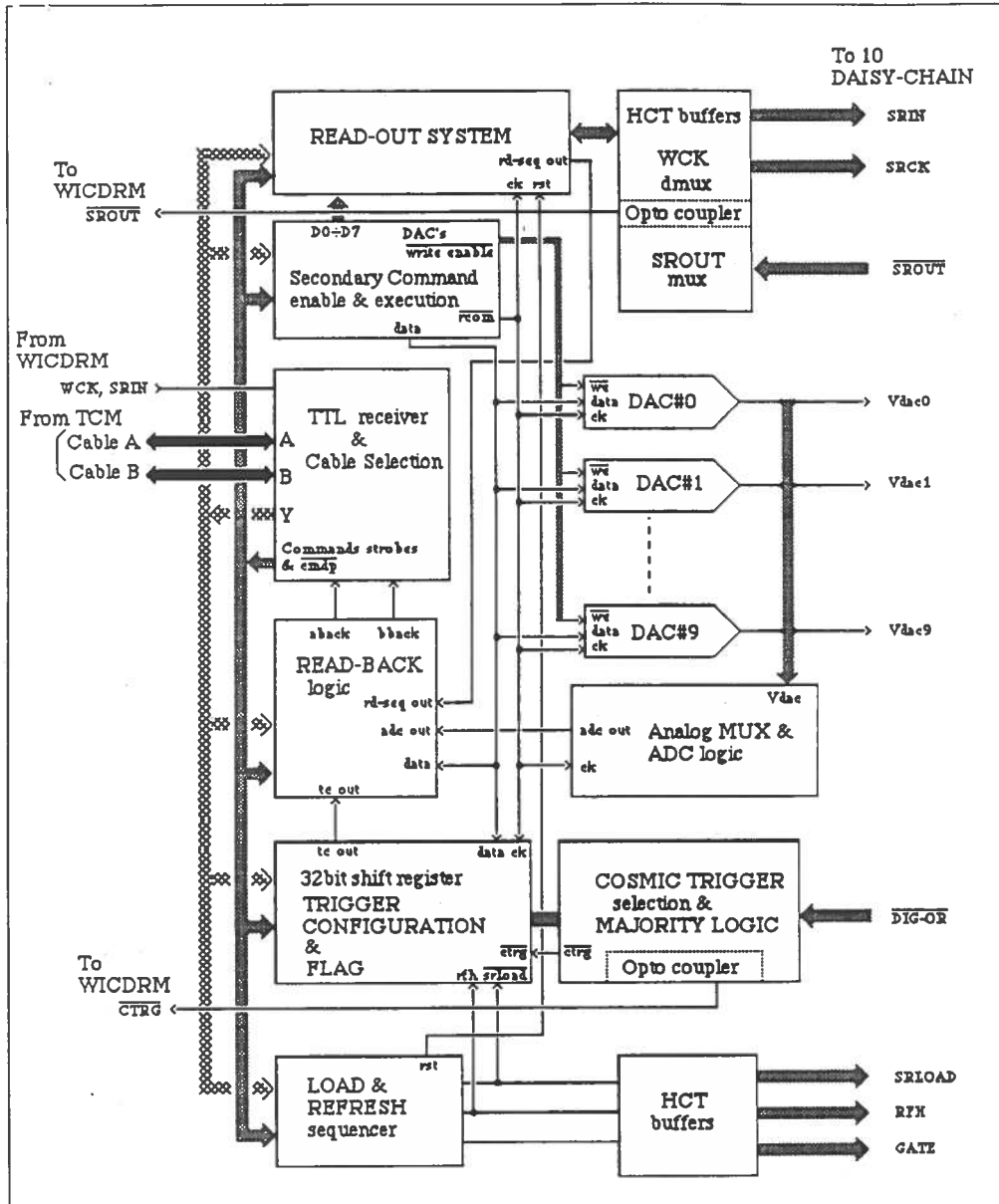


FIG. 1 - Module connections and logic diagram.

The Splitter Board communicates serially with the Timing and Control Module (TCM)[4] via two sets of differential TTL lines. The sets are identical and are duplicated for reliability reasons. They are used to transmit control commands and timing signals to the Splitter Board, as shown in Fig.4b. The Cmd line identifies a command being transmitted, the Data line, when Cmd is high, transmits a 5 bit command code and furnishes data necessary for the execution of the command, such as DAC values for threshold setting. The clock line provides synchronization pulses and timing marks. Control commands requiring feedback use the read-back Rb line.

The other two lines are generated by the data acquisition module (WICDRM)[5] and used only during data readout. The data and cosmic trigger signals are directly sent by each SB to the WICDRM via a fiber optic cable (see Fig 13a).

The strip readout of the Warm Iron Calorimeter foresees 42 Splitter Boards. All the Splitter Boards relative to a single WICDRM form a group: we have 6 of such groups. The first Splitter Board of every group is preceded by a card which converts optical signals from the WICDRM (2 lines) and TCM (8 lines) into differential signals. Each Splitter Board passes on these signals to the next SB, while duplicate is converted into TTL standard.

3. - Control Commands

The control commands are divided into two groups, primary and secondary. The SB always responds to primary commands, but responds to secondary commands if previously enabled. This allows one TCM to communicate with a Splitter Board individually or as a SB group.

The Splitter Board has implemented 13 Control Commands.

Primary Commands

- *Select Me.* Selects which cable is used to communicate with the TCM.
- *Run Short Gate* Executes the normal run sequence. The sequence is triggered using the timing marks from the TCM.
- *Run Long Gate.* Similar as above, except that the run sequence is executed using a long gate width for the discriminators.
- *Set Address* Enables a Splitter Board for following secondary commands. An 8 bit word, sent along with command, is used to identify the module.
- *Reset Address* Disables the Splitter Board selected by a Set Address. An 8 bit word is used to identify the module.

Secondary Commands

- *Load Readout Table..* A table is stored in RAM, containing the length and in which order the daisy chains are to be readout.
- *Load Trigger Configuration.* Writes a word into an internal register which sets the muon/cosmic trigger configuration such as enables for strip planes, number of planes for trigger to fire and the majority level.
- *Load Threshold DAC's.* Loads threshold values into DAC's, one for daisy chain.
- *Data Loopback.* Used to test communication failures.
- *Read Readout Tables.* Reads the readout table stored in RAM.
- *Read ADC's.* Reads threshold and power voltages using an ADC.
- *Read Trigger Configuration .* Reads the trigger configuration and a register containing control flags.
- *Clear Control Flags.* Clear the control flag register.

4. - Circuit Description

The SB is logically divided into 10 functional blocks:

- 1) Differential receiver & cable selection
- 2) Load and refresh sequencer
- 3) Secondary command enable & execution
- 4) Read-out system
- 5) DACs for threshold values
- 6) ADC logic
- 7) Trigger configuration shift register
- 8) Cosmic trigger management
- 9) Read-back logic
- 10) Voltage supply filters & security

For sake of simplicity every block will be referred to by its number in the following sections.

The connections of the SB are as follows:

MODULE	LINE NAME	PROTOCOL	I/O	
TCM	Cable A:	ACMD	differential	input
		ASTB	"	"
		ADATA	"	"
		ABACK	"	output
	Cable B:	BCMD	"	input
		BSTB	"	"
		BDATA	"	"
		BBACK	"	output
WICDRM	WCK	differential	input	
	SRIN	"	"	
	SROUT	optical	output	
	/COSMIC	"	"	

In the daisy chain connectors there is one line of electric shielding for the cables This line is joined to a pin put next to each connector in order to allows the connections of external shielding. The other lines are standard for SGS cards.

Block (1) - Fig. 2 -

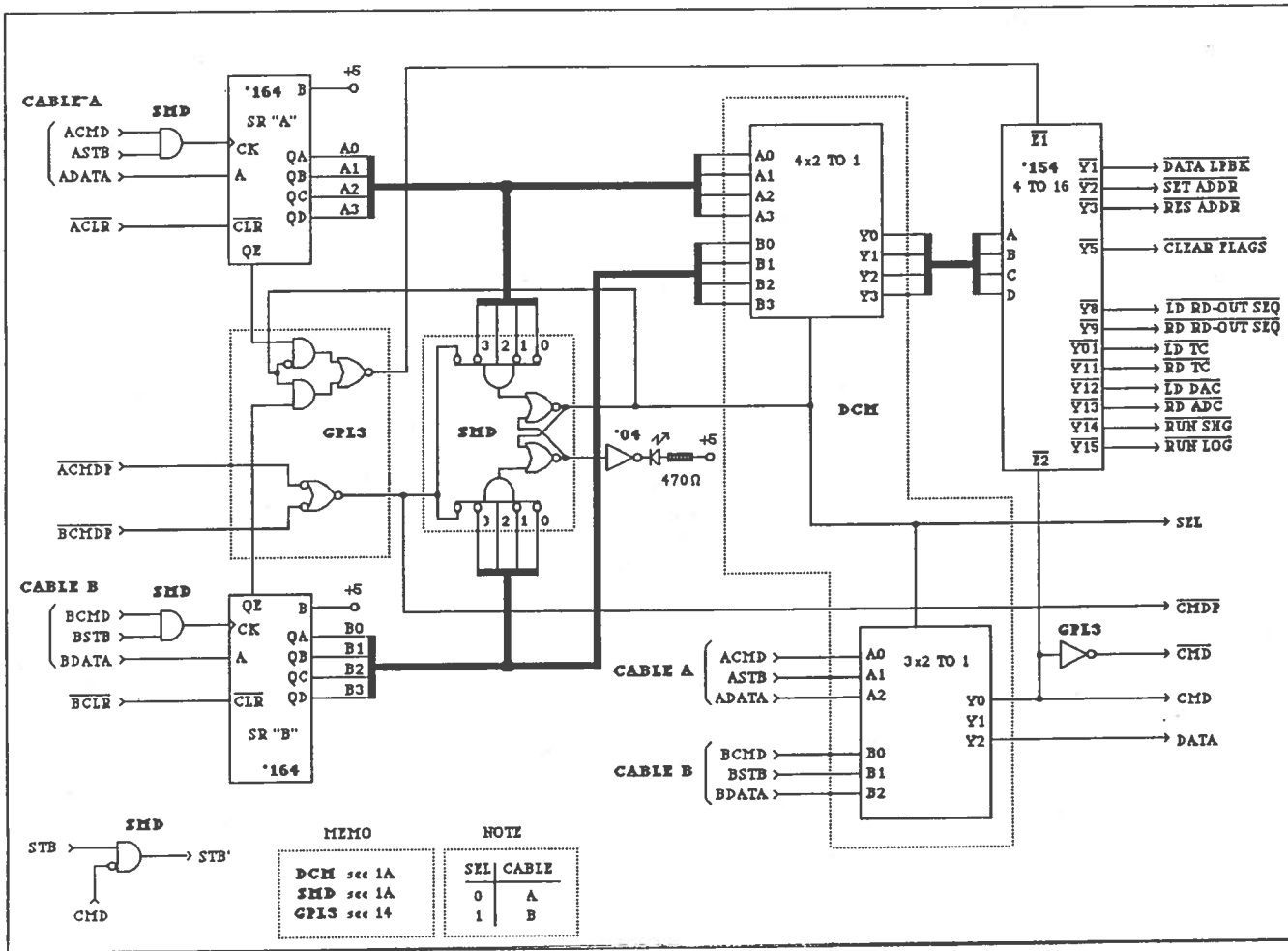


FIG. 2 - Select-Me scheme.

The first function consists in the selection of cable A or B considered valid for communication with the TCM.

Two shift registers, cleared at the start of a command by a one-shot, receive the op-code and send it to the SMD and DCM devices.

The Select Me Device controls whether the op-code corresponds to the command Select Me. At the end of command, indicated by another one-shot pulse, it forces the SEL line to 0 or 1, according to where the Select Me command has arrived.

The Data & CoMmand device multiplexes signals and op-codes coming from cable A or B, according to the select line.

Every op-code selects its command strobe line setting it to 0.

The mux disables all command strobes during the op-code arrivals in such a way that during the reception no command can be executed.

Moreover the mux is enabled only if the op-code sending was succesfully: this is done by using the check bit of each command as enable of mux.

SMD also generate the STB' signal which is as STB without the first 5 pulses, these being used only for the two shift register above (see Fig 4a).

Block (2)

- Fig. 3 -

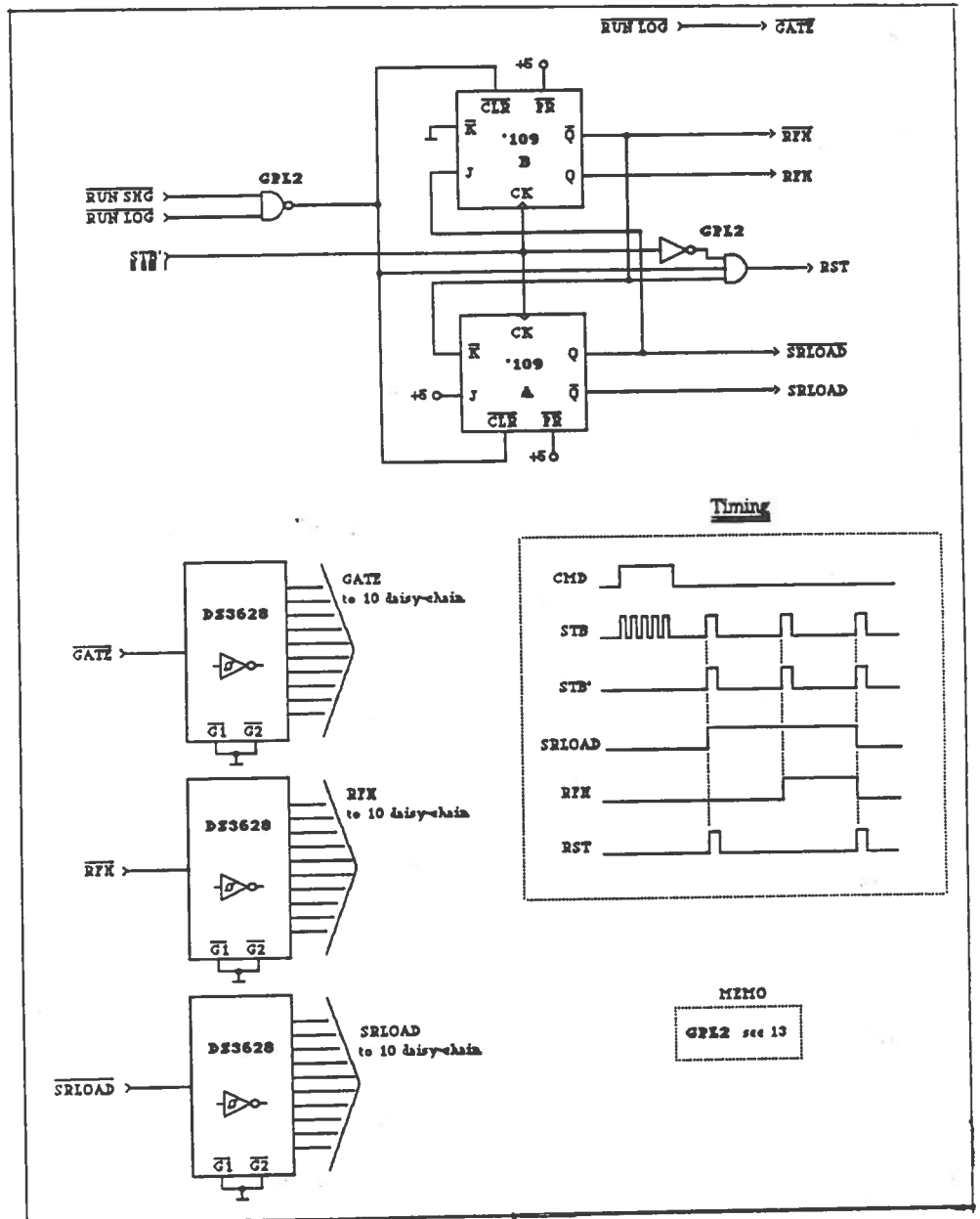


FIG. 3 - Timing sequencer.

This block executes two primary commands generating the timing shown in Fig. 3. As for timing we have chosen to set the REFRESH line (RFH) high in order to disable the one-shots on the SGS boards during Read-Out. This choice guarantees against random DIG-OR signals which are a possible source of noise in the daisy chain cable. The timing sequence is repeated every 3 strobe pulses (timing marks) coming from the TCM, without any other run commands. Thus other loads and read-outs are possible when a cosmic trigger occurs.

A single read-out by the WICDRM can be performed anytime, but only once, between the first and the third pulse of STB line.

In each sequence a RESTART signal directed to block 4 is also generated; this signal resets the read-out system and prepares it for the next read-out.

The daisy chain signals are driven by current buffers.

Block (3) - Fig. 4 -

This block enables or disables the SB for the secondary commands and generates correct timing for the execution of these commands.

The enable/disable of the secondary commands is performed by the SET/RESET ADDRESS commands by sending on the data line the 8-bit address of the chosen SB, to operate with a single SB, or 0 to enable/disable all SBs at the same time.

The /SCE line is forced to 0 or 1 according to the SB is enabled or disabled.

A SR sorts the data which come from the serial line DATA.

A sequencer based on the 4-bit counter "master" generates a strobe pulse, /RCOM, when the parallel data are ready, and a clock, /ST1, when serial data are validated.

/RCOM occurs every 8 or 12 /ST1 pulses, according to whether the command to be executed requires 8 or 12 bits, or a multiple of them.

See timing in Fig 4a.

Block (4) - Figs. 7, 5 and 4 -

Each daisy-chain is seen as a long shift register in such a way the SB, during a read-out, must read some shift registers one at a time.

The daisy chains are connected in parallel: the shift-in arrives to all daisy chains simultaneously, but a demultiplexer (WCKDMUX) sends the clock (WCK) to only one daisy chain and a multiplexer (SROUTMUX) returns only one shift-out to the WICDRM (Fig. 7). The shift-in line (SRIN) is delayed with some inverters to equalize the WCK delay introduced by the WCKDMUX.

A RAM contains the readout table with the address sequence of the daisy chain to be read, in the first nibble, and the length of each, given as number of SGS board, in the second nibble.

In this way one scans the table, i.e. changes the mux address, every time the read-out of the plane is completed.

During the read-out a 4-bit counter, Table Pointer, scans the RAM table, following the terminal count of the SGS counter.

The SGS counter is a double stage counter: the first one with 32 fixed modulo, each SGS card having 32 bits to be read; the second stage, 4-bit counter, with a variable modulo, according to the content of the RAM table, the number of SGS cards in each plane being in general different.

So the terminal count from the SGS counter indicates that a plane has been read, and starts a one-shot pulse which increments the Table Pointer and loads a new value into the SGS counter.

The logic shown in Fig. 5 contains the possibility of writing and reading the RAM table, obtained by using parallel data and the /RCOM pulse.

The RESTART line, coming from block 2, initializes the above counters for a correct reading of the first plane.

The last byte of the RAM table must be \$FF, in order to stop the Table Pointer and disable all the daisy chains upon completing the read-out. So if the WICDRM sends more clocks than those needed, the Table Pointer remains stopped at an address of non existing plane, and therefore the data sent are forced to 0.

There are 10 DACs to generate independently one Vdac per plane.

Block (5) - Figs. 9 and 4 -

We have chosen the 12-bit DAC AD7543 with an internal shift register which minimizes the logic connections. The DACs are selected with a maximum gain error of one LSB.

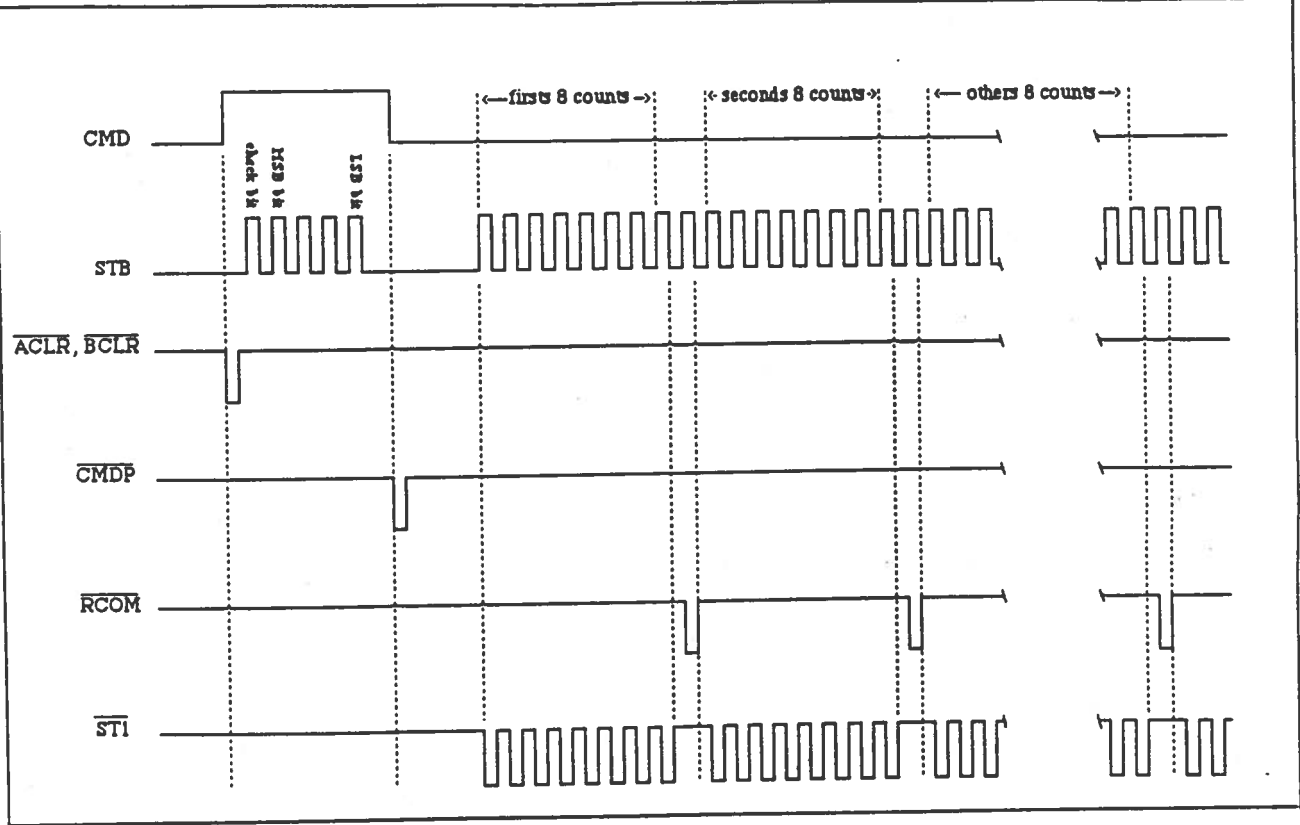
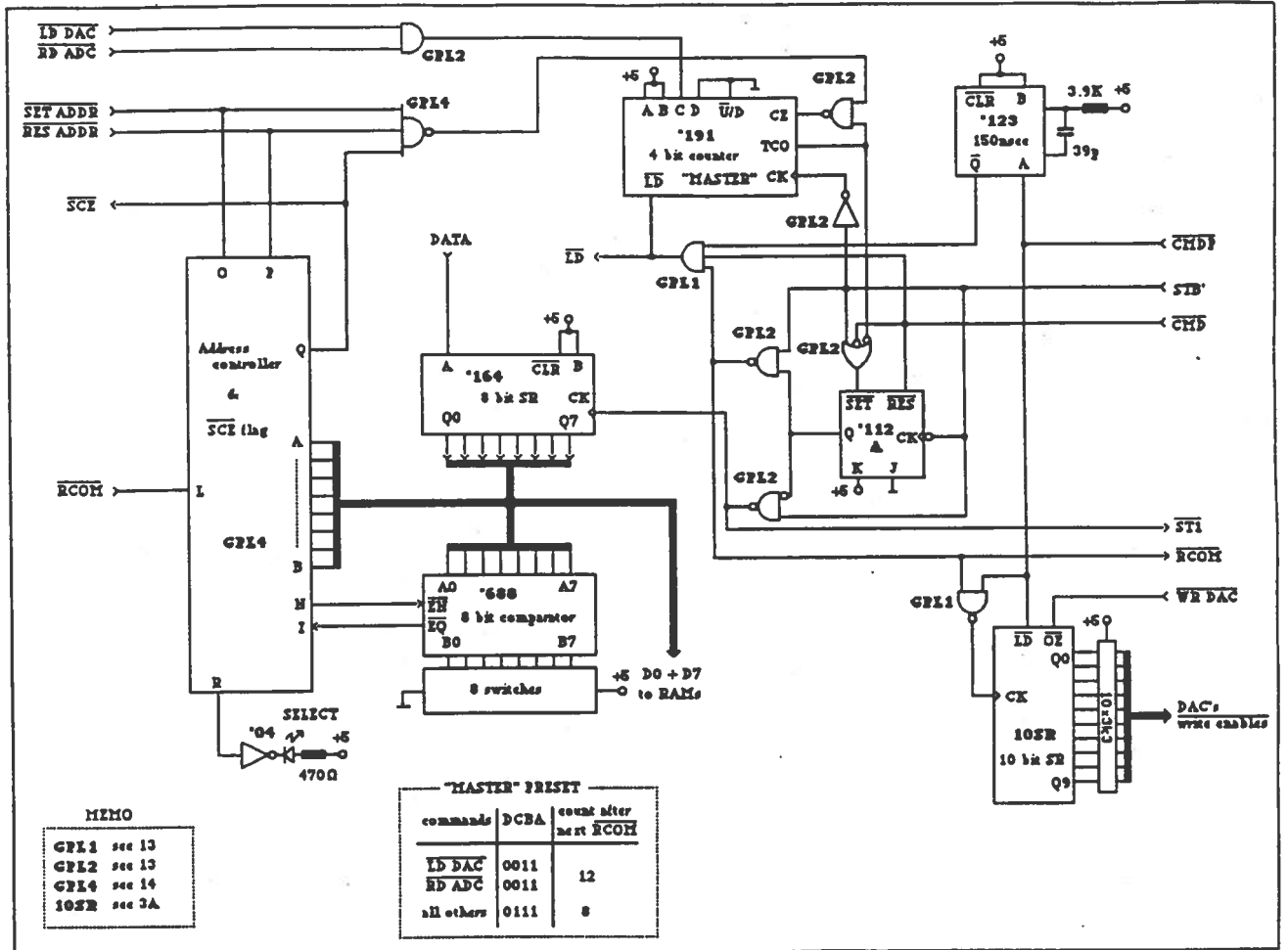


FIG. 4 - Secondary command enable & execution. 4a) Timing sequence.

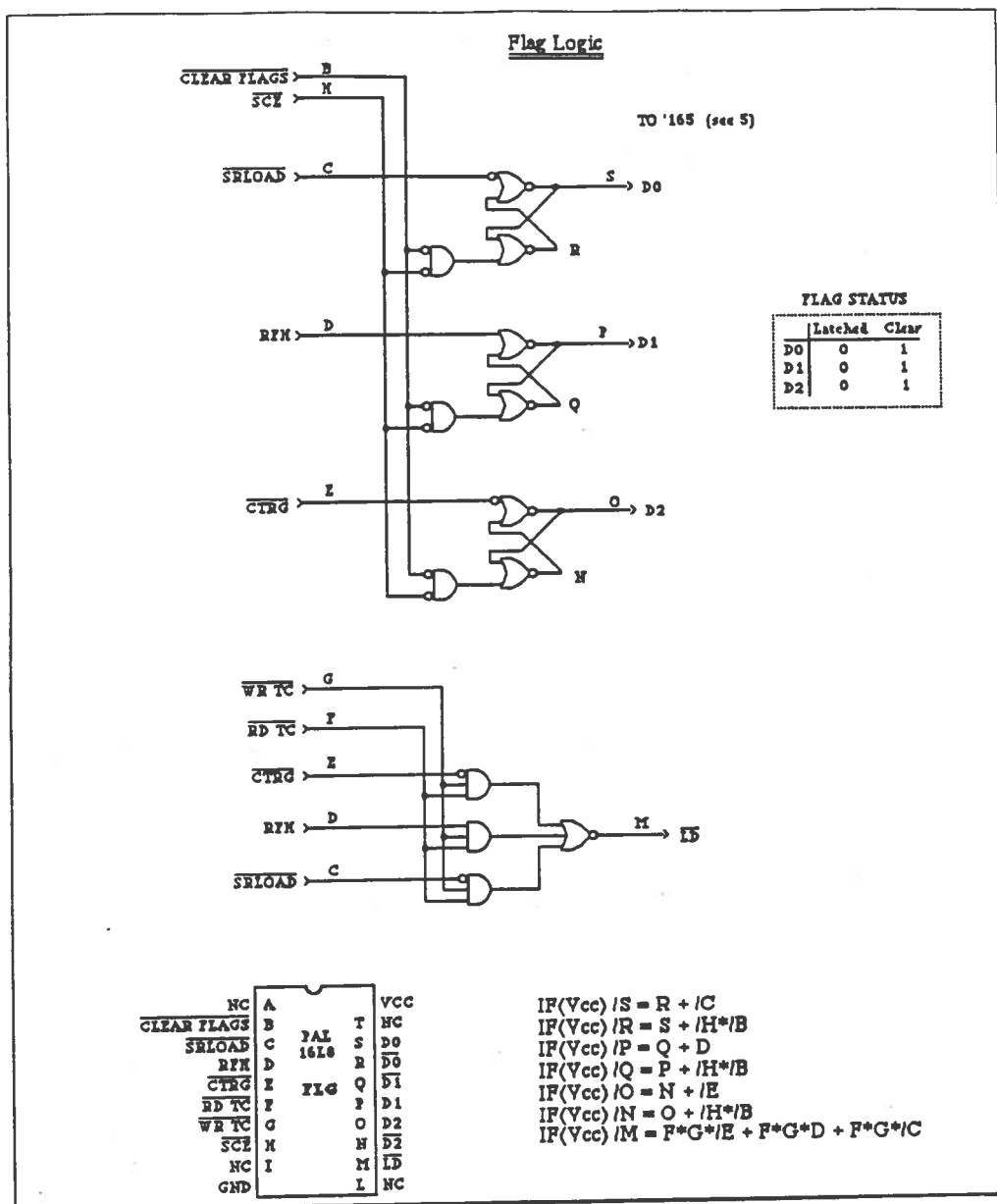


FIG. 6a - Flag logic.

A single command loads all the DACs, and the 10-bit Shift Register (10SR), clocked by the /RCOM pulse, enables one DAC at a time.

A 0-40 Volt range for Vdac is obtained for every daisy-chain with an OP and a transistor voltage buffer.

Block (6) - Figs. 8, 8a and 4a -

The Vdac's, the supply voltages and the Vref are monitored by a 10-bit ADC, one at a time by a single command. A 4-bit counter Channel Pointer scans the address of the analog multiplexer every /RCOM signal.

In this case the STB' line substitutes the /ST1 line because, for the chosen ADC, the start conversion pulses (CVST) must cover two clock pulse. A simple logic with a gate and a flip/flop allows the generation of correct timing for the start conversion (see Fig. 8a).

For this command the maximum frequency of STB clock is fixed at 5.45MHz according to the ADC characteristics, and to the switching rate of the analog mux which is about 200 nsec.

Block (7) - Figs. 6, and 6a -

The Trigger Configuration shift register (TC) must furnish in parallel 24 bits for the cosmic ray management set up. Other 3 bits of an additional 8bit shift register are used to read the status flags of the /LOAD, RFH and /COSMIC lines.

The resulting 32 bits are cascaded as a single shift register while a double multiplexer provides the needed logic for a correct loading and reading.

The Flag LoGic device (FLG) instead contains the 3 flags and the logic to load them into the shift register.

Block (8) - Figs. 11, 12 and 13a -

Cosmic trigger management is done in three levels: a first to select planes where to see the /DIG-OR signal, with the 10 Plane Select lines; another to fix planes where the /DIG-OR signal must be always present, with the 10 Plane request lines; the last to make a majority logic between /DIG-OR signals, previously filtered, with the 4 "Majority Level" lines (see Fig. 6).

The plane selection includes a termination with a pull down transistor for each line to avoid possible noise on the daisy-chain cables.

The ECL gates are chosen as fast current generators: a common base transistor provides the current summing and the current/voltage conversion. A 4-bits DAC generate the voltage corresponding to the majority level selected. This is obtained with another common base transistor, in order to equalize thermal drift of the two comparator inputs. A fast LM261 comparator is used to discriminate.

Block (9) - Fig. 13 -

Two transistors in common-base insure impedance adaptation.

The read-back logic is made by the single Data Loopback Device (DLD) which provides the connection of the read-back lines ABACK, BBACK to TCM module.

Four signals can be backed to the TCM each by its own command: the output of the ADC (/ADC OUT), the output of the Trigger Configuration shift register (TCOUT), the output of the RAM table and finally the DATA line to perform a check of the connections.

All these signals are backed in positive logic.

Block (10) - Fig. 10 -

The voltage supplies which are provided to each daisy-chain, +12V and +Vcc, are previously filtered.

The +Vcc value can vary from a minimum of +7.0 up to +20 Volt. Inside the SGS Vcc is fixed to +5Volt by a regulator.

The Splitter Board provides an high current regulator for the +12 used by the SGS boards. The other voltage supplies, which are used by SB, are regulated and filtered.

Each supply line is provided by a resettable fuse which increase safety and reduce board maintenace.

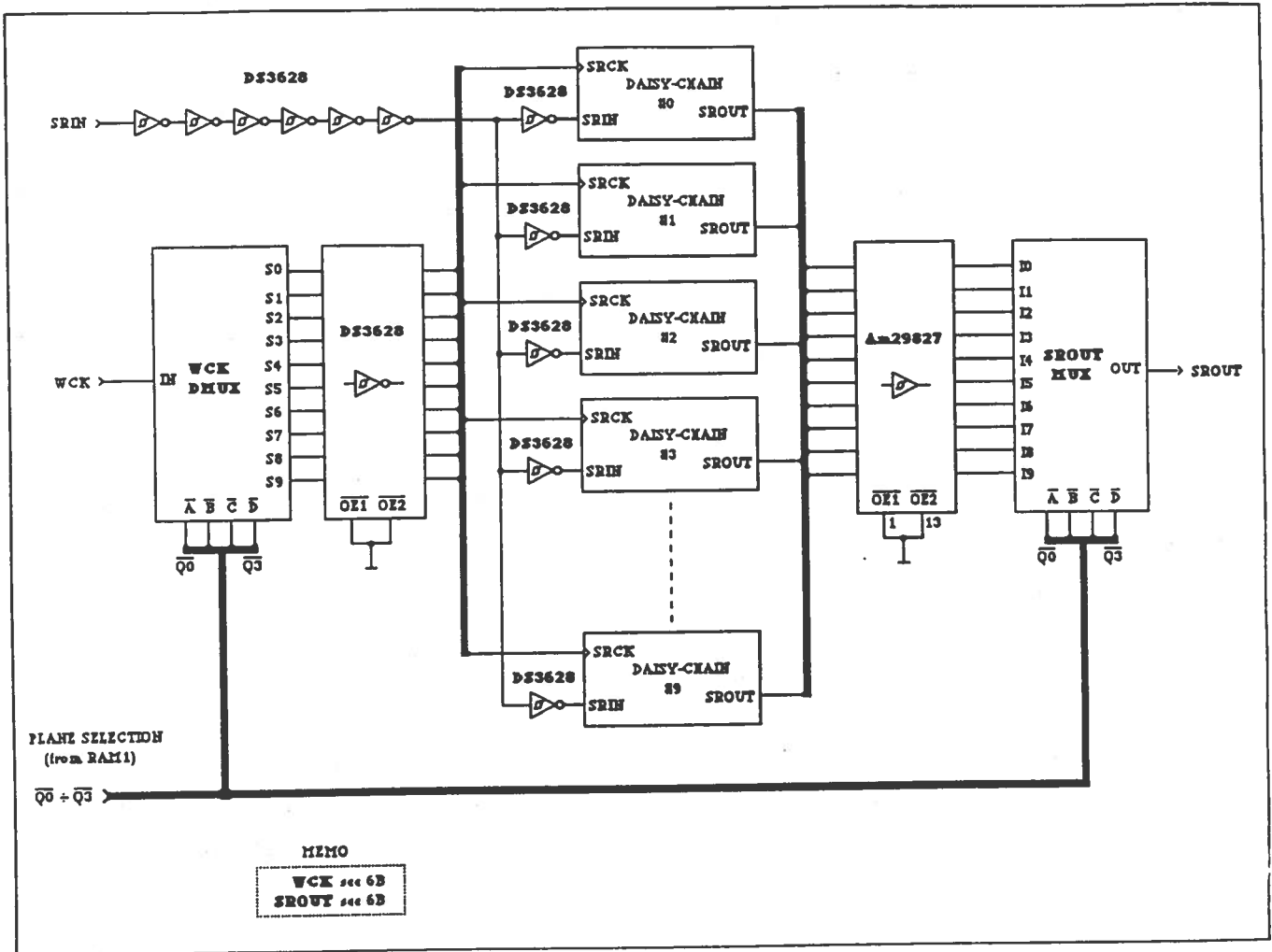


FIG. 7 - Plane selection for read-out.

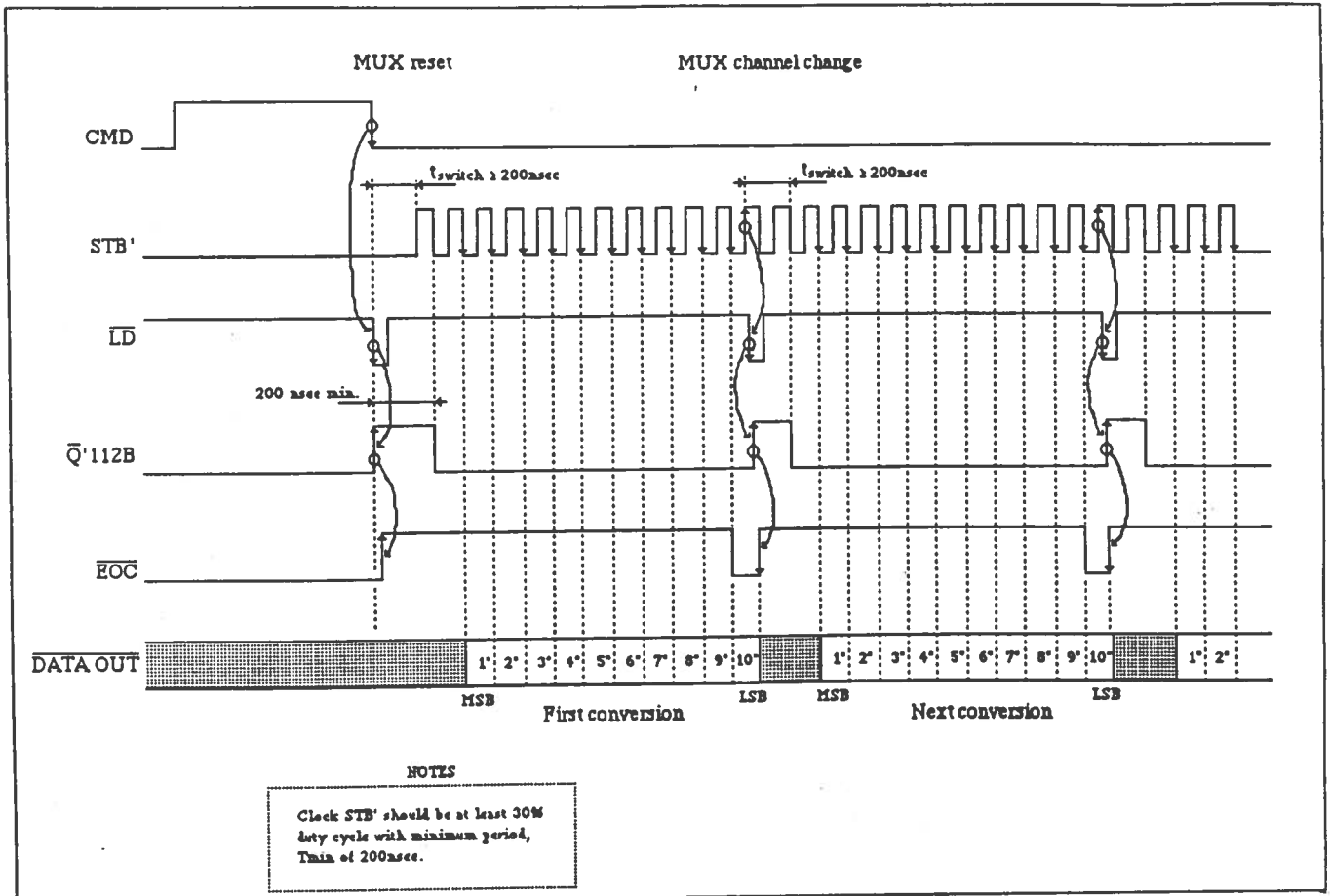
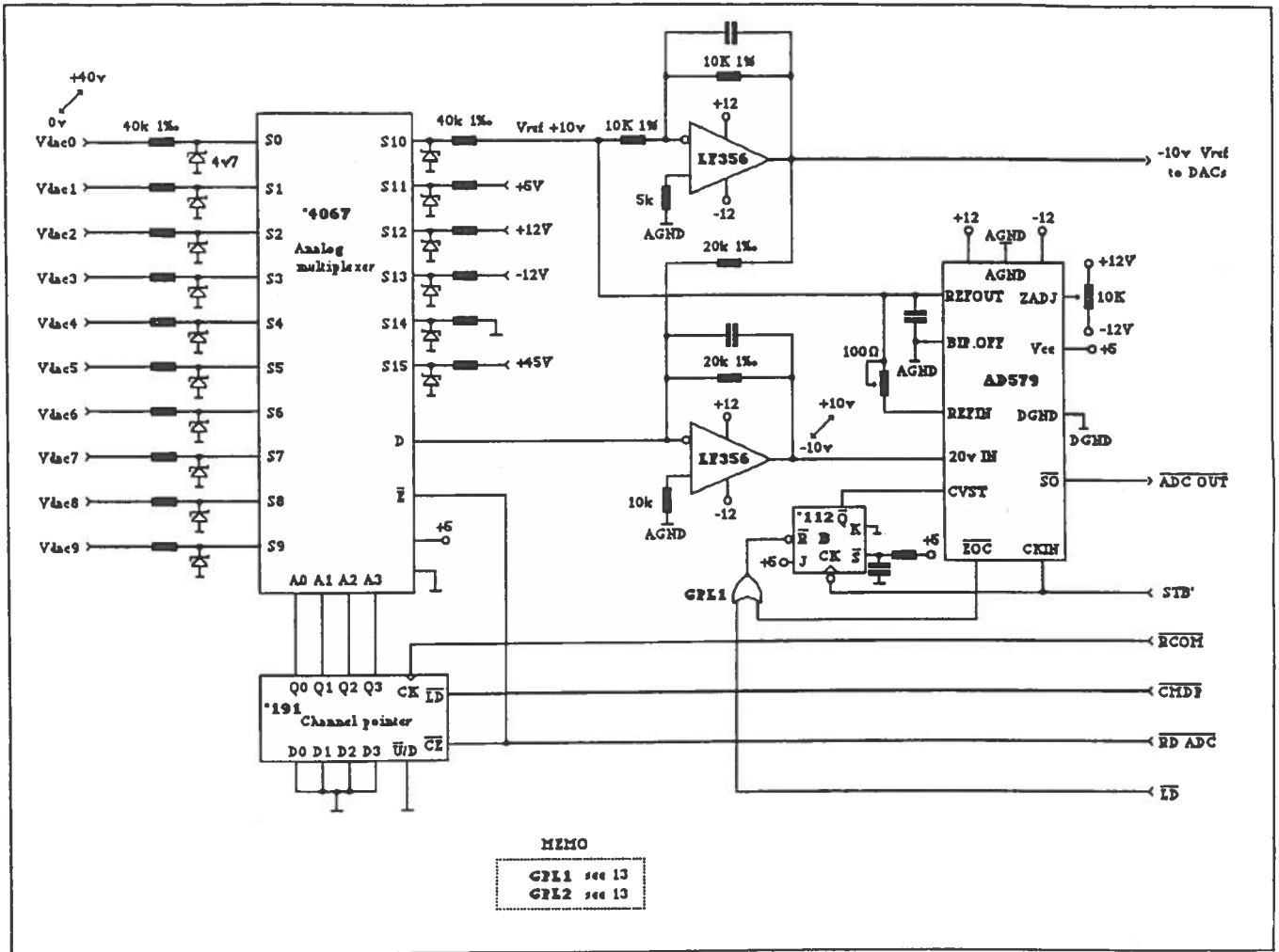


FIG. 8 - Vdac monitoring system. 8a) - ADC timing.

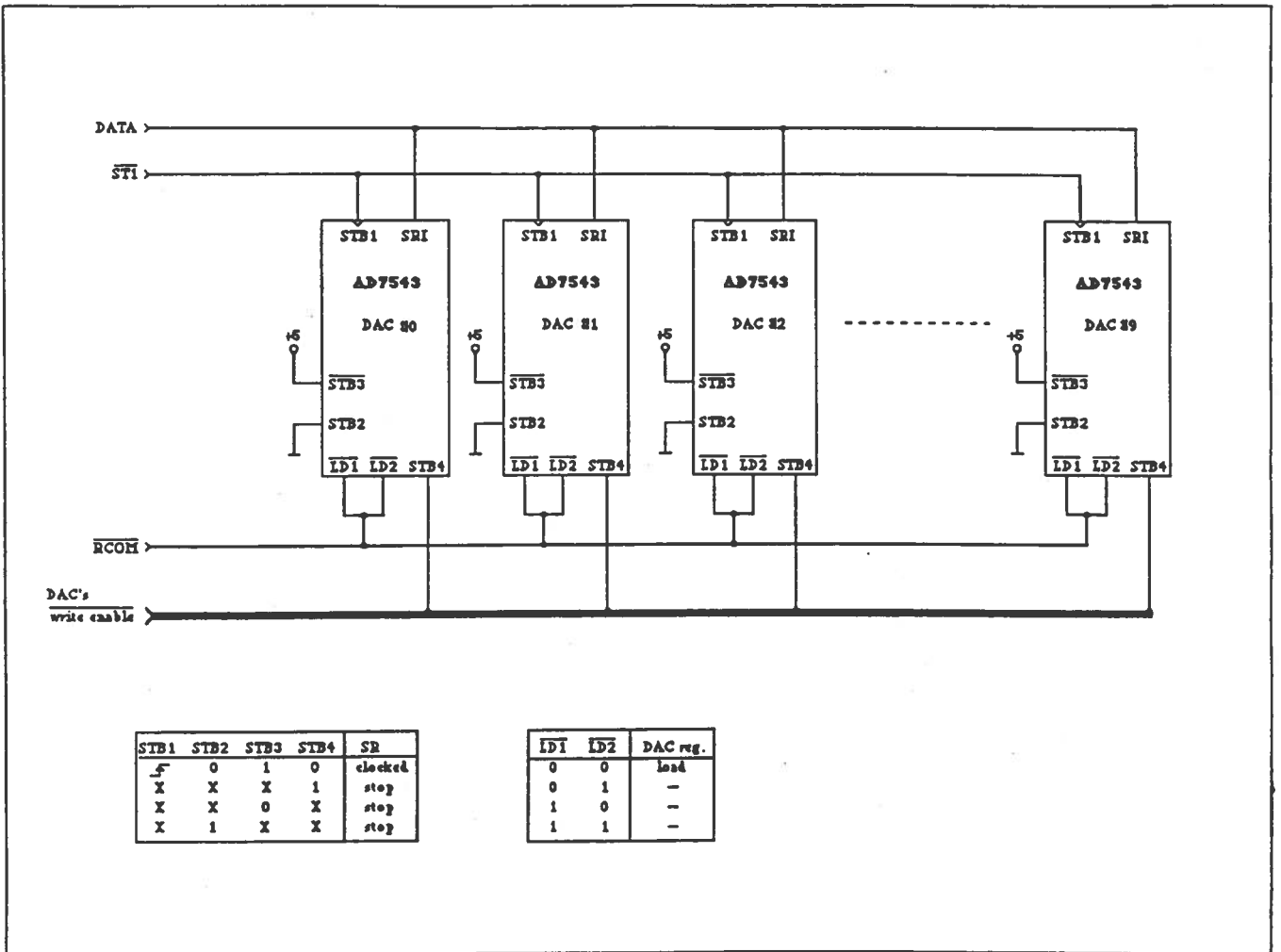


FIG. 9 - DAC's logical connections.

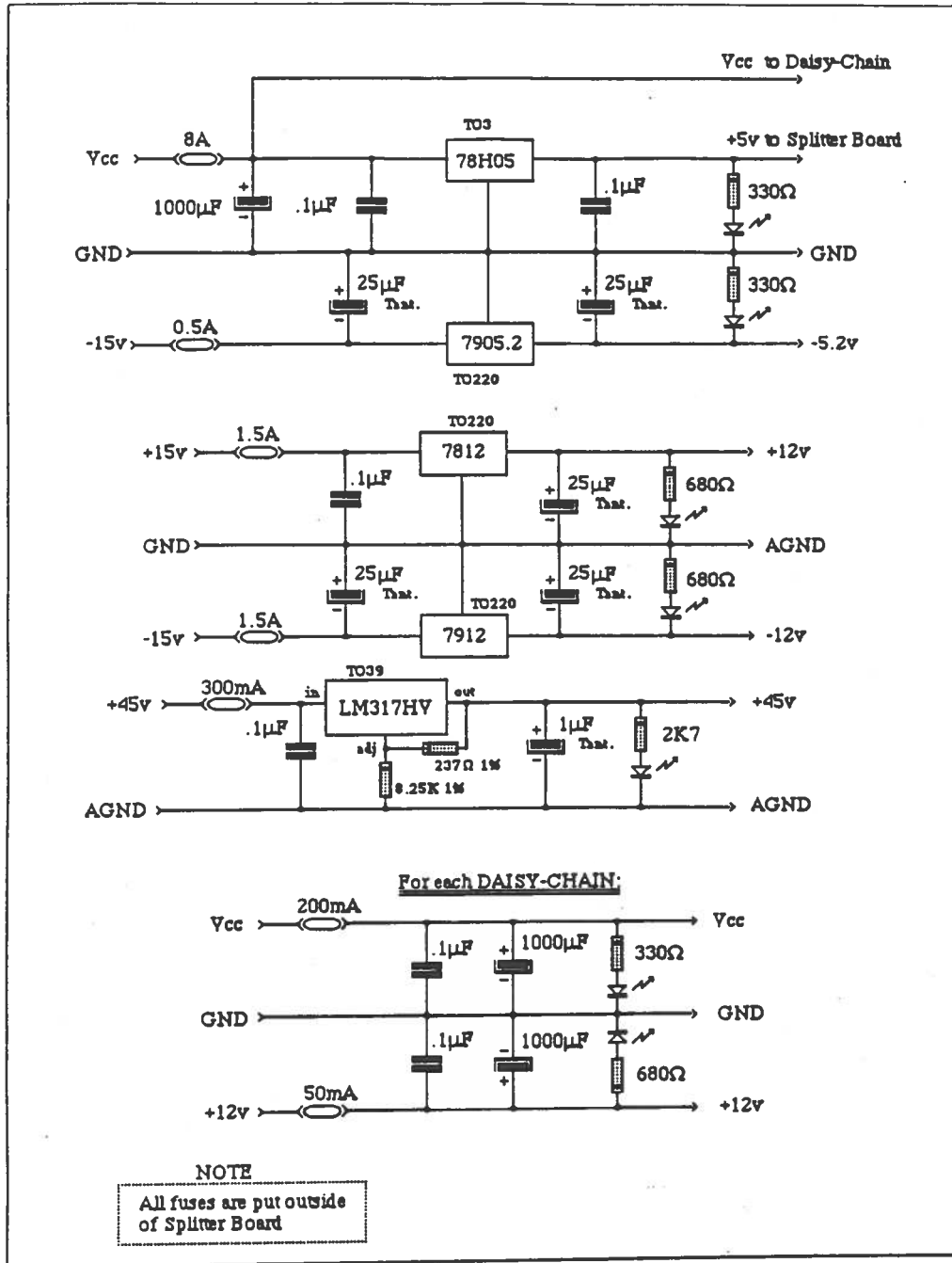


FIG. 10 - Voltage supply fuses and filters.

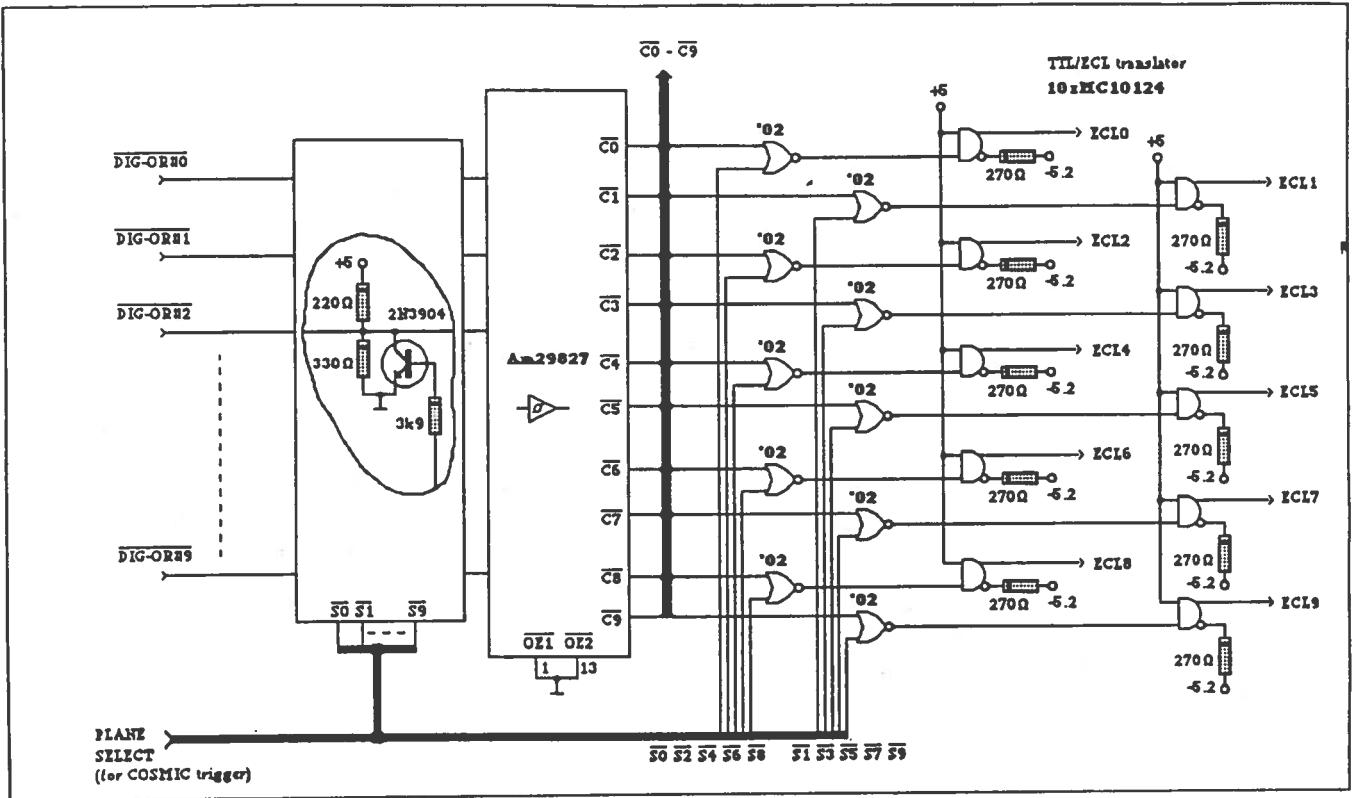


FIG. 11 - Cosmic trigger system (logical connections).

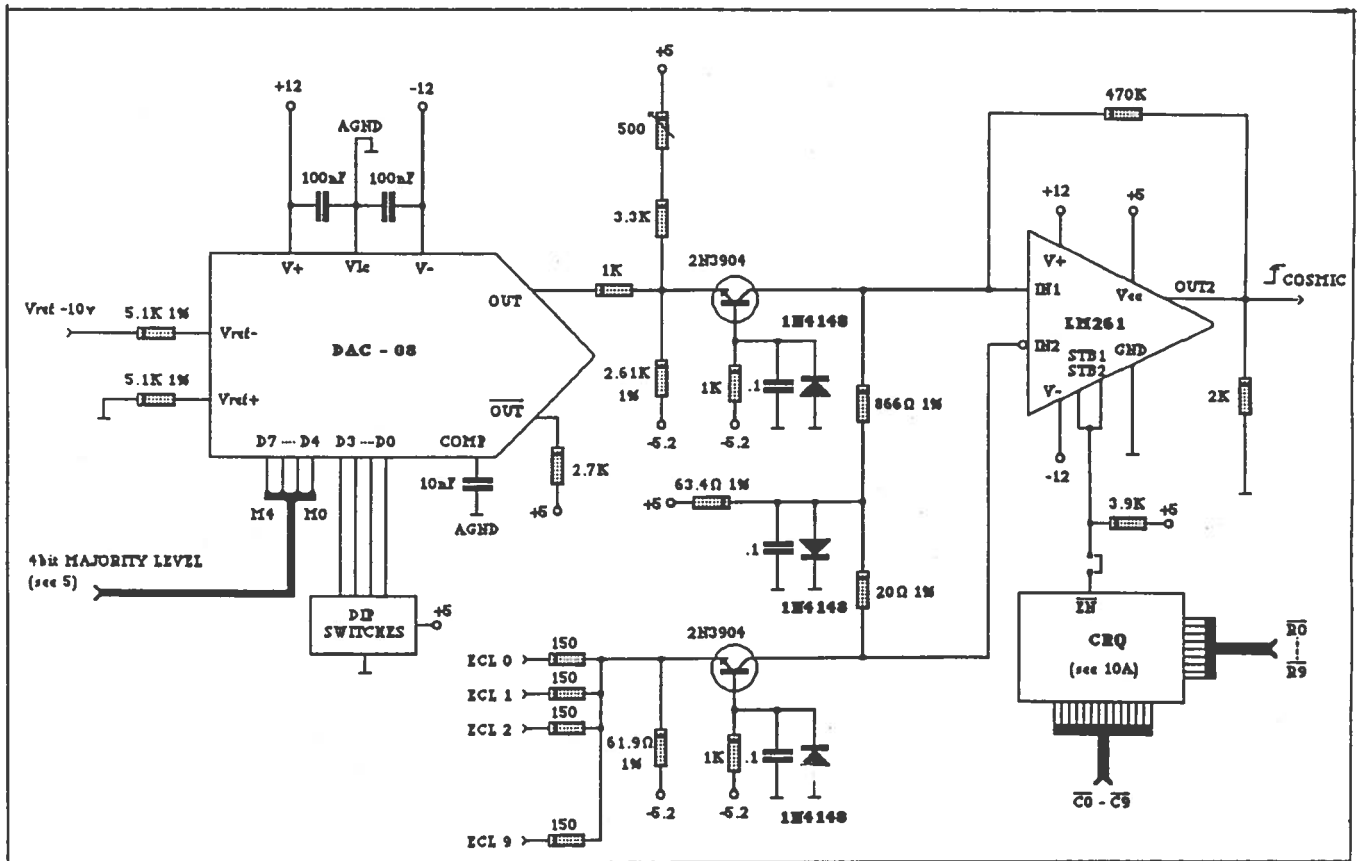


FIG. 12 - DAC & comparator for majority logic.

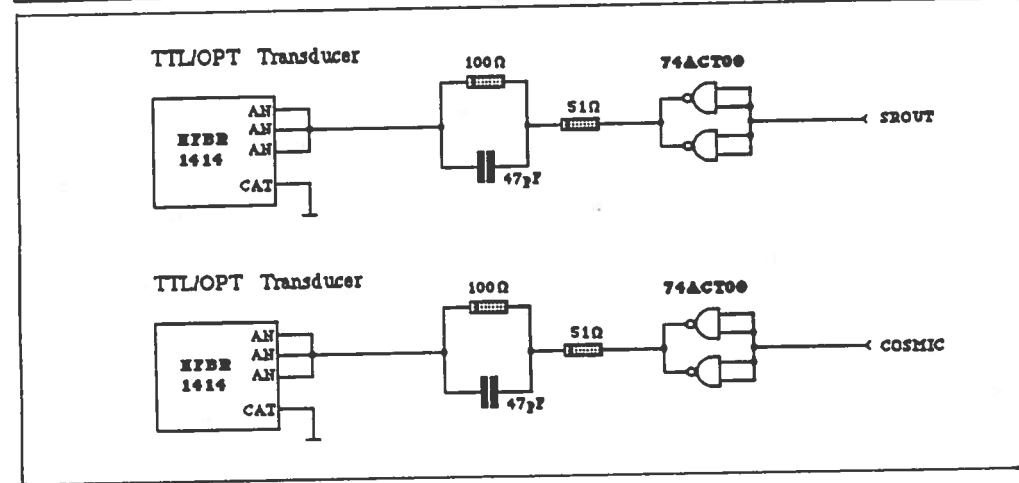
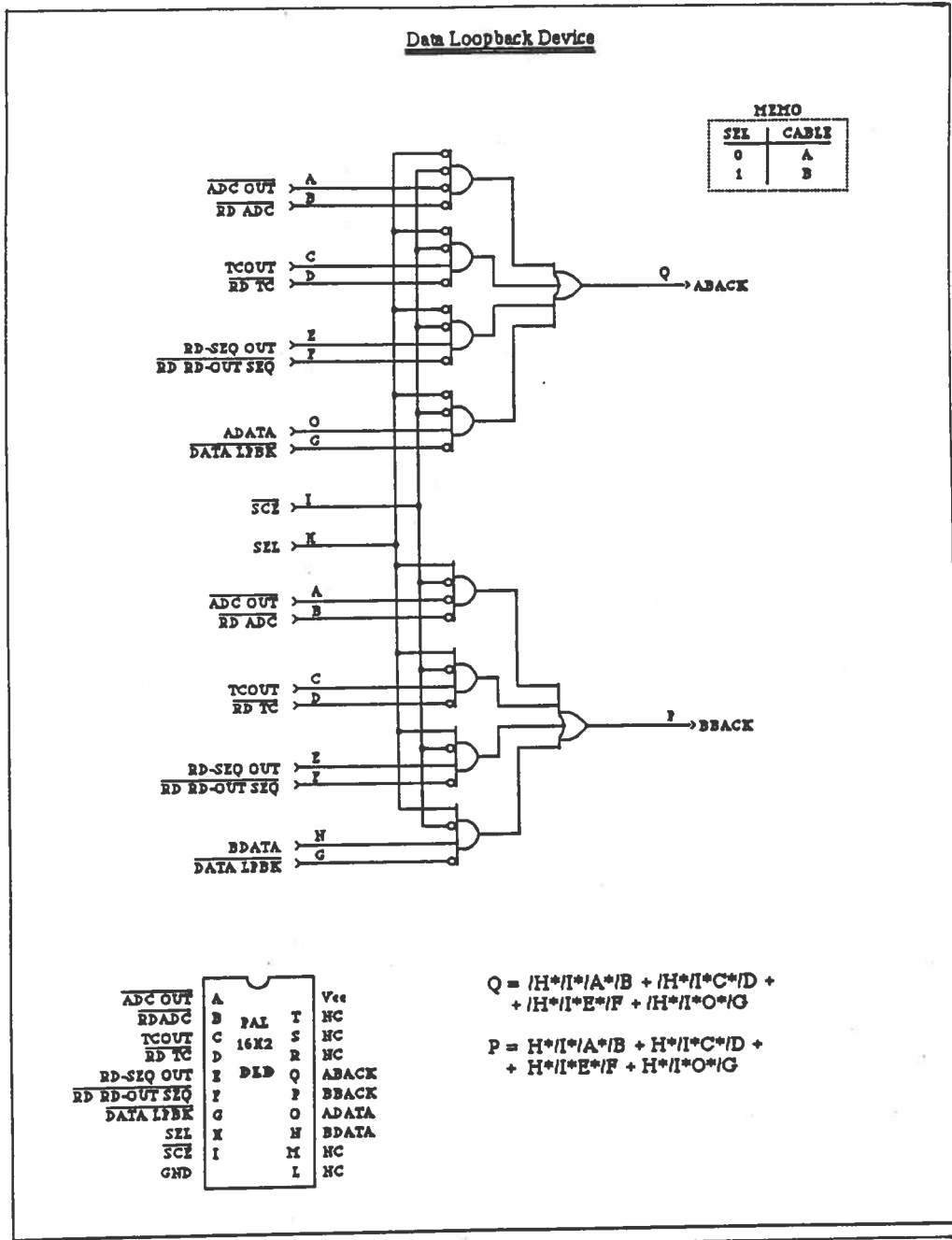


FIG. 13 - Data Loopback Device pal specification. 13a) - TTL/Optical transducers 0-16 MHz.

5. - Conclusion and Acknowledgments

A controller unit has been designed for the WIC readout at the SLD. The module will be used for data collection and control function. The design of the module is completed and a first prototype is under test. We would like to thank D. Toniolo, D. Sherden and S. Centro for helpful discussions and suggestions during the design.

Command Directory

DATA LOOPBACK (opcode 1) secondary

This causes the Splitter Board to go in loopback mode. Bits following the command are sent back to the TCM. The SB stays in this mode until another command is received.

SET ADDRESS (opcode 2) primary

Enables the specified SB to receive secondary commands. At the end of the opcode 8 bits of data are necessary to addressing.

RESET ADDRESS (opcode 3) primary

Disables the specified SB to receive secondary commands. At the end of the opcode 8 bits of data are necessary for addressing.

SELECT ME (opcode 4) primary

Select the communication line for all the SBs with the TCM. The selected line (A or B) is through which the command arrives.

CLEAR FLAGS (opcode 8) secondary

Clears the control flags of the LOAD, REFRESH, and COSMIC TRIGGER signals.

LOAD READOUT SEQUENCE (opcode 9) secondary

Fills the table with 8 bit words:

- a) D3-D0 number of SGS boards in the specified plane
- b) D7-D4 plane number

LOAD TRIGGER CONFIGURATION (opcode 10) secondary

Loads 24 bits:

- a) 10 to fix the selected planes
- b) 10 to fix the planes which must to be present
- c) 4 to fix the majority logic level.

READ TRIGGER AND FLAGS CONFIGURATION (opcode 11) secondary

Reads the 24 bits written in the Trigger Configuration Register and the Control Flag Register.

LOAD DACs (opcode 12) secondary

Writes the desired thresholds in the DACs.

READ ADC (opcode 13) secondary

Reads Vdacs, power supplies and Vref trough an ADC>

SHORT GATE RUN (opcode 14) primary

Set to 0 the gate line on the daisy chains, activates the LOAD-REFRESH sequence and resets the read-out system.

LONG GATE RUN (opcode 15) primary

Sets to 1 the gate line on the daisy chains, activates the LOAD-REFRESH sequence and resets the read-out system.

References

- [1] D. Sherden : SLAC-PUB-429 (1987).
- [2] SLD Design Project: SLAC-Report-273 (1984).
- [3] F. Beconcini et al.: INFN/TC-86/17 (1986).
- [4] S. MacKenzie, SLD LAC Timing unit, SLD internal note (1987).
- [5] G.M. Bilei and R. Castaldi: A Fastbus Digital Readout Module for Streamer Tubes, Presented to IEEE Nuclear Science Symposium, S. Francisco (USA), October (1987).