ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Milano

INFN/TC-87/7

12 Giugno 1987

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BIG - a BInary Generator

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ABSTRACT

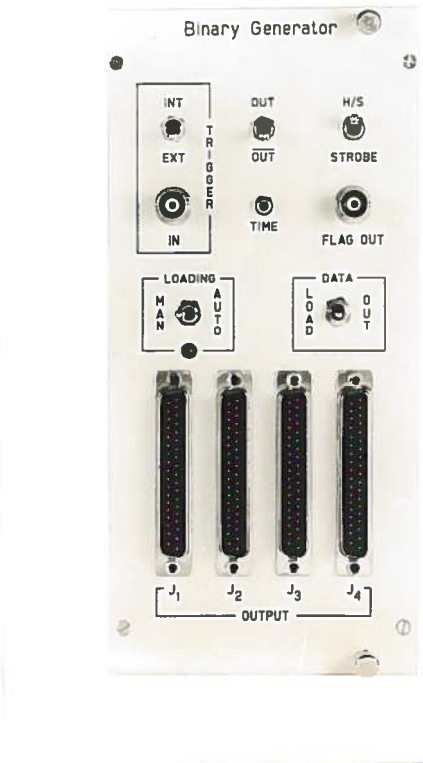
This paper describes a new kind of apparatus, able to present in output four arrays of digital data each long up to 2048 12-bit words.
The data are transmitted to the apparatus by a host computer, through a RS232C port and fill its memory. This, later, can be repetitively read, with a frequency up to 1 MHz, and the digital data can be used to test special peripherals.
The apparatus can also work with a proper hand-shake or can present the data together with a particular signal to allow the peripheral to accept them.

1.- INTRODUCTION

The problem to test digital circuits is more complicated than the testing of analog ones.
In fact to test an analog circuit can be enough an usual voltage generator, at least to obtain a rough idea of its real performance.
The testing of digital circuit, otherwise, depends on the number, not only of words, but also of bits we need, on the kind of words (integer, floating, simple or double precision, and so on) and specially on the frequencies we need to submit data to the circuit. For these last reasons we can't use a standard serial interface (RS232C), because of its not adequate transmission speed and procedure.
From an other point of view, with standard interface we are not able to validate also the particular handshake chosen for the circuit under test.
For these reasons to test an Advanced Microprogrammed Data Acquisition System, AMDAS [1], and in general different kind of special peripheral and digital circuits, we have designed, built and tested BIG, a BInary Generator, able to present, repetitively in output, four arrays of 12-bit words, long up to 2048, with a frequency up to 1 MHz.
Its general structure is described in section 2). The 3rd section reports the experimental results obtained.

2.- GENERAL STRUCTURE

Observing the front panel (Fig.1a, besides Fig. 1b shows the component side), we can summarize the general architecture of BIG. The generator has an internal trigger at 153 kHz, otherwise the option is for an external one, with allowed frequencies up to 1 MHz. Two complementary digital output representations (OUT & $\overline{OUT}$) allow to satisfy the peripheral requirements.
Two are the communication procedure, handshake or valid data signal (STROBE). In this last case the signal width is adjustable by means of the TIME potentiometer.
The FLAG OUT connector allows to control the correct timing of the communication procedure.
If the LOADING of the words into the memory is MANual, we need to start the reading process in the peripheral, also to store the data into the memory. Otherwise AUTOmatically the data are loaded and can successively flow through the output, independently of the peripheral status.
J1 to J4 are four standard 37 pin OUTPUT connectors, each carrying the communication procedure and the data.
The BIG memory consists of 2048 locations, each 48-bit long.



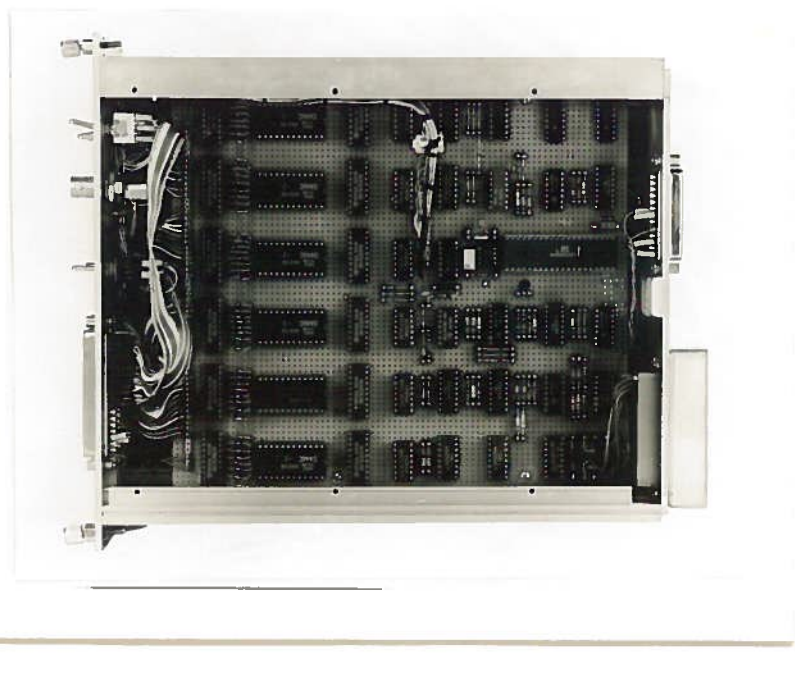


Fig.s 1

a): the front panel b): the component side

It is filled through a RS232C port at 9.6 kBaud with the data received from the host computer. Later it can be read at a fixed or variable frequency. The data sent through the serial line are ASCII coded and the communication procedure uses the Transmit-data, Receive-data, Data-terminal-ready signals.
BIG, among all ASCII characters, recognizes and decodes only the numerical (0-7) ones and the slash (/), used as string terminator.
To write in the BIG memory arrays shorter than 2048, it is sufficient to close the transmission with a double slash (//). These characters are interpreted by BIG as a string of all one or zero (depending on the chosen representation $\overline{\text{OUT}}$ or OUT), and are used as terminator of the writing operation. During the reading, obviously, the same condition is interpreted as an erasing signal for the address counter. In this way the memory content can be continuously read, avoiding the necessity of the refreshing. As previously seen, the BIG memory can be read with a fixed 153 kHz or with a variable frequency (external trigger) up to 1 MHz. This means each BIG 48-bit word goes-out every 1 μs, i.e. the reading speed can reach the 48 Mbit/s.

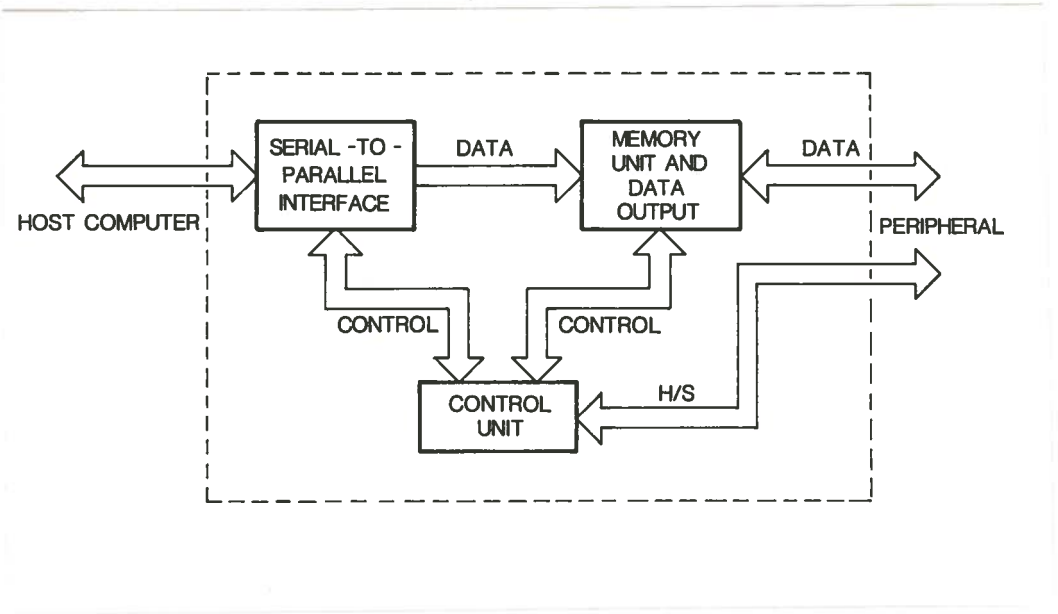


Fig. 2: Simplified block diagram

We have used BIG connected to an auxiliary port of a video-terminal together with the VAX-8600 computer of the Sezione di Milano (obviously, any kind of host computer can be used). In any case, the apparatus is activated, during the memory filling, by the operator. The data received from the host computer are displayed on the screen and contemporary stored in the BIG memory through the auxiliary port.
In this way we can use different codes to generate the usefull arrays, or otherwise we can transmit true data previously collected and stored. Because the BIG memory is made of 48-bit locations and each character (octal number) consists of three significant bits, we need 16 characters to fill each location. Besides, using the slash character we can send a smaller number of characters because BIG provides to set at zero the non interested bit of the location. In this way, during the memory reading we can obtain quadruplets, triplets, pairs or simply 12-bit words. On the other hand, a 'long' word, up to 48-bit, can be displayed if necessary. Another possibility concern, as already seen, the communication procedure. BIG, in fact, can work in two different ways: in the first, the chosen handshake is generated by the control unit; in the second the data are presented together with a valid data signal, of adjustable length.
We can describe the general structure of BIG following Fig.2, where it is subdivided in three sections:
1) serial-to-parallel interface
2) memory and data output
3) control unit.

2.1. - Serial-to-parallel interface

As shown in Fig.3, this section consists of three parts.
The first is essentially an UART (CDP 1854), which receives from the host computer the ASCII characters and transforms them in parallel words.
In the second (Character Identifier) these words can be interpreted as octal values (0-7) -and converted in a 3-digit binary string- or as the control character (slash). All other characters are ignored. In the third part, the binary strings are run through the Representation Selector until the slash character is recognized. Anyway, independently of the number of words in input, after it, the internal bus is always 48-bit long.
Following the details of Fig. 3, the control unit sends the clock signal to the UART, which, received the ASCII words from the host computer, transmits the 7-bit codes to the Character Identifier. When this recognizes a number, the corresponding digits are transmitted to the Representation Selector, enabled by a proper "number identified" flag. Otherwise, when one slash code is recognized, the control unit is enabled to start the character storage into the memory registers.
The Representation Selector is used to provide complementary outputs (OUT & $\overline{\text{OUT}}$) of 48-bit strings. To reach the first goal 8-bit parallel--to-serial converters, which provide both assertion and negation outputs, are used. For the second one, the serial data enter serial-in-parallel-out shift registers, to obtain the 48-bit string in the chosen logical representation.

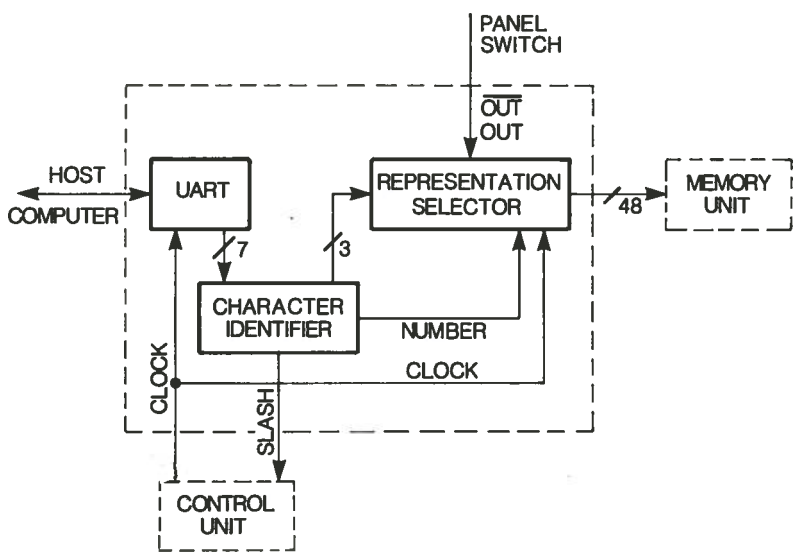


Fig. 3: Serial-to-parallel interface

2.2 Memory and data output

A memory of 2048 48-bit locations (Fig. 4) is filled with the parallel data coming from the previous section. The addresses and the writing and reading commands come from the control unit.
The End of Data Identifier recognizes the all zero or one 48-bit strings as end of the filled memory and enables a proper flag in the control unit.
The 3-state line driver is enabled by the panel Loading switch to send the data to the output connectors.
The data bus in this section is unique and connects all the three blocks and one external section (serial-to-parallel interface).
When the latter sends the 48-bit data, the 2K-memory data-bus is locked in 3-state and the string can be written in the memory registers.
During the memory reading cycle the output lines of the serial-to-parallel interface are in 3-state, so that the data stored into the memory can reach the other two blocks of this section.

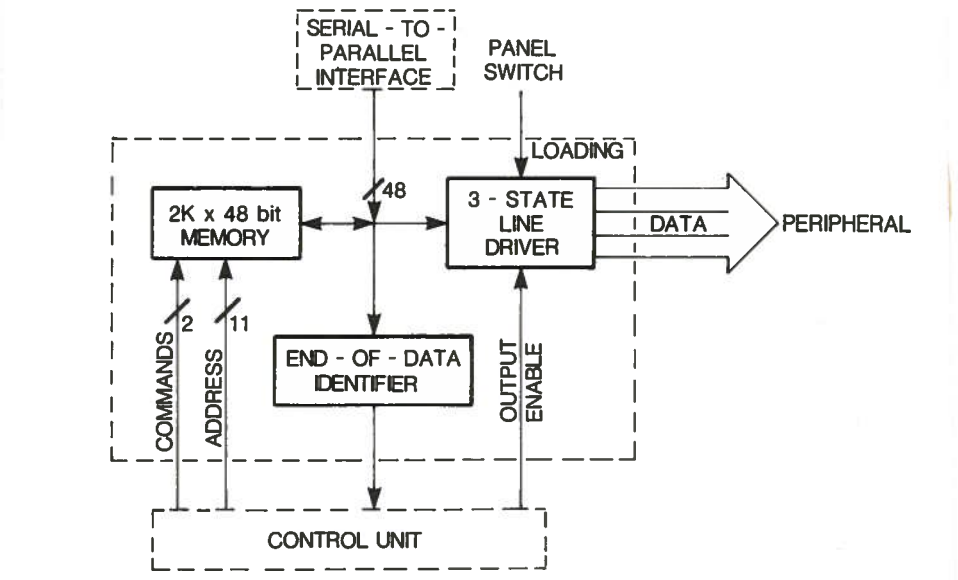


Fig. 4: Memory and data output

2.3 Control unit

The control unit (Fig. 5) consists of three parts. The first provides the clock signal for the UART (153 kHz), necessary to assure the right reception speed (9600 Baud), and the choice for the memory reading clock, which depends on the TRIGGER switch.
The memory reading cycle happens when the DATA switch is at the OUT position. The address generator increases the proper counter at the chosen frequency, when the peripheral has acquired the addressed data.

Then, the address increment signal, the memory reading signals -which puts at high impedence the serial-to-parallel interface data bus-, and the signal informing the peripheral about the new data , are generated.
When the address value is higher than 2048, or the memory location content is a 48-bit string of all zero or one, the address counter is erased, and a new reading cycle begins automatically.
With the DATA switch at the LOAD position, the signal exchange with the peripheral is stopped, and the UART starts the character reception.
When the slash character is recognized by the serial-to-parallel interface, the control unit lets the memory to write the received characters, temporarily stopping the new character reception, increasing the address counter and allowing to write again into the memory.
When the received characters are a double slash (//) or all zero or one, a string of all zero or one is written and the counter is erased.
This condition happens also when the address counter value is greater than 2048, in case of wrong transmission (array too long).

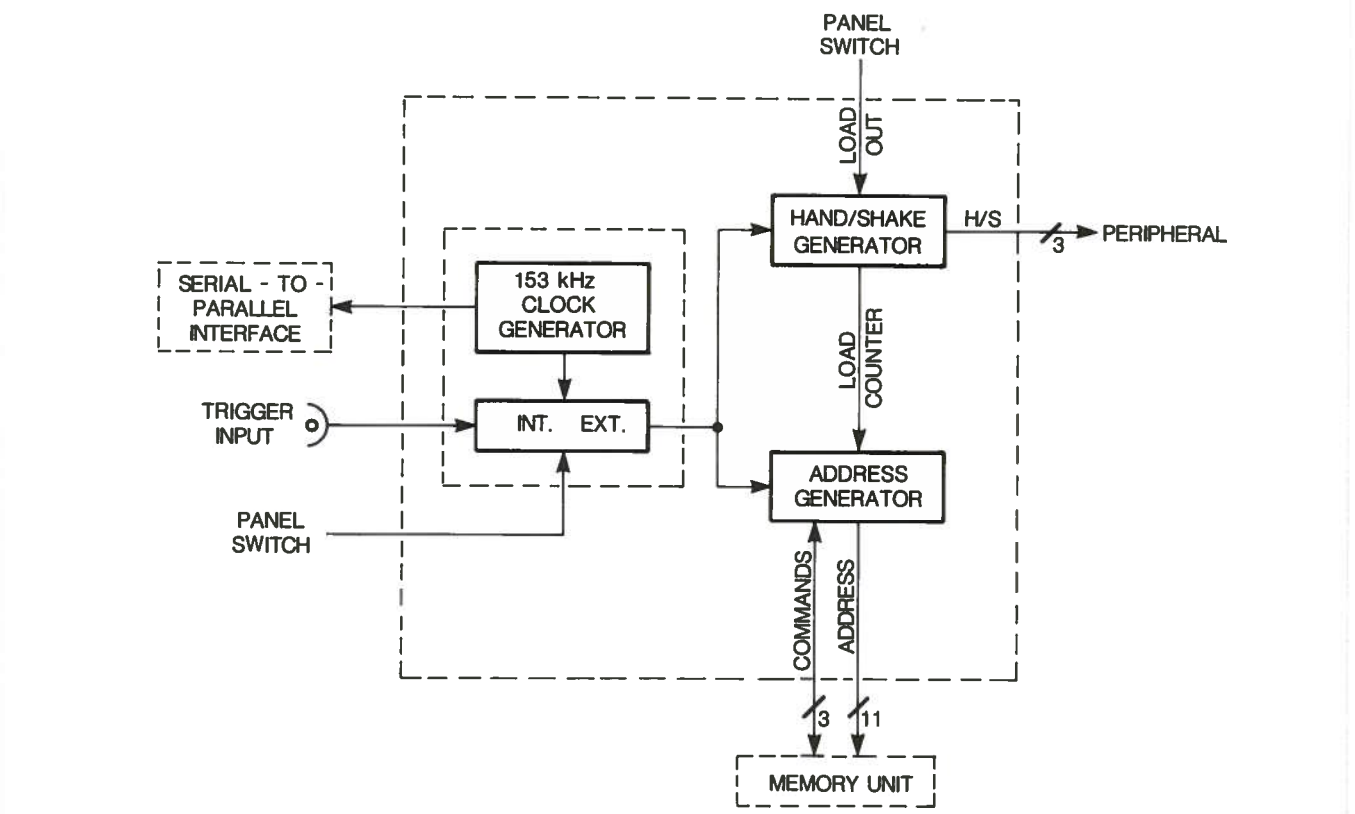


Fig. 5: Control unit

2.4 Working mode

The using procedure of BIG is very simple. We can create a data table, up to four columns and up to 2048 rows, in the host computer memory, in octal code. Once connected BIG to the auxiliary port of the video-terminal (set at 9.6 KBaud) and to the peripheral, we can type the matrix on the terminal, with the auxiliary port enabled. In this way the data coming from the host computer are visualized on the screen and fill, through the port, the BIG memory.

During this operation the BIG switches have to be: TRIGGER INT or EXT, indifferently, OUT or $\overline{\text{OUT}}$, depending on the peripheral characteristics, H/S, AUTO LOADING, and DATA LOAD. We have to remember that the DATA three-position-switch in the intermediate position realizes the address counter clearing. During the memory filling the online lamp of the keyboard can flash because of the rate of the communication procedure.

When the memory is filled, we can begin to use BIG. In this case, the switches have to be: DATA OUT, MAN or AUTO LOADING, INT or EXT TRIGGER, depending on the chosen frequency, H/S or STROBE, -depending on the peripheral requirements-. The OUT-switch has to be in the same position as in the filling. Also, during this cycle the DATA switch in the intermediate position lets to erase the address counter and to begin from the first position the memory reading.

3.- EXPERIMENTAL RESULTS

BIG was tested to verify its general architecture and to validate its behaviour in the digital circuit testing.

In fact, thinking about the role of BIG as an apparatus necessary to test different peripherals in conditions as close as possible to the experimental ones, it was necessary to be sure of its reliability in regard not only to the adopted structure, but also to peripheral validation. We verified the BIG performance with a Multichannel Analyzer (MCA) Silena mod CATO[2], directly connected, using a partial memory extension (2048 channels). In this way was possible to test one or two outputs at time, to control the right working mode of the memory blocks and of the address generator. The data used were different: a straight line, (0001 the first word, 0002 the second, 0003 the third, and so on, up to 4000_8), or an increasing ramp, ranging from 1 to 64 -100_8- (the word 0001 one time, the 0002 two times,..., the last one 64 times) or a decreasing one (the word 0001 64 times, the 0002 63 times, and so on),(see Fig.s 6).

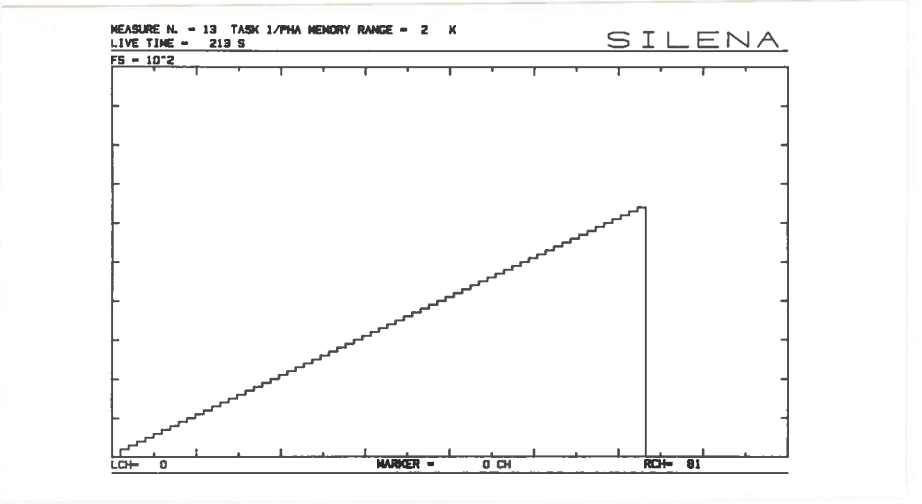


Fig. 6a: The increasing ramp obtained from BIG

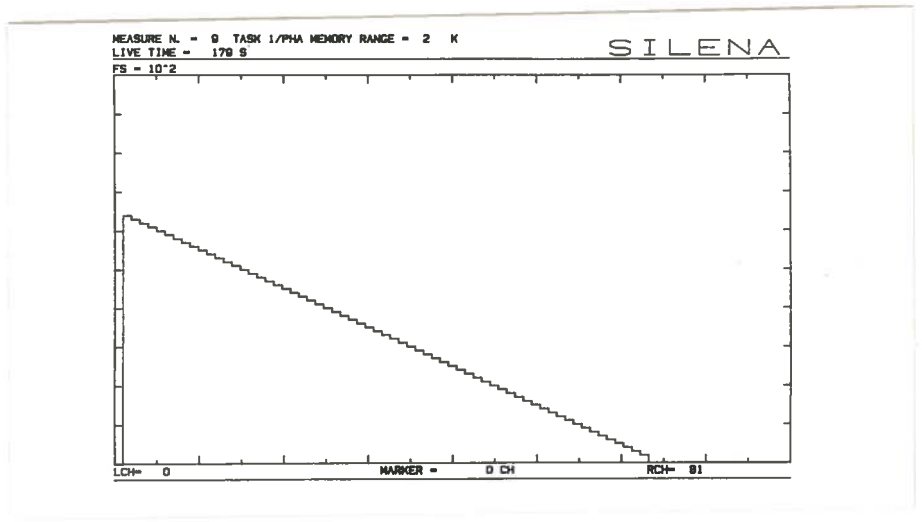


Fig. 6b: The decreasing one

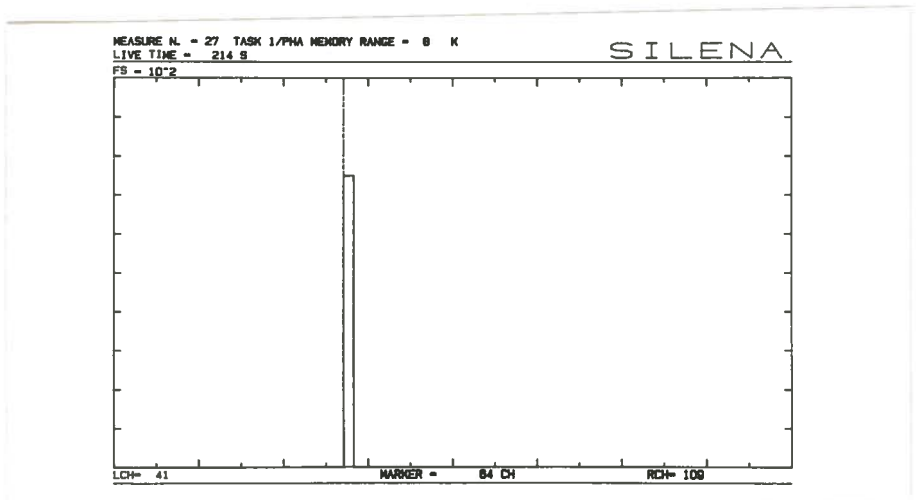


Fig. 7: The plotting of AMDAS output showing a constant value as result of the addition of the ramps of Fig.s 6

The second set of tests was addressed to verify the utility of BIG in the validation of peripherals.
In Fig. 7 is shown one of the result obtained with AMDAS, the apparatus previously referred. In this case, AMDAS added the two ramps of Fig.s 6 in input, obtaining as result the constant value of Fig. 7. In this way the effective coincidence of the two outputs of BIG was assured, independently of the frequency of repetition.

AKNOWLEDGMENTS

We wish to thank Mr. G. Tettamanti (*) for the accurate mounting of the apparatus and for the help given to us during the electronic test.

This work was partially supported by a grant of Italian Ministry of Education.

REFERENCES

(1) M. Annunziata, P. Guazzoni, L. Lisca, G. Sechi, L. Zetta
Microprocessing and Microprogramming 18 (1986) 515
(2) CATO - Multichannel Analyzer: User Guide and Electrical Schemes
Ditta Silena - Cernusco S/N - Milano - Italy

(*) Ditta Ascom - Milano - Italy