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**I. D'Antone, G. Mandrioli, L. Marradi and G. Sanzani:
AN INTELLIGENT VME-CAMAC INTERFACE CBA**

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AN INTELLIGENT VME-CAMAC INTERFACE

CBA

(I.D'Antone, G.Mandrioli, L.Marradi, G.Sanzani)

ABSTRACT

A dedicated VME module for the acquisition of a CAMAC branch was developed at the Bologna INFN Electronic Laboratory. It is an intelligent slave module that contains a 68000 CPU, handles the interrupts coming from a CAMAC branch and stores the readout data into a dual-port memory. The 68000 unloads the system processor in the VME from the CAMAC controlling tasks.

1. -INTRODUCTION.

A dedicated VME module for the acquisition of a CAMAC branch (CBA: Acquisition Branch Controller) was developed at the Bologna INFN laboratory. It is seen from the VME bus as an intelligent slave module. The task of this module, which contains a 68000 CPU, is the handling of the interrupts coming from the CAMAC branch and the storing of the readout data into a dual-port memory, using an internal bus. In this way the data readout functions are separated and overlapped in time with the CPU master activity. Furthermore many CBA could be present at the same time in the master crate without having the VME bus busy.

2. -GENERAL CHARACTERISTICS.

The CBA is made up of three main parts: a 68000 CPU, a CAMAC interface and a dual-port memory. Its block diagram is shown in fig. 1. The total amount of memory is 256 Kbytes and allows the storing of events and programs for data treatment. The CBA has a status register to enable interrupts or to read status signals coming from the CAMAC branch. It is 2 slot VME wide (see fig. 2).

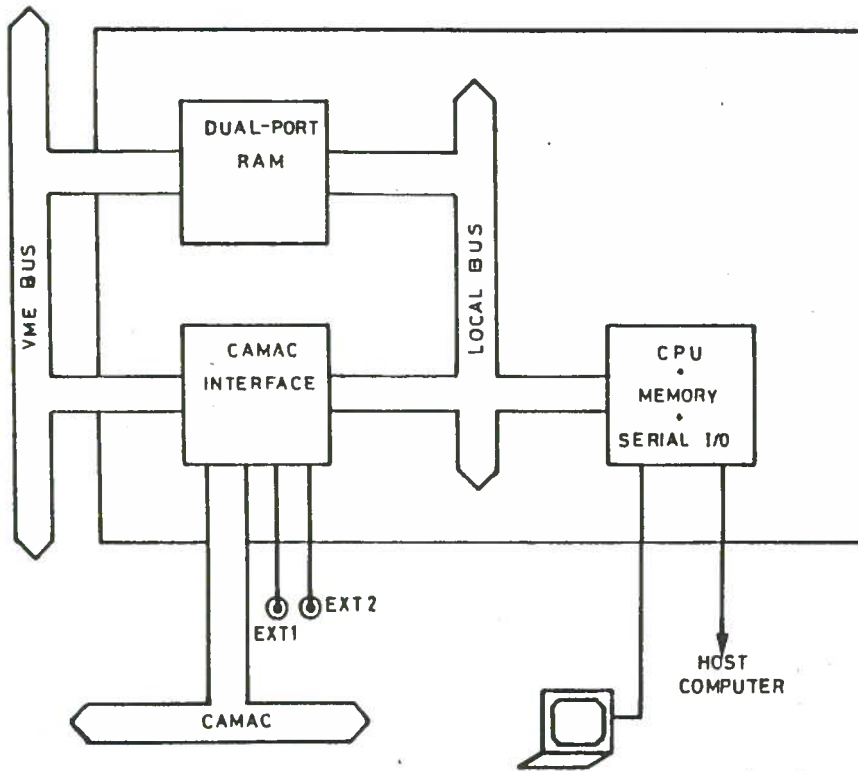


Fig. 1 - CBA block diagram.

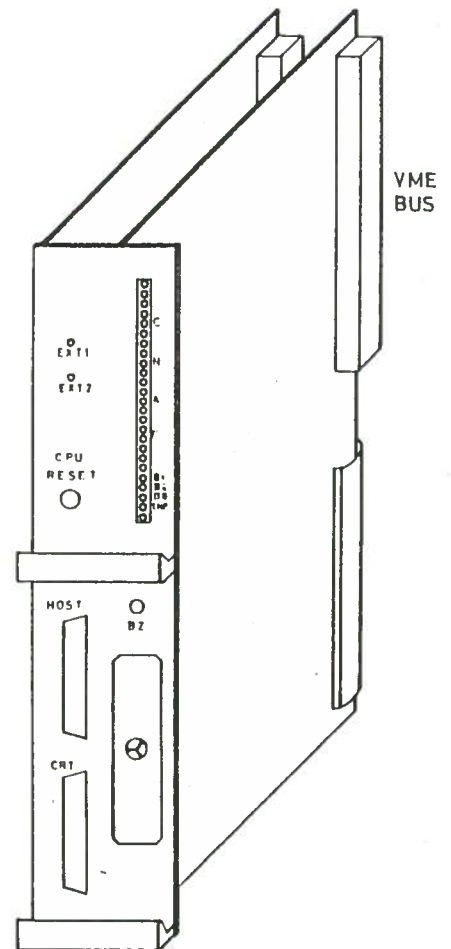


Fig. 2 - CBA.

A manual Branch Z is available on the front-panel. A set of LEDs monitors all the important CAMAC parameters driven by the CBA; crate number, encoded N, encoded A, encoded F, BX status, BQ status addressed by the last CAMAC command are displayed. Besides the branch BD signal in transparent mode and ENBD signal of the status register are monitored.

2.1. - The CPU board.

The CPU board is composed of:

- 68000 microprocessor in the 8 MHz version;
- 64 kbytes of local static RAM memory;
- 128 kbytes of dual port static memory;
- 64 kbytes of EPROM memory which contains a monitor, CAMAC ESONE routines, readout interrupt routines and the intercommunication task running in parallel with the master CPU user acquisition program;
- the necessary logic for handling the interrupts to the 68000 microprocessor;
- the chips for the decoding of the addresses;
- a time-out generator responding after 2 msec to lack of DTACK* (Data acknowledge of the 68000).

- 2 serial RS232 ports, on the front panel, working at any speed from 1200 to 9600 baud.
A block diagram is shown in the fig. 4.

2.2. - The memory.

The CBA has 64 kbytes of EPROM memory addressed from 0 to 0FFFF from the 68000. The local static memory is addressed from 10000 to 1FFFF. The dual-port memory is addressed in the range 40000 to 5FFFF from the 68000 and may be accessed from the VME bus at a base address configurable by switches. The complete memory table is shown in fig. 3. The block diagram of the dual-port memory is in fig.5.

Once the arbitration circuit has selected the processor which is allowed to access the DPM (Dual-Port Memory), the other processor waits and cannot gain access to the DPM until the first processor has completed its bus cycle. The local access has a higher priority than the VME access. The logic gates in the arbitration circuit allow the use of the TAS (Test and set) instruction that executes a read/modify/write cycle and simplifies support of the dual-port memory semaphore register.

2.3. - Interrupts.

The BD signal coming from CAMAC branch, if enabled, is converted in a vectorized interrupt to the 68000. Besides two suitable bits of the status register (EXT1 and EXT2 bits) produce two signals that are directed to the front panel. To send these signals as interrupts to the VME an external interrupt vector generator has to be used. We have developed an Interrupt Vector Generator (IVG VME module) that is a transparent software module that generates interrupts to the VME when it is given a TTL signal in input. The interrupt level is switch selectable.

2.4. - CAMAC Interface

The 68000-CAMAC interface transforms the address sent by the microprocessor into a Camac address following the specification given by CERN in the report "CERN Implementation Recommendations for M68000 based CAMAC controllers, EM Rimmer, DD, May 1983". The 24 bits address is coded in the following way, where B, C, N, A, F are respectively the Branch, Crate, Station, Address and Function.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	B		C		N			A		F			L/W									

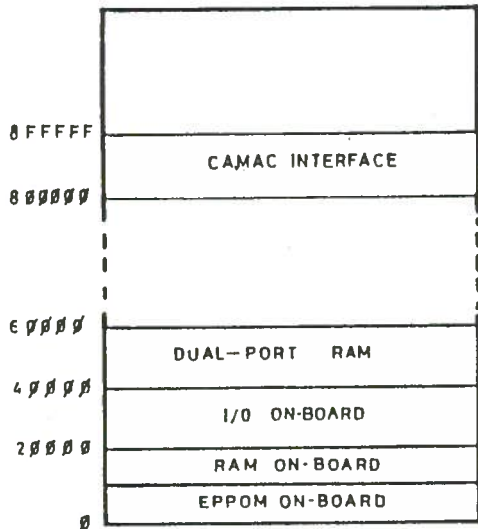


Fig. 3 - CBA address map.

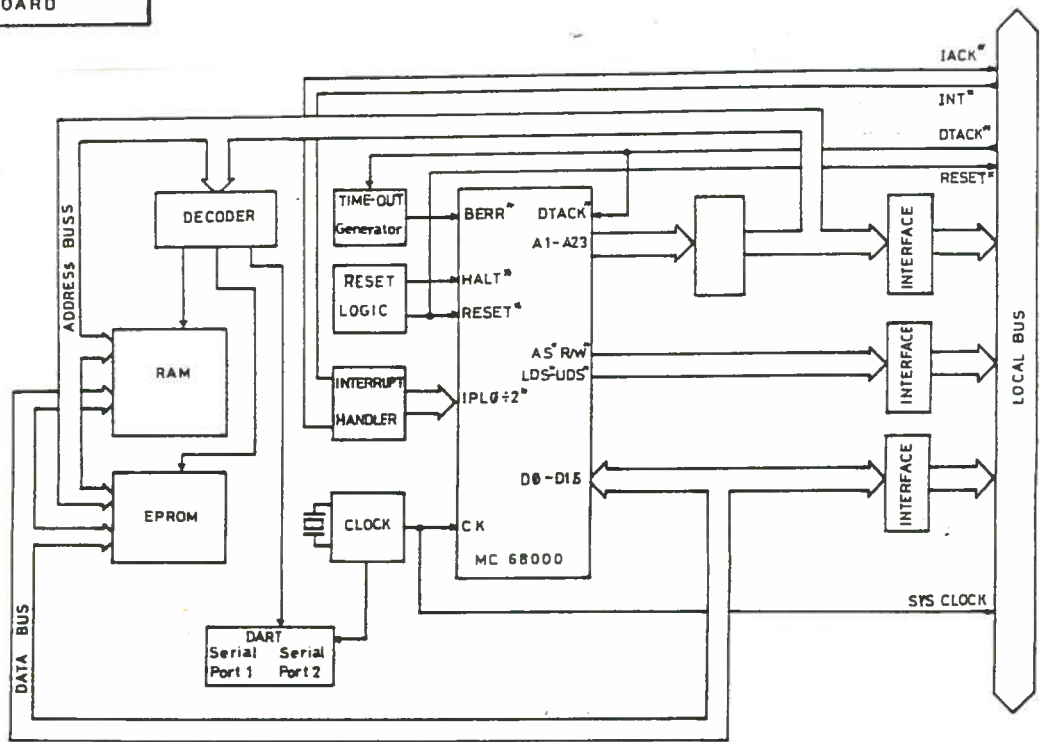


Fig. 4 - CPU block diagram.

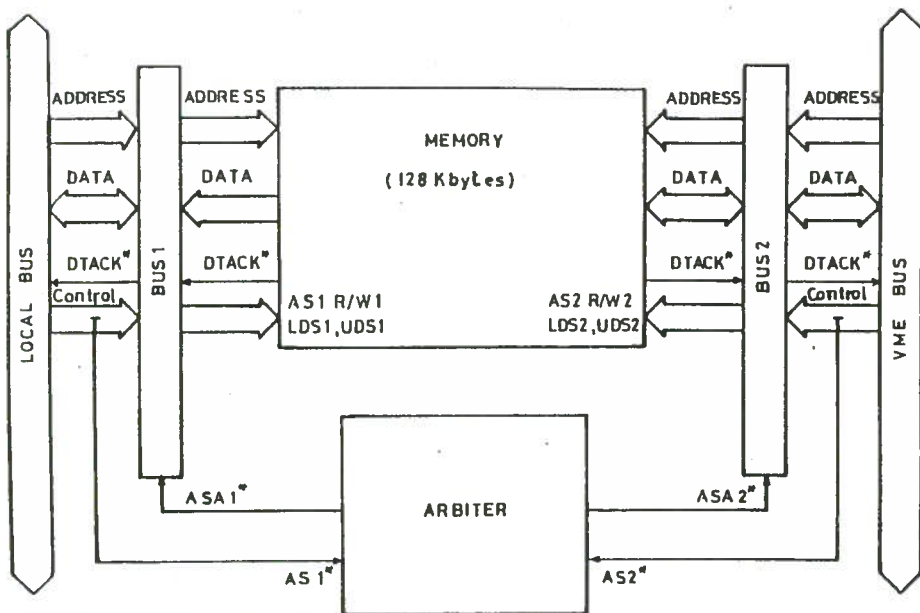


Fig. 5 - Dual-port memory block diagram.

Camac address space occupies only 1/64 of the total 16 Mbytes address space of the 68000 processor. The interface is connected through a Branch Highway Camac to a CCA2 crate controller and the data transfer is performed with a complete handshake between these modules (fig. 6 shows the minimum system). The Camac cycle is executed within a VME data transfer cycle. The block diagram is shown in fig. 7.

Fig. 8 shows the Camac Branch control signals in relation to the 68000 timing, for a long-word transfer cycle. The branch Camac cycle and the 68000 cycle are interleaved; two cycles are needed to read the 24 bits Camac.

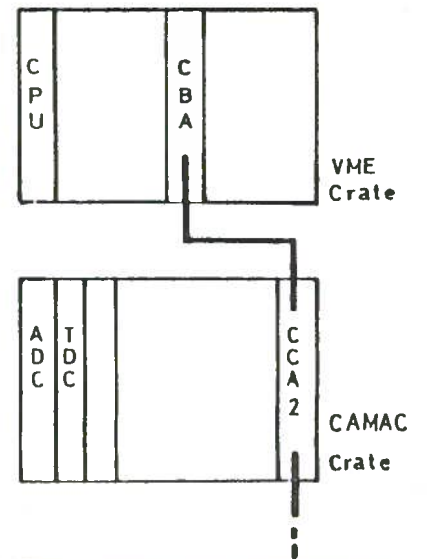


Fig. 6 - Sample system.

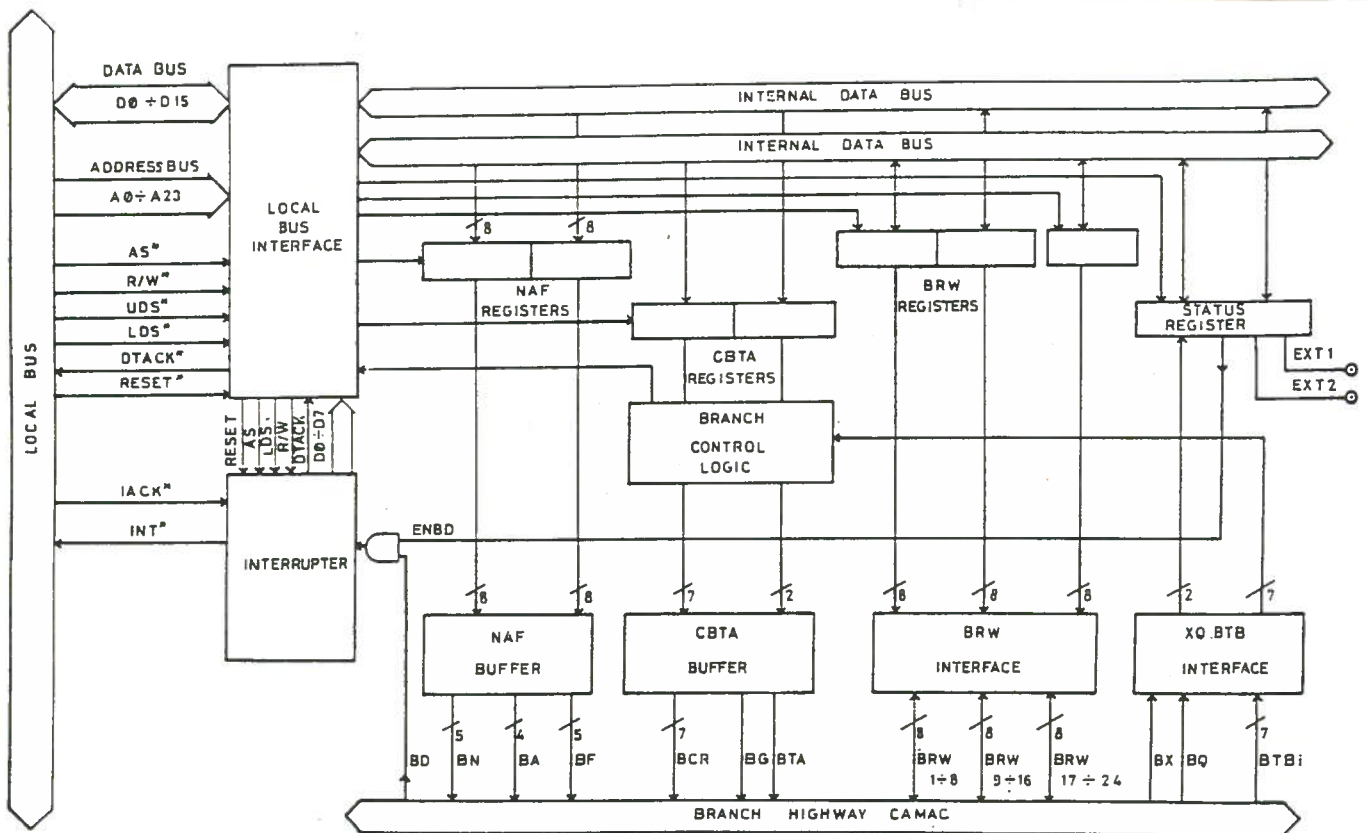


Fig. 7 - Local bus-CAMAC interface.

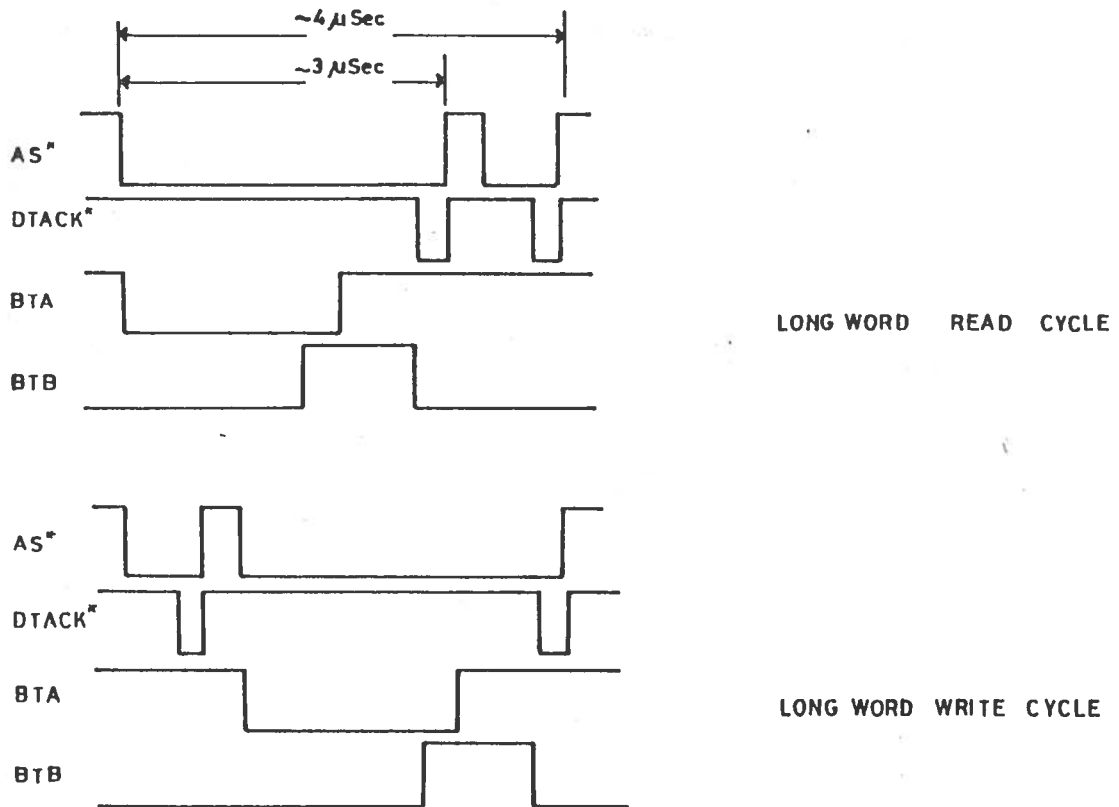


Fig. 8 - CAMAC branch control signals in relation to 68000 timing.

Using a Branch Highway of about two meters, the execution of a complete Camac cycle, that is the time from when the processor sends the address to the bus, up to the time when the interface gives the Data acknowledge signal to the processor, is about 3 μs for a 16 bits transfer and about 4μs for a 24 bits transfer.

3. -CBA FIRMWARE.

As stated the CBA allows a fast branch acquisition while a master VME CPU has the task of run control (initialization, Camac I/O list, etc..) and data handling (storing, histogramming, etc..). A protocol must be fixed for the messages exchange between the two CPUs. Being the CBA seen from the CPU master in the VME as a memory bank, it is possible a commands exchange by means of a mailbox.

We have written a simple CBA firmware that contains:

- a debug monitor with memory display, breakpoint setting and tracing;
- an intercommunication task that allows the messages exchange with the CPU master in the dual-port memory bank (see fig. 9);
- the service routines of the CAMAC interrupts and an essential CAMAC library. The interrupt routine simply performs a series of MOVE instructions (which transfer a word or a long-word from a Camac address to the CPU registers) and stores the data read into a circular buffer in the dual-port memory.

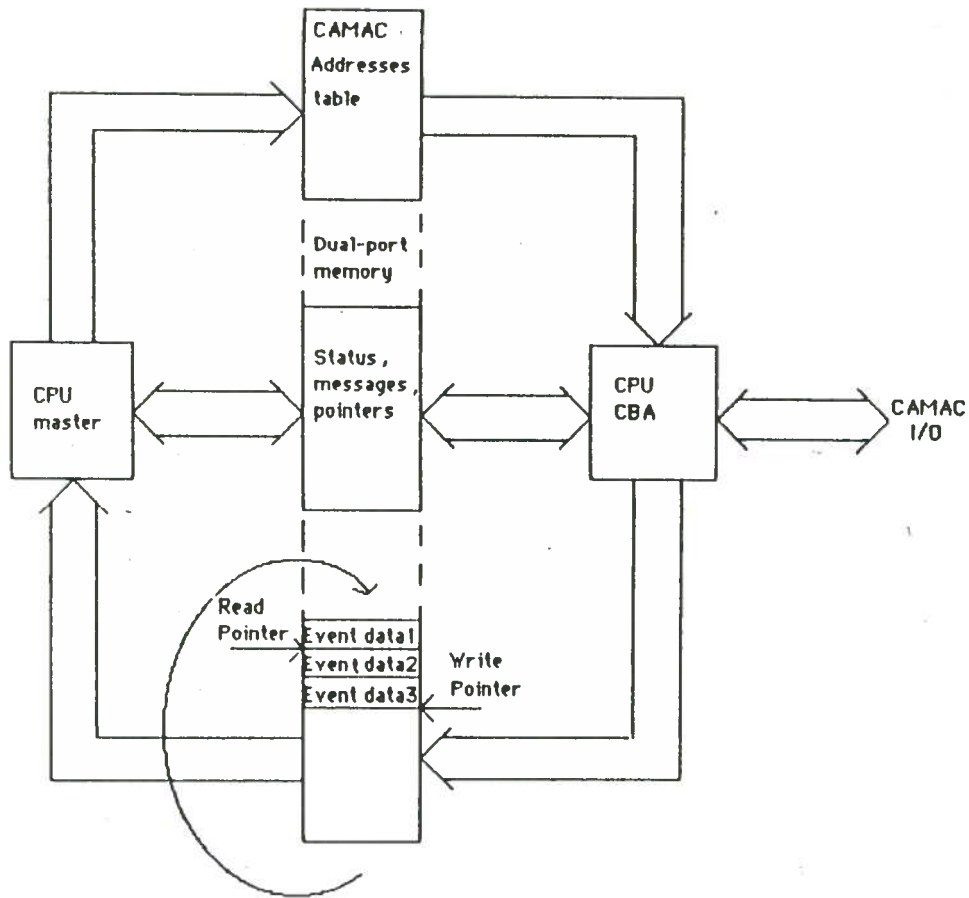


Fig. 9 - Block diagram of the intercommunication software.

This firmware can execute the readout of a branch Camac using a predefined Camac addresses table set by the CPU master according to the configuration of the current modules. In this way the readout proceeds at the highest speed possible.

Of course the master CPU must empty out the data buffer. For this reason the CPU in the CBA sends an interrupt to the VME bus when it completes the routine writing to the buffer.

4. -USAGE.

4.1. -Serial ports.

The 2 RS232 serial ports are initialized during Reset by monitor. Baud-rate is selectable (1200, 2400, 4800, 9600) by means of jumpers. The 2 25 pins CANNON connectors are located on the front panel. The first port may be connected to a terminal, the second to a host computer. The monitor has a command (TM) switching to transparent mode and allowing to work on the host computer.

4.2. -Memory.

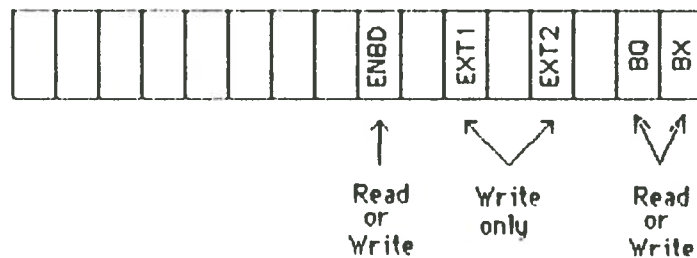
The base address of the memory seen from the VME is selectable by means of switches. Each of the VME bus address lines A17-A23 may be chosen to be low or high allowing any base address.

4.3. -Camac function execution.

To read or write a 16 bits word the MOVE.W instruction has to be used at an address following the specification in paragraph 2.4. To read or write a 24 bits word the MOVE.L instruction has to be used. When the Camac function does not imply data transfer (test functions) the TST instruction may be used. A switch must be positioned to indicate the Branch number.

4.4. -Status register.

The CBA has a 16 bits status register at the address 89E800, a pseudo-Camac address N29 A0 F0. The content of this register is the following:



ENBD: When this bit is set by the 68000, interrupts coming from the Camac branch (signal BD) are enabled

EXT1,EXT2: These bits produce a signal directed to the front-panel

BX,BQ: BX and BQ response

After a Camac function is executed one can know about the BQ and BX response reading the status register.

5.-AN APPLICATION.

In order to obtain a complete acquisition system that could be used in simple test runs, we have developed an acquisition program that runs on the master CPU of the crate containing a CBA. We have used an hardware configuration composed by a commercial VME board with 68000 CPU, a 5" 1/4 hard-disk with a commercial disk controller and a RAM board.

The software, written in assembler, is an interactive program allowing the control of the run.

It is composed of the following modules:

- SET UP: it allows the set of the branch CAMAC configuration (current crates and modules, active channels, LAM enabled, etc);
- MONITOR: it contains many commands to execute simple CAMAC operations, program tables display and so on;
- RUN: the purpose of this module is the reading of the circular buffer, the event handling and the data output in a predefined way (display on a terminal, output

through a serial port, storage on hard-disk and histograms display. All these activities proceed in parallel with the CBA acquisition activity;

OUTPUT: it contains the commands for the data output definition, the histograms parameters, etc.

This software allows, using standard modules (TDCs, ADCs, SCALERS, etc), the acquisition of a CAMAC channel in less than 25 μ s in word mode. This time, which is calculated by dividing the execution time of the interrupt routine by the readout channels, depends on the number of instructions and on the controls executed by the CBA's service routine. In our program the interrupt routine contains checks on the CAMAC operation (X and Q response, LAM tests, etc) and the building of a logical event record.

In the system described the CPU master, that is the CPU having the software control of the acquisition, is in the VME crate. This master function may be also executed by an external CPU, provided a fast link with the VME crate is available. We have mounted and tested a system composed by a μ VAX linked with the VME crate by means of a parallel interface having a DMA transfer capability. In this way it is possible a direct transfer of the event-data from the CBA memory to the μ VAX.

6.-CONCLUSION.

We have developed a system able to read a Camac branch by means of an intelligent module in VME (CBA). The Camac interface of the CBA follows the CERN-Saclay standard of memory mapped CAMAC I/O in the VME bus.

An M68000 based acquisition software has been written for usage in stand-alone systems.

Acknowledgments

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