ISTITUTO NAZIONALE DI FISICA NUCLEARE

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MICRO-LEARN

A LOW COST MICROPROCESSOR DEVELOPMENT SYSTEM FOR LABORATORY USE BASED ON STD-BUS, Z-80 CPU AND CP/M OPERATING SYSTEM.

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ABSTRACT.

The MICRO-LEARN development system consists of two boards based on the STD-BUS: MICRO-LEARN CPU board based on the Z-80 microprocessor and MICRO-LEARN Disk Controller board.

The low cost of the boards and the modularity in hardware (STD-BUS) and in software (CP/M OPERATING SYSTEM) give the possibility to use these boards in a wide range of applications such as:

- Process control: automation, measuring devices, real time data acquisition, digital control of machine-tools, etc.
- Development system for Z-80 microprocessor.
- Instrumentation laboratory controlled by microprocessor (IEEE-488-1978).
- Portable stand-alone instrumentation.

1. - INTRODUCTION

We have developed these boards with the intent to give an easy and flexible means to the user to make data acquisition systems and to interface sensors, displays and motors or actuators in real time process control. In selecting the hardware and software standards, we have referred to the statistics given by "Datapro", "IC Master", "Micropro" and "IPI" which indicate that CP/M is the most used Operating System among the 8-bit microprocessors. Besides, more than one hundred firms from several countries are building boards based on the STD-BUS (1). All this means that a lot of tested, high quality software running under the CP/M Operating System, including "Drivers" for STD-BUS boards, has been written. Large software houses, like Digital Research, Microsoft, etc. have provided several languages under CP/M: Pascal, Assembler, Fortran, Basic, Lisp, Forth, Logo, Cobol, etc. as well as debuggers: (DDT, ZSID, etc.) and linkers: L80, MTLink etc.

Compared to the other CPUs available, the advantages are: low cost, versatility, multifuntionality, no need for custom components (e.i. Mostek and other CPUs have custom components) and easy repairability because the most standard components on the market have been used.

An examination of the field of 8-bit microprocessor applications has been made. From the data given by "DATAPRO", "IC MASTER", "MICROPRO" and "IPI" index catalogs in this field, the following classification can be extracted.

- Z-80 ZILOG. The most widely used microprocessor, in particular in Data acquisition, monitoring and industrial process control systems.
- 8085 INTEL. Has smaller instruction set but with a better interrupt capability respect to the Z-80. It was more popular in the past because it was on the market before the Z-80.
- 6502 MOS-TECHNOLOGY. By far the most popular among personal computers (Apple, Commodore, etc.)
- 6809 MOTOROLA. Less popular than the previous ones but certainly, among the 8-bit microprocessors, the one with the most powerful instruction set (which gives the possibility to generate good quality, low-cost relocatable assembly programs), best architecture and interrupt system (NMI, FIRQ, IRQ). Unfortunately the market doesn't offer as many development systems or as much application software and boards for industrial process

control as for the previous ones. (Used in a few personal computers: TRS-80, DRAGON, etc.).

Among the most popular operating systems for 8-bit microprocessors, there is CP/M that offers the following features: single user, device independence, spooling, multitasking, networking capability, minimum file size 0, maximum file size 256 Kbytes, maximum number of files on disk 64, record length 128 bytes, random access file accessability.

A large number of languages in either compiler and/or interpreter versions are available, among which: Assembler (8080, Z-80), APL, BASIC, FORTH, C, PASCAL, LISP, LOGO, PL/1, COBOL. Besides these, many other application programs (crossassemblers, debuggers) are available from many software houses, transportable on single or double density 5 1/4 or 8-inch floppy disks.

Other well known 8-bit operating systems are: UCSD-PASCAL (TM), OS-9 (TM) and FLEX (TM) for Motorola 6809, Dos 3.3 For Apple, MP/M that is like CP/M but with multi-user capability.

2. - POSSIBLE CONFIGURATIONS WITH THE CPU BOARD.

2.1. - Instruments controlled by microcomputer in an automatic test and experiments laboratory

In conjunction with a MICRO-LEARN Disk board and an IEEE-488-1978 interface board, several instruments equipped with IEEE-488 interface can be connected together and controlled remotely from the microprocessor.

Some instruments can be connected to the controller (CPU) as listeners (Receive data from the BUS). Examples are: printer, display, power supply, signal sources; up to 14 active at one time. Some could be connected as talkers (Transmit data onto the BUS), for example: voltmeters, digital oscilloscopes, counters, etc., (only one active at a time).

The official standard is IEEE-488-1978. Other names for the identical BUS are: HP-IB, GPIB, IEEE-BUS, ASCII-BUS, PLUS-BUS, IEC-BUS. More than 200 manufactures from 14 different countries are making over 1000 different instruments with the IEEE-488-1978 standard.

2.2. - Development system and stand alone CPU.

A microcomputer application makes use of a programmable IC (microprocessor) and very

little hardware to perform an almost infinite variety of very complex tasks by executing a sequence of program steps. An entirely different task can be performed with the same hardware by changing only the program.

A development system is a tool that gives a means :

- To write the program that performs a particular task.
- To test the program itself.
- To test the program in a particular enviroment through tracing, debugging and interacting with the specific hardware.
- To write in EPROM the final version of the tested program that performs the task.

A stand alone CPU is the hardware support for the program in EPROM generated by the development system.

The MICRO-LEARN CPU can perform both tasks, depending on which EPROM and RAM are installed. This yields the following advantages:

- easy to develop the software, because the basic enviroment is the same in the two cases: System CPU or User CPU.
- lower cost
- faster realization time. It is not necessary to design a new board for the application; at most only some special I/O like counters, interrupts, etc. need be added.

Among the many software tools available on the market under the CP/M operating system, the more suitable ones are:

- Assembler M80 (MICROSOFT)
- Linker L80 (MICROSOFT)
- Fortran F80 (MICROSOFT) offers double precision arithmetic routines
- Pascal MT+ (Digital Research) is a compiled version with the possibility to write overlaid programs in high level language and direct Z-80 machine code.
- LinkMT (Digital Research) is used to link relocatable object codes of modules, written in Assembler or Fortran, with Libraries.
- ZSID (Microsoft) is one of the best debuggers for all programs generated by the above tools. It allows to inspect and, if necessary, modify registers and memory contents. It permits single stepping of instructions and tracing of several instructions. It also allows breakpoint insertion and symbolic debugging (the user may use the same name for

variables and labels as in the source code).

2.3. - Didactical development system.

The CPU and DISK MICRO-LEARN boards along with a minidrive and the "Logidules" (cubic plastic modules containing prewired digital integrated circuits, developed at the Ecole Polythecnique Federal de Lausanne. EPFL) form a Didactical Development system that gives the possibility to the inexpert user to put hands on Digital-Logic and microprocessor interfaces.

It has been proved statistically that, on the average, most people remember 25 % of what they hear, 45 % of what they see and hear, and 70 % of what they see, hear and do practically. Many educational methods today try to involve the participants in the learning process, offering them some practical intervention (IVIS from DEC., IBM touch panel, etc.).

The personal computer is usually cheap, general-purpose, stand-alone, microprocessor-based and offers conversational interaction with the user. The user can profit from these systems to learn how to write programs using different languages, but they are not very useful (some of them are black-box inaccessible) to learn microprocessor interface techniques and digital logic.

The reason for having equipped the CPU board with the EPFL-BUS is meant to provide a means to teach hardware and low level software (assembler).

A simple microprocessor instruction "store accumulator to I/O device" (interface) in order to light up Logidule LEDs (registers and digital logic) gives a means to learn how to connect the microprocessor to the external world.

A great advantage in using the logidules, rather than connecting the integrated circuits directly on a proto-board, is that the set up of circuits can be done in a reliable way in a few minutes and without destroying many circuits through errors.

3. - MINIMUM DEVELOPMENT SYSTEM CONFIGURATION.

There could be several approaches in configuring a system. In all configurations, an alphanumerical terminal is needed.

The simplest is made of a CPU and an alphanumeric terminal. A simple monitor resident

on EPROM, with a few commands, gives the possibility to hand-code and execute simple programs.

The more advisable configuration is made of:

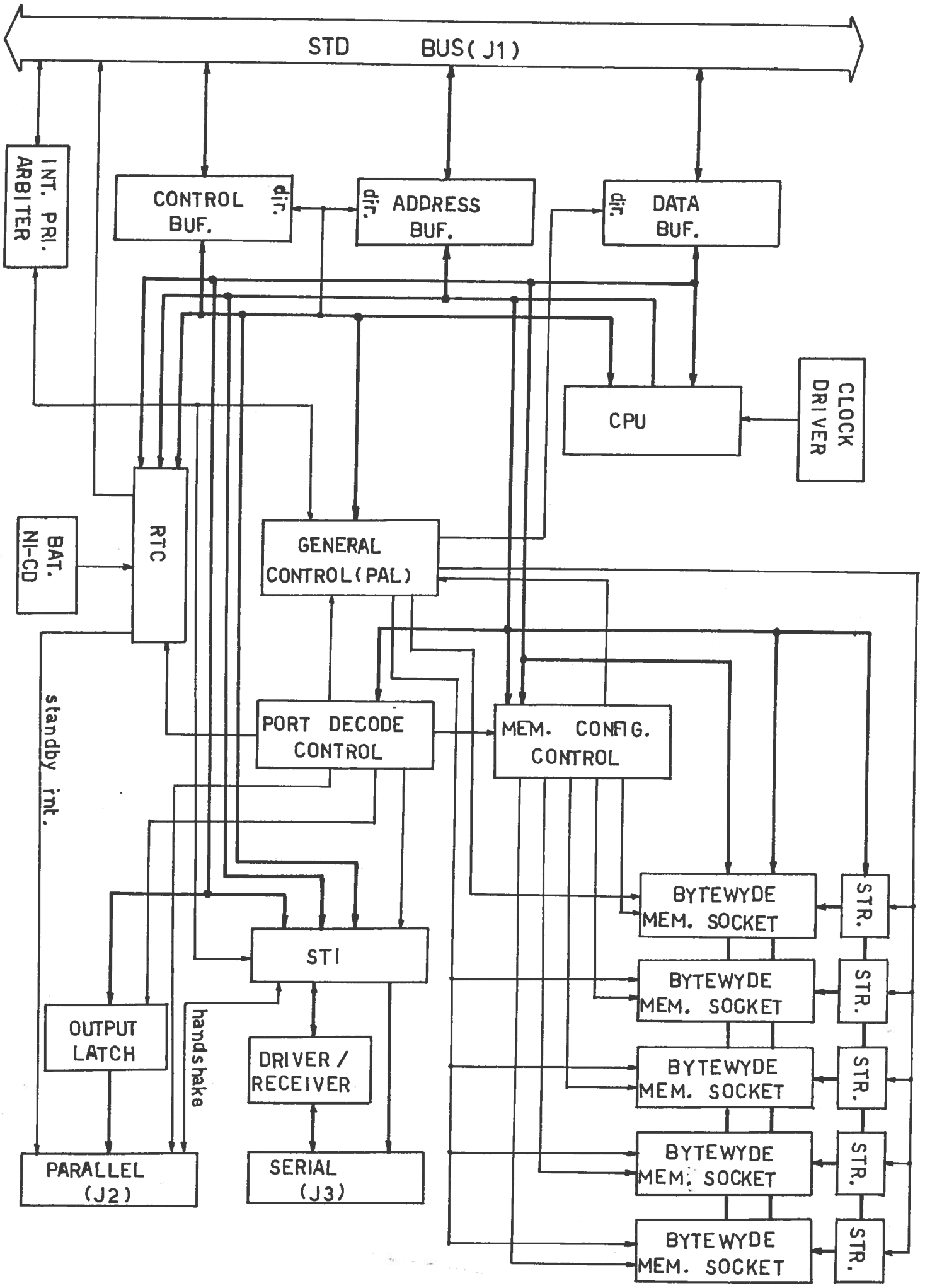
- Alphanumeric terminal with serial RS232-C port
- MICRO-LEARN CPU with 2K EPROM and 64K RAM
- MICRO-LEARN Disk board
- 2 floppy disk drives
- M80 ASSEMBLER (Microsoft)
- L80 LINKER (Microsoft)
- ZSID DEBUGGER (Microsoft)

Other configurations can include more floppy drives and/or Winchester disk drives also.

4. - CPU FEATURES

We now describe the CPU board which is illustrated in Fig. 1.

- STD-BUS compatible
- Five 28 pin sockets for industry standard BYTEWYDE (TM) ROMs, EPROMs or RAMs (one for ROM, four for RAM).
- Flexible memory decoding of RAM/ROM memory on any 4K boundary.
- Phantom ROM capability (see below).
- 32 Kbytes EPROM and 64 Kbytes of RAM (Maximum configuration Sept. 84').
- 128 Kbytes EPROM and 256 Kbytes of RAM (Maximum future configuration using the announced new memories with 28 pins: Hitachi HM65256P-20, 32768 * 8 Bit pseudo static RAM and Advanced Micro Devices AM27512, 65536 * 8 Bit EPROM).
- 8K of RAM memory (one level of socket A4) sustained for at least five days with fully charged batteries. (Ni-Cd rechargeable batteries).
- Supports memory bank switching to allow access to more than 64 Kbytes.
- Supports MEMEX (memory expand) capability as foreseen by STD-BUS.
- Real time clock calender having 2 interrupt outputs with 8 possible interrupt sources (10 Hz, 1Hz, once per minute, once per hour, once per day, once per week, once per month,



Fifure 1. BLOCK DIAGRAM OF CPU BOARD.

and when a real time counter register coincidence occurs). One of these is a standby interrupt by which the computer can turn itself on to do some acquisition or calculation and then turn itself off.

- Bidirectional address, data, and control busses to permit external DMA to on board-memory.
- 8-bit output port with handshake (Centronix printer interface).
- 8-bit output port, EPFL-BUS interface to "LOGIDULES". Joining several Logidules mechanically together (by their interlocks) and connecting them electrically (by their side contact springs or with cables) allows to test digital systems of any complexity. Power is automatically distributed by contact springs.
- Serial RS232-C I/O Port with full handshake (RTS/CTS).
- Bidirectional power-on reset allows operation with power-fail controllers.
- Two programmable 8-bit timers with offboard outputs.
- Fully buffered signals for system expandibility.
- Fully compatible with software running on Mostek boards CPU3 and CPU4.

5. - CPU DESCRIPTION

Very few gates are used in this board. Most of the control signals, in the block "General Control", are generated by the use of a PAL (Programmable Array Logic). Two 256 * 8 bits PROMS are then used, instead of decoders, for providing a very flexible memory map (MEM. CONFIG. CONTROL) and I/O map configuration (PORT DECODE CONTROL). This allows the RAM to be enable/disabled in 4 Kbyte increments and the ROM/EPROM to be mapped on 4K boundaries anywhere in the 64K memory map. There are 8 memory maps selectable; each different map is selected under software control. It supports also a memory bank (a bank corresponds to 64K of memory) operation which allows memory expansion beyond the normal 64 Kbytes limitation of the Z-80. A 64K bank out of the total system memory is selected by outputting a bank select byte to port FFH. The memory map configuration will then specify in which 4-Kbyte boundary will internally be organized each bank.

The use of this technique in memory decoding, gives not only a hardware flexibility by accepting several memories of several types and size, but it gives also programming

advantages by changing banks, maps and restart addresses and also by supporting the so-called Phantom ROM type of operation. In that operation, a ROM contains just enough code to bring a large operating system into RAM, from which by switching to another map, the ROM is disabled dynamically and operation begins in a purely RAM configuration. A method to do this is to have memory map 0 in the configuration PROM contain the boot-up map and then switch to the desired map configuration. The following procedure is then followed:

- copy the ROM/EPROM code into the RAM.
- switch to other maps by outputting a new map number to the memory configuration port (0FFH), allowing the copied code in RAM to be active.
- execution of the program will continue at the next intruction now in the RAM.

In the MICRO-LEARN system configuration, there is a 2 Kbyte 2716 EPROM in socket A3 containing a simple monitor and a boot program. At reset operation, system has memory map 0; the EPROM 2k code is copied to RAM address E000-E7FF; the memory map number is switched to 5; and execution of the program continues from RAM in a 64k RAM bank. The program then waits for a carriage return from the alphanumeric terminal, a routine with automatic baudrate determination sets automatically the timer of the serial I/O terminal. The program then checks if a Disk controller board is present on the STD-BUS; if so, it then boots the M/OS-80 operating system (CP/M compatible) into RAM, if not, the user may type a "." to enter the simple EPROM resident monitor.

6. - CPU HARDWARE

6.1. - Electrical specifications

SYSTEM CLOCK: 3.6864 MHz +/-0.05 %

OPERATING TEMPERATURE: 0 °C to 60 °C

POWER SUPPLY REQUIREMENTS:

+5 Volts @ 1.8 Amp max (excluding BYTEWYDE TM sockets)

+12 Volts @ 50 mA

-12 Volts @ 50 mA

6.2. - Mechanical specification

CARD DIMENSIONS

11.43 cm. wide by 16.51 cm. long

1.71 cm. maximum profile thickness

0.16 cm. printed circuit board thickness

6.3. - STD-BUS edge connector (J1)

56 pin dual readout; 0.317 cm. centers

6.4. - Serial I/O connector J3)

26 pin dual readout; 0.254 cm. grid

6.5. - Printer or EPFL-BUS connector (J2)

Same as Serial I/O Connector. On the same connector, depending on the jumpers selected on J9 (see Fig. 6a - 6b and 7a - 7b), a set of signals for the parallel printer or the EPFL-BUS can be brought out at the 26 pins.

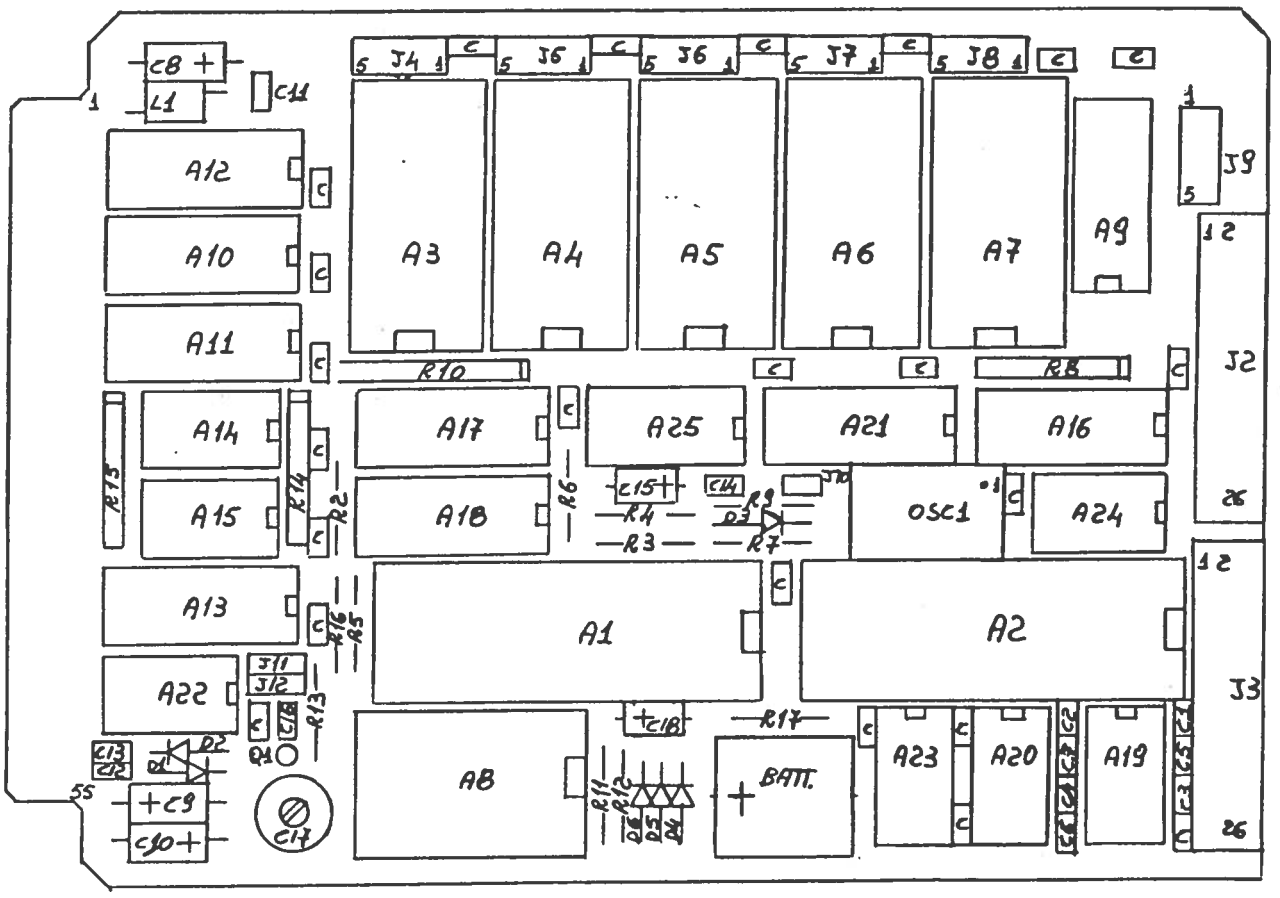


Figure 2. COMPONENTS AND JUMPERS CONNECTORS LAYOUT OF CPU BOARD.

6.6. - Custom MAP PROM connector (J10)

If it is desired to use a custom MAP PROM which uses all 8 memory maps, then J 10 must be installed.

6.7. - Test connector (J11)

This header is used for testing purposes only and is strapped (Pin 2-3).

6.8. - Interrupt connector (J12)

This connector enables the interrupt from the "Logidules" (parallel port connector J2, Pin 15) when J12 Pin 1-2 strapped; enable the interrupt from the real time clock when J12 Pin 2-3 strapped.

7. - CPU BOARD: SOFTWARE DESCRIPTION AND CONFIGURATION GUIDELINES

7.1. - Memory refresh

All address and control signals necessary to refresh external dynamic RAM modules are generated by the MICRO-LEARN CPU.

7.2. - Interrupts

The MICRO-LEARN CPU will process external interrupts in Z-80-CPU interrupt modes 0, 1, and 2. Internal onboard interrupts can be processed only in mode 1 or 2.

The real time clock calender IC National MM58167A may generate:

- 8 possible interrupt signals to the CPU (10 Hz, 1Hz, once per minute, once per hour, once per day, once per week, once per month, and when a Real time counter register coincidence occurs).
- 1 standby interrupt signal to the external world (pin 13, connector J2).

7.3. - System reset precautions

Data in Dynamic RAM is not guaranteed to be valid after a PUSHBUTTON RESET has been initiated.

7.4. - I/O addressing

The MICRO-LEARN CPU utilizes 114 of the possible 256 port addresses, leaving 142 port addresses available for expansion by the user.

DEVICE	PORT ADDRESS
MK3801 STI	B0H-BFH
PARALLEL OUTPUT LATCH	D0H
MEMORY CONFIGURATION	FFH
REAL-TIME CLOCK	00H-1FH
EPFL-BUS	40H-7FH

Figure 3. PORT ADDRESS.

7.5. - I/O MAP PROM programming guidelines

If it is desired to use port addresses other than those which are supplied, then the following procedure should be used.

Each address in the I/O Map PROM corresponds directly to a port address. The bits of the output byte are defined as shown in Figure 4. Select the desired port address and corresponding output bit definitions for that address and program a new I/O Map PROM with the new data.

OUTPUT BIT DEFINITIONS	ACTIVE
01 ON BOARD PORT SELECT	LOW
02 SELECT MEMORY CONFIGURATION	HIGH
03 SELECT PARALLEL OUTPUT	HIGH
04 SELECT REAL-TIME CLOCK	HIGH
05 EPFL-BUS	HIGH
06 SELECT STI	HIGH
07 (SPARE FOR USER)	
08 (SPARE FOR USER)	

Figure 4. BIT DEFINITION LIST OF I/O MAP PORT.

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power (bussed)	2	+5VDC	In	Logic Power (bussed)
	3	GND	In	Logic Ground (bussed)	4	GND	In	Logic Ground (bussed)
	5	VBB #1	In	Logic Bias #1 (-5V)	6	VBB #2	In	Logic Bias #2 (-5V)
DATA BUS	7	D3	In/Out	Low-Order Data Bus	8	D7	In/Out	High-Order Data Bus
	9	D2	In/Out	Low-Order Data Bus	10	D6	In/Out	High-Order Data Bus
	11	D1	In/Out	Low-Order Data Bus	12	D5	In/Out	High-Order Data Bus
	13	D0	In/Out	Low-Order Data Bus	14	D4	In/Out	High-Order Data Bus
ADDRESS BUS	15	A7	Out	Low-Order Address Bus	16	A15	Out	High-Order Address Bus
	17	A6	Out	Low-Order Address Bus	18	A14	Out	High-Order Address Bus
	19	A5	Out	Low-Order Address Bus	20	A13	Out	High-Order Address Bus
	21	A4	Out	Low-Order Address Bus	22	A12	Out	High-Order Address Bus
	23	A3	Out	Low-Order Address Bus	24	A11	Out	High-Order Address Bus
	25	A2	Out	Low-Order Address Bus	26	A10	Out	High-Order Address Bus
	27	A1	Out	Low-Order Address Bus	28	A9	Out	High-Order Address Bus
	29	A0	Out	Low-Order Address Bus	30	A8	Out	High-Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUXGND	In	AUX Ground (bussed)
	55	AUX +V	In	AUX Positive (+12V DC)	56	AUX -V	In	AUX Negative (-12V DC)

*Low-level active indicator

Figure 5. STD-BUS CONNECTOR (J1).

The STD-BUS address, data and control lines are bidirectional to allow external masters to access memory on the CPU board directly and are buffered and brought out to a 56 pin edge connector as shown in Fig. 5.

The 8 bit parallel output port with handshake lines is configured to accomodate direct connection to a Centronics type printer interface (Fig. 6). The programming information for the standby interrupts on pin 13, is described in the technical manual "CMOS DATABOOK" Real-time Clock MM58167A from National Semiconductor

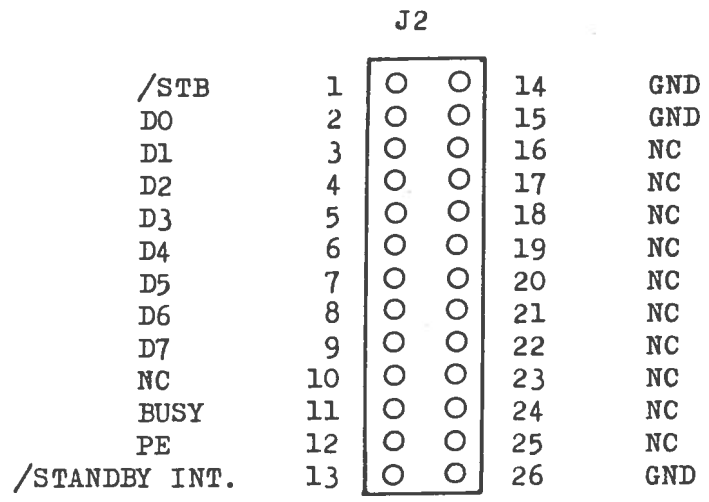


Figure 6a. PRINTER CONNECTOR (J2) WITH SIGNALS.

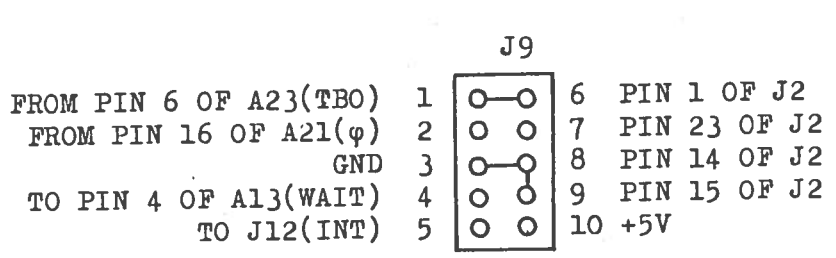


Figure 6b. J9 STRAPPING FOR PRINTER.

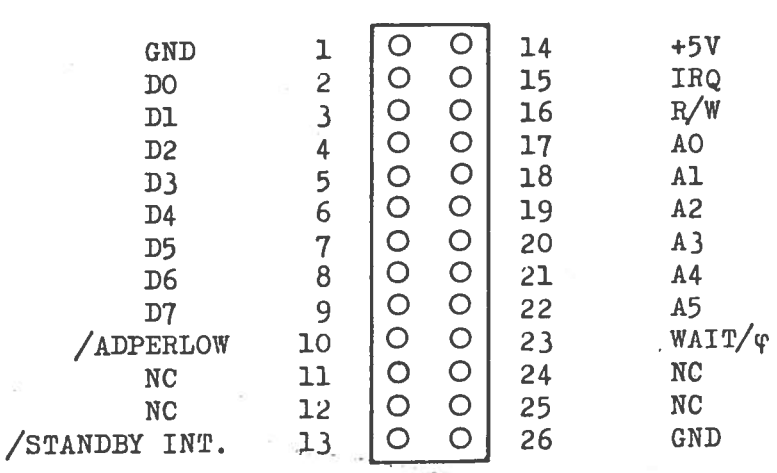


Figure 7a. EPFL-BUS CONNECTOR (J2) WITH SIGNALS.

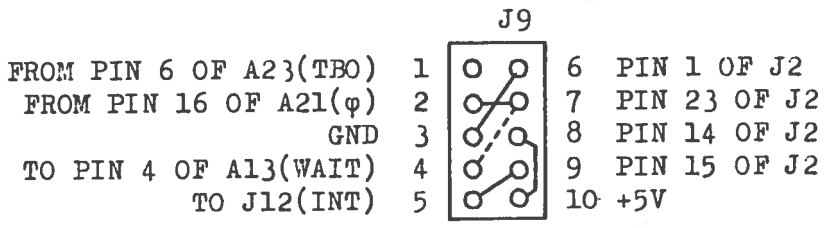


Figure 7b. J9 STRAPPING FOR EPFL-BUS.

This bus has 8 data lines D0 to D7 (positive true), six address lines A0 to A5 to allow I/O for 64 locations, INTERRUPT REQUEST (IRQ), READ/WRITE, WAIT/ (active low for slow memories), +5 volts and GND (Fig. 7a). The bus signals are valid, whenever /ADPERLOW is true (low) indicating "base address decoded".

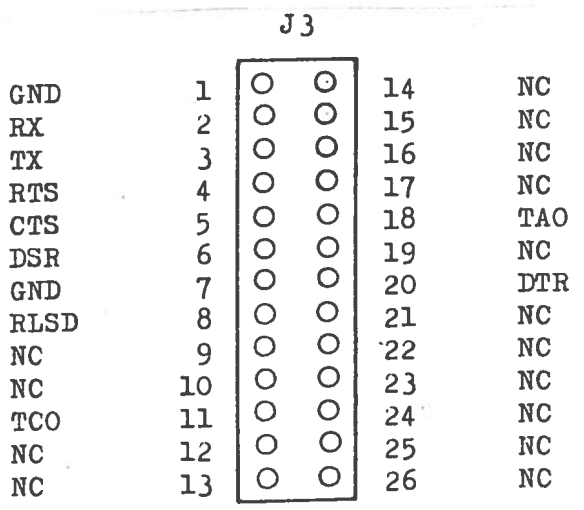


Figure 8. SERIAL CONNECTOR (J3).

The serial comunication signals to perform an RS232-C type interface to the alphanumeric terminal without null modem are buffered and brought out to a 26 pin connector as shown in Fig.8; the timer outputs are also buffered and brought out on pin 11 and 18.

Programming information for the serial channel and timers can be found in the SERIAL TIMER INTERRUPT CONTROLLER (STI) Technical manual, Mostek publication number 4420250.

7.6. - RAM/ROM/EPROM strapping

The jumpers J4-8 (Fig. 9a and Fig. 9b) allow the BYTEWYDE TM sockets A3-A7 to be

configured to accept various devices (Fig. 10). Each socket is associated with a jumper connector for strap selection of a particular memory type. (Ex. connector J4, select memory type in socket A3; J5 jumper, select A4 socket....)

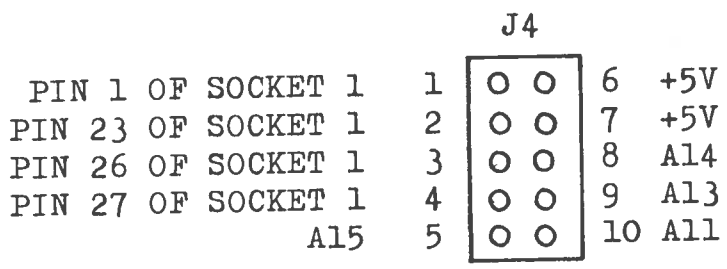


Figure 9a. JUMPER CONNECTOR J4 FOR EPROM SOCKET A3.

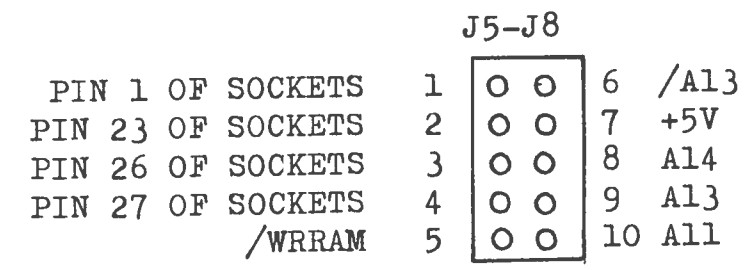


Figure 9b. JUMPER CONNECTORS J5-J8 FOR RAM/ROM SOCKETS A4-A7.

The memory map PROM (A17) contains eight memory configuration maps. As the chart in Figure 11 indicates, resolution of the maps is 4K byte blocks. The numbers enclosed in brackets ( ), represent BYTEWYDE (TM) memory sockets on board. The memory installed may be either RAM or ROM. The indication (RAM) represents offboard RAM.

7.7. - MEMORY MAP PROM programming guidelines

Each memory MAP in the Memory Configuration PROM consists of a series of bytes which define what memory is enabled. The function of each bit of the byte is defined in Figure 12.

- SELECT SOCKET A3 TO A7: This generates the signals which enable each BYTEWYDE socket for operation.

- OFF-BOARD MEMORY SELECT (MEMEX): This bit generates a signal which is defined by the STD-BUS specification for the MEMEX signal. In most single board configurations this bit is asserted low.

- ON-BOARD MEMORY SELECT: This bit indicates that one of the on board memory sockets has been selected.

TOSHIBA BYTE-WIDE MEMORY PIN OUT (CURRENT AND FUTURE DEVICES)

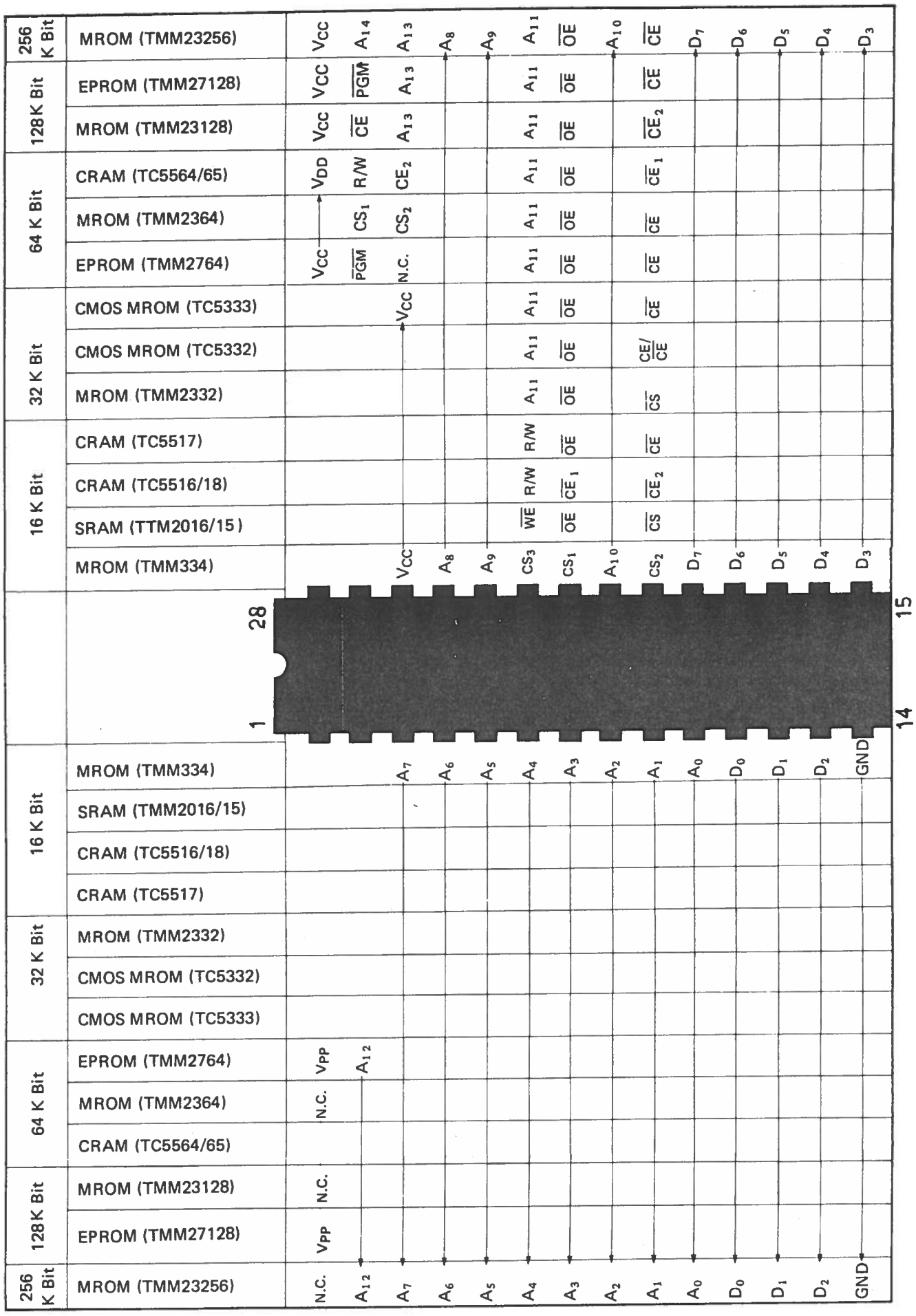


Figure 10. EXAMPLES OF BYTEWYDE TM ROM, EPROM AND RAM TYPES.

MAP / ADDRESS	0	1	2	3	4	5	6	7
F000H	A7				A7	A7	A7	
E000H	A3/A7							
D000H	A7				(RAM)		(RAM)	
C000H								
B000H	A6					A6		
A000H								
9000H								
8000H								
7000H	A5					A5		
6000H								
5000H								
4000H								
3000H	A4					A4		
2000H								
1000H								
0000H	A3							

Figure 11. MEMORY MAP.

OUTPUT BIT DEFINITIONS	ACTIVE
01 SELECT SOCKET A3	LOW
02 SELECT SOCKET A4	LOW
03 SELECT SOCKET A5	LOW
04 SELECT SOCKET A6	LOW
05 SELECT SOCKET A7	LOW
06 OFF-BOARD MEMORY SELECT(MEMEX)	HIGH
07 ON-BOARD MEMORY SELECT	LOW
08 SYSTEM BOOT	LOW

Figure 12. BIT DEFINITION LIST OF MEMORY MAP PROM.

- SYSTEM BOOT: This bit indicates that BYTEWYDE (TM) socket A3 has been selected while in map 0.

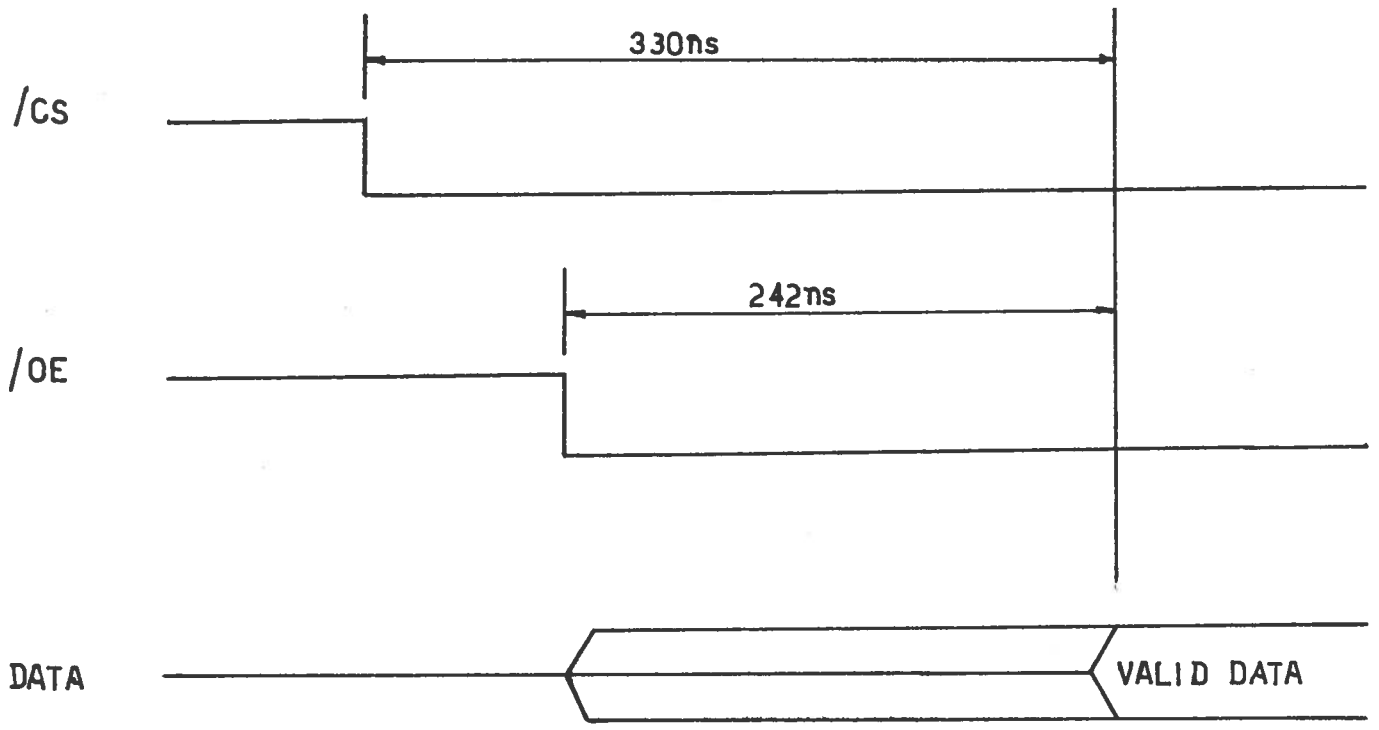


Figure 13. RAM/ROM ACCESS TIME.

The time required for the RAM/ROM memory to be accessed by the CPU is defined by two specifications; /CS and /OE. First the /CS to valid data must be <330ns. Secondly the /OE to valid data must be < 242 ns. These requirements must be satisfied in order to meet the minimum setup time for the CPU under worst case conditions. See Fig. 13.

8. - DISK CONTROLLER BOARD FEATURES

We now describe the Disk Controller board which is illustrated in Fig. 14.

- STD-BUS compatible.
- Controls up to four 8-inch floppy or three 5 1/4-inch minifloppy single or double density and single or double sided jumper-selectable Shugart compatible floppy disk drives.
- Provision for priority DMA daisy chain operation.
- For each floppy, provides soft sector operation, including variable-length sectors.
- For each floppy, provides IBM 3740 and System 34 diskette formatting capability.
- For each floppy, provides automatic track seek with verification and programmable step rate.
- For each floppy, provides DMA or programmed data transfer of single sector, multi-sector

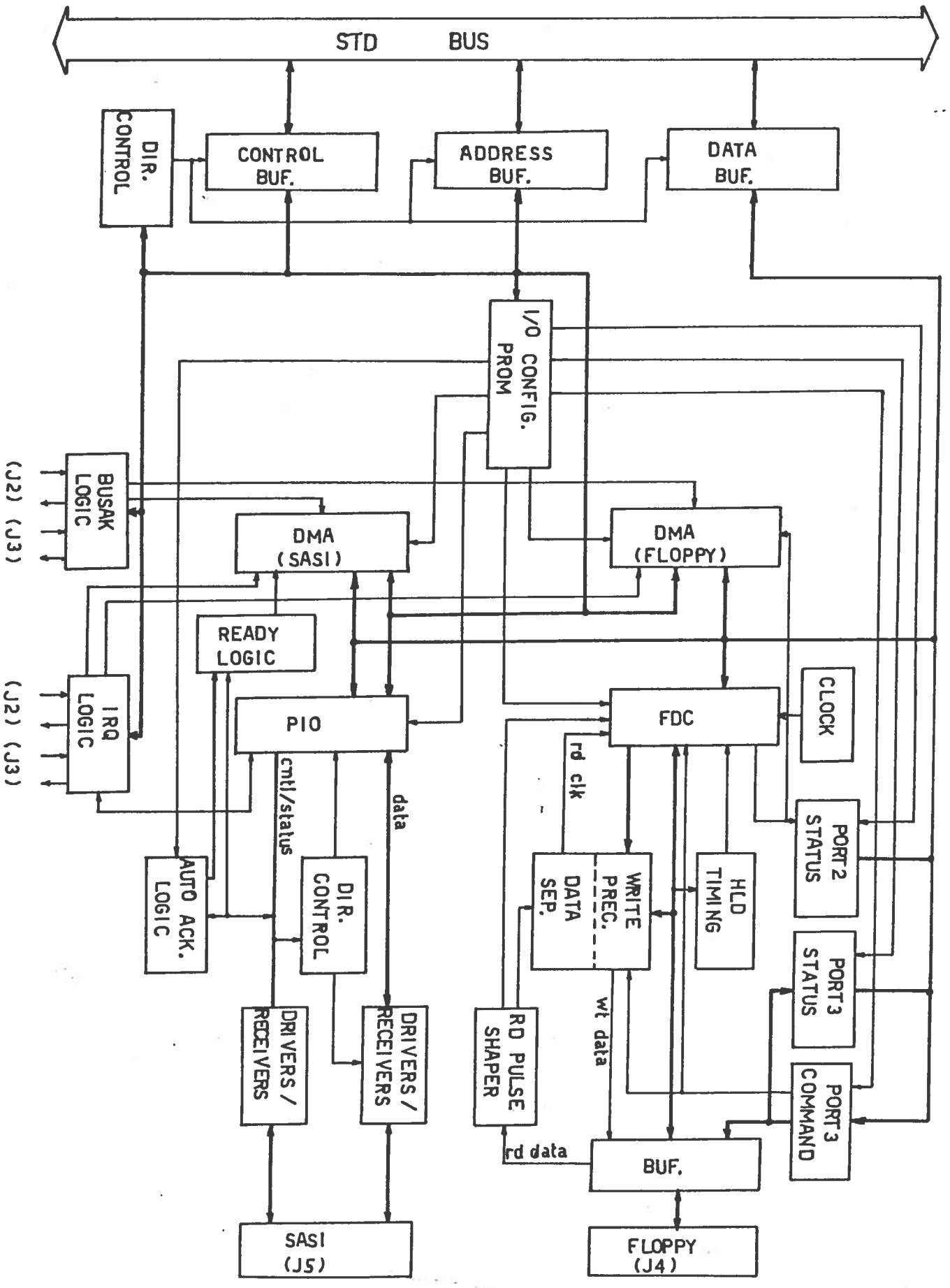


Figure 14. BLOCK DIAGRAM OF DISK CONTROLLER BOARD.

or full track.

- Interrupt driven or polled operation.

- For each floppy, provides automatic CRC generation and checking.

- Supports Shugart Associated System Interface (SASI™).

- Up to 4 MHz operation. Maximum transfer rates: SASI, 570 kbytes/sec.; double-sided double-density floppy disk 62.5 Kbytes/sec.

- Flexible I/O configuration by the use of I/O configuration PROM

- External wait request supported.

9. - DISK CONTROLLER DESCRIPTION

The disk controller board is made of two sections: one section controls the floppy drives, the other section controls the Winchester type hard disk drive. If the hard disk is not necessary in the system, part of the components can be saved or the second section can be interfaced to other peripheral devices using DMA transfer type comunication.

The bidirectional buffer for address, data and control lines and the port I/O decoding part is done in common for both sections.

In the floppy section, transfers to and from the disk are handled by the Z8410 DMA controller; programmed data transfer is also possible. Multiple Disk Controller boards can be operated simultaneously since daisy chained priority DMA operation is possible.

The Disk Controller board operates with a wide variety of disk drives, such as those by Shugart Associates, Teak, Tandon, Basf, etc.. Either 5 1/4- or 8-inch drives may be used; a simple change of five straps converts the Disk Controller board from a 5 1/4-inch controller to an 8-inch controller.

Since the Disk Controller board is based on the WD1797 Floppy Controller, many advanced features are available. These include IBM 3740 or IBM System 34 diskette formatting capability, automatic track seek with verification, programmable step rate, and automatic CRC generation and checking. In addition, single sector, multisector, or complete track transfer are possible.

The second section makes use of a Z8410 DMA Controller and a Z8420 PIO Parallel Input/Output in order to support the Shugart Associated System Interface (SASI). SASI is a universal system interface that lets OEMs upgrade, mix, and interchange peripherals wi-

thout affecting software, and which results in easy peripheral integration.

The board also contains auto acknowledge logic. This strapping option provides automatic handshaking for SASI information transfer, and is essential to the board's DMA operation. If finer control is required for debugging purpose, the auto acknowledge can be disabled.

10. - DISK CONTROLLER HARDWARE

10.1 - Electrical specifications

DATA BUS: 8 bits bidirectional

ADDRESS BUS: 16 bits, lower 8 bidirectional, upper 8 output during DMA activity.

SYSTEM BUS: STD compatible.

INPUTS: one 74LS load max.

OUTPUTS: I = 15 mA min at 2.4 Volt.

I = 24 mA min at 0.5 Volt.

SYSTEM CLOCK: up to 4 MHz.

I/O ADDRESSING: Flexible I/O addressing by using I/O configuration PROM. At present, it's configured that A0H - A7H is for SASI and E0H - E7H is for floppy.

MEMORY ADDRESSING: on board DMA is capable of addressing any memory address.

POWER REQUIREMENT: +12 Volt @ 100 mA max.

+ 5 Volt @ 2 A max.

OPERATING TEMPERATURE: from 0 to 60 °C.

10.2. - Mechanical specifications

CARD DIMENTIONS: 11.43 cm wide by 20 cm long

1.71 cm. maximum profile thickness

0.16 cm. printed circuit board thickness

10.3. - STD-BUS edge connector

(J1): 56 pins dual readout; 0.317 cm. centers.

10.4. - INTERRUPT PRIORITY/DMA daisy chain for floppy connector (J2)

8 pin dual right angle; 0.254 cm. centers

10.5. - INTERRUPT PRIORITY/DMA daisy chain for SASI connector (J3)

8 pin dual right angle; 0.254 cm. centers

10.6. - Floppy interconnect (J4)

34 pin right angle; 0.254 cm. center.

10.7. - SASI interface (J5)

50 pin 0.254 cm. centers.

10.8. - Jumper connectors

The layout of the jumpers on the board is shown in Fig. 15.

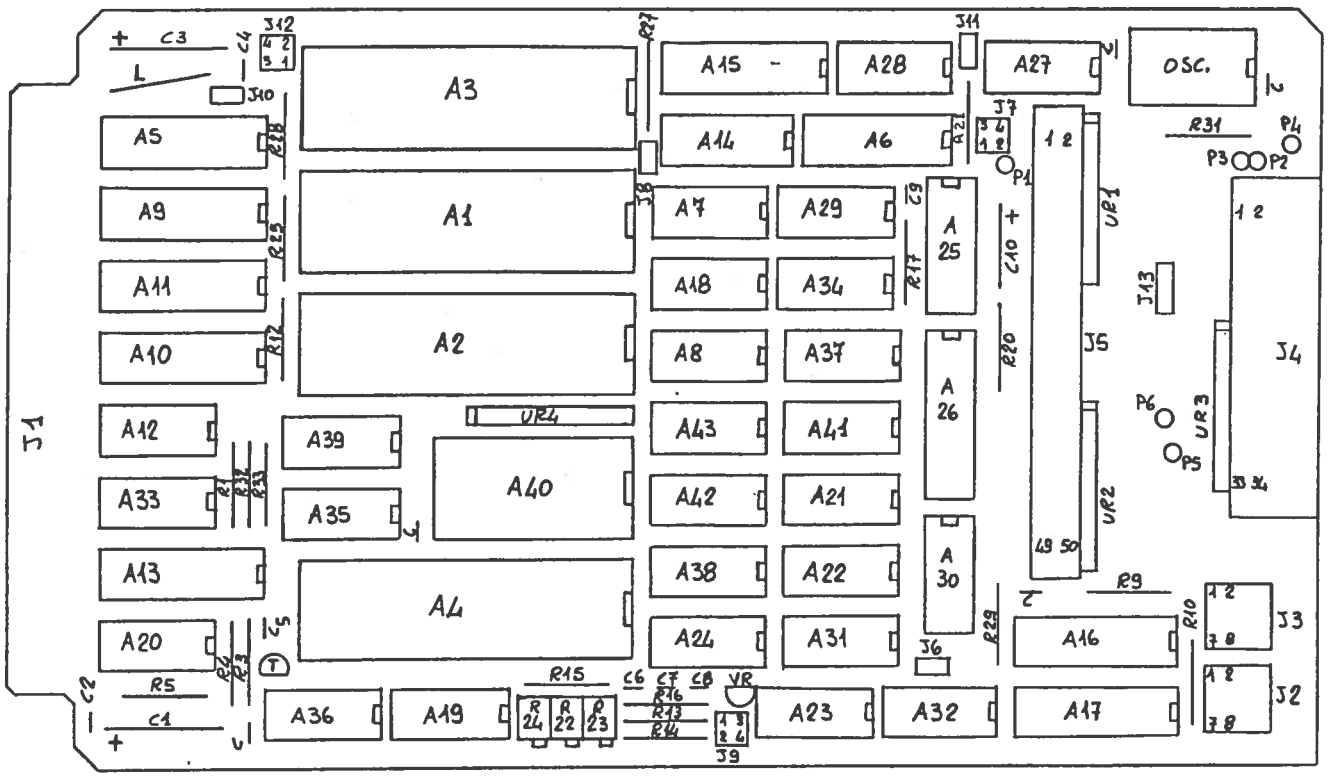


Figure 15 COMPONENTS AND JUMPER CONNECTORS LAYOUT OF DISK CONTROLLER BOARD.

11. - STRAPPING OPTIONS

11.1. - J6: Auto Acknowledge Enable

It's strapped to enable the Auto Acknowledge logic of SASI. This circuit will carry out the SASI bus handshake on information transfer without requiring the CPU to bit toggle control lines (SASI ACK). J6 must be strapped if DMA operation is desired. If the user needs to explicitly bit toggle the SASI ACK line (e.g. to debug a controller board) the J6

strap should be removed.

11.2 - J7: 8 or 5 1/4-inch Clock

Strap for either a 4 MHz clock (pin 3 and 4) for 8-inch floppy or a 2 MHz clock (pin 1 and 2) for 5 1/4-inch floppy.

11.3. - J8: 8-inch Ready

When using an 8 inch floppy, this strap connects a ready signals to the Controller. When using a 5 1/4-inch drive, this strap is not connected. Thus a 5 1/4-inch floppy will always appear ready.

11.4. - J9: VCO Clock

This clock is either a 4 MHz clock (pins 1 and 2 strapped) for 8-inch floppy or a 2 MHz clock (pins 3 and 4) for 5 1/4-inch floppy.

11.5. - J10: Auto Precompensation

When open, double density write precompensation is always in effect (provided DDEN is low). This is primarily for 5 1/4-inch drives that require write precompensation on every track. When strapped, write data is precompensated only for tracks greater then 43; this is the case of 8 inch floppy.

11.6. - J11: 5 1/4-inch floppy

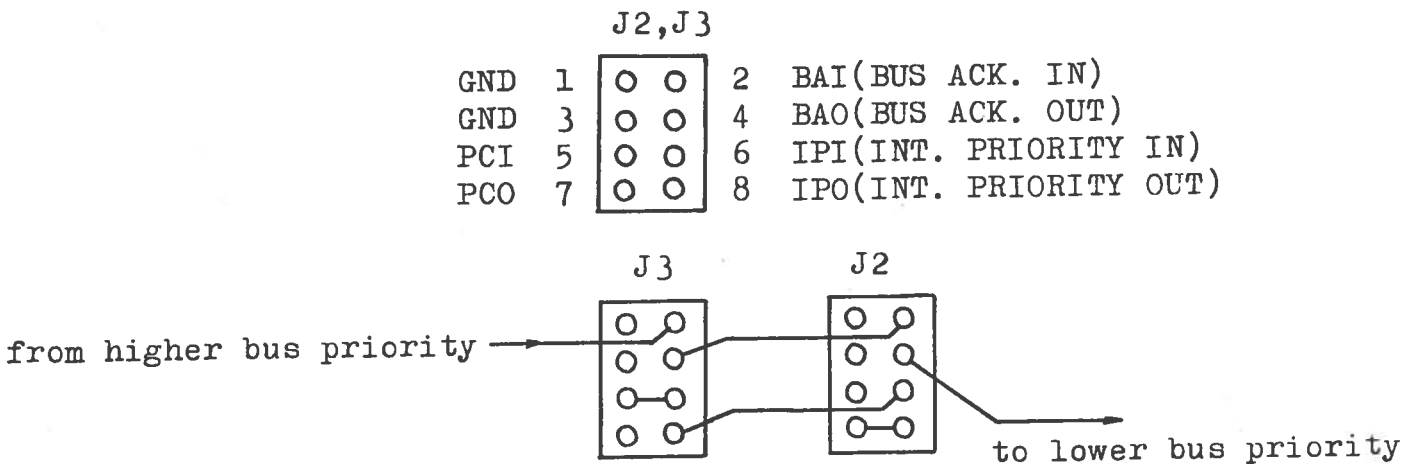
This strap may be used by software to determine whether 5 1/4 or 8-inch floppy is used. Strap J11 is needed for 5 1/4-inch floppy.

11.7. - J12: Test Points

Test points are for maintenance only.

11.8. - INTERRUPT PRIORITY/DMA daisy chain option

There are two DMA controllers on the board, and this board is also designed to support additional DMA operations in a system. J2 and J3 are used to implement the interrupt priority and DMA daisy chain connection, the pin assignement of J2 and J3 and their connections are shown in Fig. 16. Typically, twisted pairs (signals + ground) are used to connect the priority chain.



(The priority of bus and interrupt for SASI is assumed to be higher than that for floppy.)

Figure 16. INTERRUPT PRIORITY AND DMA DAISY CHAIN CONNECTION.

Signals	Directions	Terminal Nos.	
		Signals	0V
RESERVED		2	1
IN USE/HEAD LOAD	INPUT	4	3
DRIVE SELECT 3	INPUT	6	5
INDEX	OUTPUT	8	7
DRIVE SELECT 0	INPUT	10	9
DRIVE SELECT 1	INPUT	12	11
DRIVE SELECT 2	INPUT	14	13
MOTOR ON	INPUT	16	15
DIRECTION SELECT	INPUT	18	17
STEP	INPUT	20	19
WRITE DATA	INPUT	22	21
WRITE GATE	INPUT	24	23
TRACK 00	OUTPUT	26	25
WRITE PROTECT	OUTPUT	28	27
READ DATA	OUTPUT	30	29
SIDE ONE SELECT	INPUT	32	31
READY	OUTPUT	34	33

Figure 17. FLOPPY DISK SIGNALS INTERFACE CONNECTIONS.

12. - CONNECTION TO FLOPPY

The logic interconnection to floppy is made from J4 on the board to a 34 pin edge connector on the drive. The connection is made with a standard 0.254 cm. center 34 pin ribbon cable. Refer to Fig. 17. Note all odd pins are ground.

13. - CONNECTION TO SASI

The logic interconnection to SASI is made from J5 on the board to SASI bus connector. Fig. 18 shows the pin definition of J5. Note all odd pins are ground.

Pin. No.	Signal	
2	DB0 (data bit 0, LSB)	SASI Data Bus
4	DB1 (data bit 1)	
6	DB2 (data bit 2)	
8	DB3 (data bit 3)	
10	DB4 (data bit 4)	
12	DB5 (data bit 5)	
14	DB6 (data bit 6)	
16	DB7 (data bit 7, MSB)	
18	Not used (data bus parity)	
20	Not used	
22	Not used	
24	Not used	
26	Not used	
28	Not used	
30	Not used	
32	Not used	
34	Not used (ATN, attention)	SASI Control Bus
36	BSY (busy)	
38	ACK (acknowledge)	
40	RST (reset)	
42	MSG (message)	
44	SEL (select)	
46	C/D (control/data)	
48	REQ (request)	
50	I/O (input/output)	

Figure 18. SASI SIGNALS INTERFACE CONNECTIONS.

14. - I/O PORTS

The floppy controller and SASI interface each occupies a block of eight contiguous I/O port addresses. These blocks of eight can be configured by the I/O configuration PROM anywhere in the main address space. At present, the floppy controller resides from E0H to E7H and the SASI interface resides from A0H to A7H. Fig. 19 and Fig. 20 show the utilization of their eight ports separately.

	b7 b0	b7 b0
A2-A0	**Read**	**Write**
0 0 0	MK3883 DMA Controller IC	MK3883 DMA Controller
0 0 1	Undefined	Not used
0 1 0	XX FB SZ XX XX XX IR SS	Not used
0 1 1	XX XX XX XX D4 D3 D2 D1	SD RS XX XX D4 D3 D2 D1
1 0 0	1797 Status Register	1797 Command Register
1 0 1	1797 Track Register	1797 Track Register
1 1 0	1797 Sector Register	1797 Sector Register
1 1 1	1797 Data Register	1797 Data Register

Figure 19. PORT UTILIZATION FOR FLOPPY.

A7	A6	A5	A4	A3	A2	A1	A0	Function
X	X	X	X	X	0	0	0	PIO Port A Data (Bidirectional)
X	X	X	X	X	0	0	1	PIO Port B Data (Bit Control Mode)
X	X	X	X	X	0	1	0	PIO Port A Control
X	X	X	X	X	0	1	1	PIO Port B Control
X	X	X	X	X	1	0	0	DMA Controller
X	X	X	X	X	1	0	1	Reserved
X	X	X	X	X	1	1	0	Reserved
X	X	X	X	X	1	1	1	Reserved

Figure 20. PORT UTILIZATION FOR SASI.

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ACKNOWLEDGEMENTS

This 8-bit microprocessor development system developed at the Istituto Nazionale di Fisica Nucleare is at present used in a real-time data acquisitionsystem for the measurement of events in nuclear emulsions. The system consists essentially of a conventional microscope complemented of the following facilities: computer control of the X, Y, Z movements; of a motorized stages and a digitalization of X, Y, Z coordinates.

GAO ZHONG-REN has carried out this work with the support from a grant of the International Centre for Theoretical Physics (ICTP) Program for training and Reasearch in Italian Laboratories, Trieste, Italy. He would also like to express his gratitude to Prof. Abdus Salam, Director of ICTP, Prof. G. Furlan, Head of the Programme, and Prof. G. Denardo for providing him the opportunity to do research in the field of microprocessors. A special thanks to Prof.sa A. Marzari Chiesa and Prof. S. Costa, Director of the Istituto di Fisica Superiore dell'Universita' di Torino, for providing the hospitality. The authors gratefully acknowledge Prof. A. Werbrouck for suggestions, criticism and proofreading of the guide and Prof. C. Manfredotti for his encouragement and support.

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