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A HIGH ACCURACY CALIBRATION SYSTEM FOR CHARGE READ-OUT ELECTRONICS

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Experiments in high energy physics performed during the last years have seen, in order to improve tracks reconstruction and particle identification, an increasing effort in improving the electronic chain connected with the various types of detectors employed.

The last family of gasous detectors, MWPCs and lately TPCs, requires with a high degree of precision, the knowledge of analog quantities such as the charge induced on the sensing elements of the detector (wires, strips and pads).

In order to obtain a precise measurement of this charge, the electronic chain associated with every channel of a detector consists usually in a charge-to-voltage preamplifier, an occasional storage device, and an ADC. One easily realizes how difficult the matter turns out to be if, together with a high precision (i.e. high ADC resolution), the detector is supposed to work with a high event rate which requires the electronics to operate at a several MHz frequency (i.e. flash ADC).

These factors impose some design rules which bring the nonperfect knowledge of some important parameters: pedestals, global gain, ADC transfer function, etc.

The electronic chain that equippes the PS170 central detector (several MWPCs with cathode read-out) and whose calibration system has been studied, presents a low noise preamp which, via a 60 mt. cable, feeds a PDC module (Pulse Detector & Converter) (Fig. 1). Cathode readout is based upon the measure of the charge induced on pads or strips by the avalanche occurred on sensing wires. In our MWPCs charge pulses have

THE PS170 CENTRAL DETECTOR ACQUISITION SYSTEM

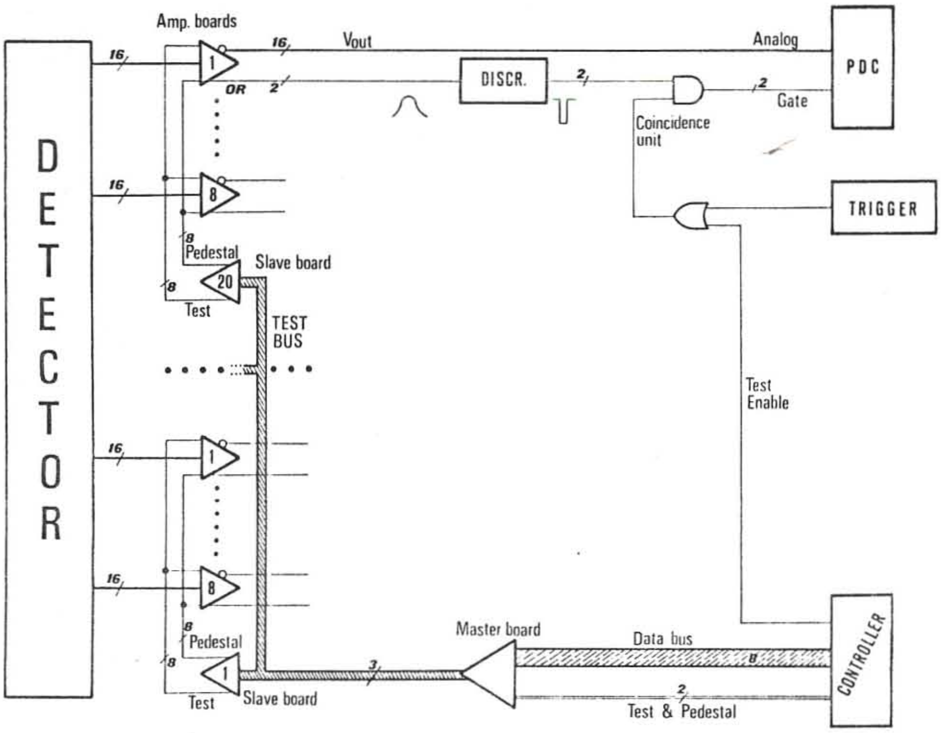

FIG. 1

a typical value of some hundreths of picoCoulomb with a maximum of 3 picoCoulomb. The preamp output varies, in consequence, up to 300 mVolt with a constant rise-time of 20 nsec. The determination of the track position is carried out by evaluating the centre of gravity of the induced charge distribution which affects about three strips. Its dimension depends upon several parameters and this may vary the number of strips involved. A very good homogeneity is then required to the electronic chain, in order to minimize the error on the determination of the charge distribution center. The PDC contains a 16 channels analog memory strobed by two independent gate signals (one for each group of eight adjacent channels). This memory is then serially multiplexed to **a 6 bit** FADC. The module operating frequency is about 25 MHz and, to lower the usually high 6 bit differential error, the FADC presents an input network which compresses the output response curve thus improving the resolution for small input signals.

These features cause systematic differencies to rise among the channels of the same PDC Module. This dishomogeneity is computed to be responsible of a 200 μm worse resolution, thus reducing the 200 μm theoretical detector resolution to 350 μm.

Early results of the calibration system applied to a MWPC equipped with 10 bits ADC showed an improvement in resolution from 400 μm to 250 μm. Furthermore, there is another striking advantage in employing such a calibration system, i.e. the possibility of monitoring the electronics status during data taking. In fact, another characteristics of the last generation detectors is the enormous number of channels associated with them, some thousands typically, which, in spite of the good reliability of the components employed, present a certain probability to break down. As quoted above, cathode read-out is extremely sensitive to channel malfunction and the absence of one channel response affects a zone of the detector much larger than that occupied by the channel sensing element.

Thus, a monitoring facility is extremely necessary in order to point out any channel not properly working.

Taking into account these requirements, together with circuitry simplicity and low cost, the following calibration system has been realized and put into operation.

The basic problem, as one can easily realize, is to inject at the beginning of the electronic chain, in parallel with the chamber detector element, a sufficient number of charge pulses covering the expected range of the signals coming from the chamber.

In order to measure the electronic chain parameters within a few percent (<5%) the charge pulse generation mechanism must obey to severe conditions: low-noise, high homogeneity between adjacent channels, very good linearity and cross-talk free operation. Furthermore, the calibration circuit has to be transparent for the signals coming from the chamber.

Since we are dealing with a relative calibration, that is the measurement of the parameters of one channel with respect to those of its neighbours, we do not care too much about thermal stability.

The mechanism of charge injection is very simple: a DAC generated voltage step is applied to a high precision capacitor connected with the preamp input. The voltage times the capacitor value gives the charge amount injected.

In our case, the charge picked-up by one detector element ranges from 0 to 4 picoCoulomb thus forcing us to use small values both of capacitor and voltage step.

We choose a value of 18 pF (±2%) for the capacitor and limited the voltage step to a maximum of 250 mVolts. This is generated by closing a high-speed MOSFET analog switch, thus connecting the DAC output voltage to a distribution network which further reduces the voltage step to the desired value.

The DAC is an 8 bits one, such to obtain an adequate number (256) of different charge pulses linearly distributed in order to measure with high accuracy the electronic relative transfer function. The system is built up with three stages: the CAMAC controller module, the master board and the slave board (Fig. 2).

The first is a single width CAMAC module whose output are: an 8 bit data word fed via a flat cable, the test and the pedestal pulses (NIM level), and a Test Enable NIM pulse whose function is to simulate the trigger signal to allow gate signals reach and trigger the PDC modules. The Test Enable pulse is regulable in width and delay with respect to the Test and Pedestal pulses. The function of the Pedestal pulse will be described

CALIBRATION SYSTEM BLOCK DIAGRAM

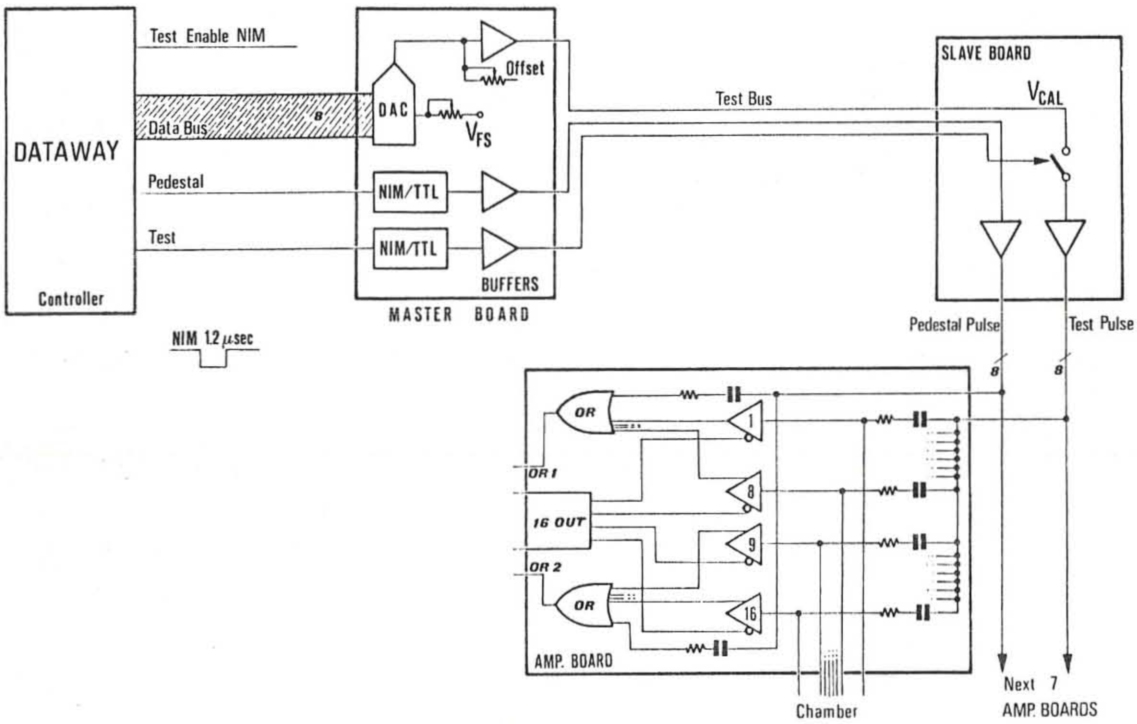

FIG. 2

later. On the master board, the 8 bits data word is applied to the DAC and the Test or the Pedestal pulse is converted from NIM to TTL level.

These three lines (the DAC output calibration voltage, the Test and the Pedestal pulses) are then buffered to the slave boards, connected in parallel via a flat cable. Each slave board then generates the calibration voltage step or the Pedestal signal which are sent to a maximum of eight preamp boards via a 30 cm 50 Ω cable.

For maximum flexibility the charge injection network, capacitances and time shaping resistances, are allocated directly on the preamp board.

Our experimental set-up with about 150 preamp board thus requires 20 slave boards which are easily driven in parallel by only one master board connected with the CAMAC controller.

Every preamp board contains 16 amplification channels whose positive output are grouped eight-by-eight and ORed together such to provide the two OR signals used to generate the gate for their own PDC. Thus, in our case, the calibration system must be able to test these OR lines, feeding an adequate signal into the OR circuit.

If the letter responds properly, its output is used to trigger the PDC without any signal present at its inputs, thus allowing the pedestal acquisition. That justify the name "Pedestal" given to this test pulse. It does not affect the calibration circuitry at all, that is without perturbing the preamp outputs.

The acquisition and knowledge of the whole electronics pedestals is very important for a correct data analysis and it must be performed periodically together with a complete calibration or, easier and quicker, with a correct-working monitoring.

That may rise some problems if not sufficient time is available among the data taking periods. One possible solution is to calibrate the electronics before every long-term run, evaluating and recording on tape the electronic parameters. This operation may take a lot of time depending upon the number of channels employed. The monitoring may then occur during the dead-time periods inside the run.

This monitor should provide few charge values whose responses have to be compared with those expected from the calibration parameters. Malfunctioning channels will be pointed out and their relative position inside the chamber has to be taken into account in order to decide if it is still possible to go on or if it is necessary to stop the run and repare the damage.

Besides the on-line employ, the calibration system is presently used to test the electronic set-up and the on-line acquisition system, together with maintenance operations and other facilities.

Its advantages are of course not limited to this experiment and its particular acquisition system, but it may find further application in future years gaseous detectors facilities because of its versatility and easy-to-modify features.

Circuit schemes and specifications are available on request.