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A ROMULUS COMPATIBLE ASYNCHRONOUS TIME AND AMPLITUDE PAD ACQUISITION SYSTEM

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ABSTRACT

A modular fast time/amplitude CAMAC data acquisition for Time Projection Chamber (TPC) pad signals is described. It works in asynchronous mode: when the pulse on a wire triggers the acquisition, the pulse height profile of the facing pad row is sampled through 7 bit flash converters. In this way an automatic zero suppression is performed at a very early stage of signal processing. The pad signals amplitudes and the drift times of ≤ 14 tracks can be measured, giving a true three dimensional readout of the TPC information. This electronics is under use in the WA71 experiment at CERN.

1. - INTRODUCTION

This paper describes a CAMAC ROMULUS compatible readout for Time Projection Chamber (TPC) pad signals[1-3] (see Figs. 1, 2, 3). It consists of master Asynchronous Timing Unit (ATU) modules and slave 8-channels Fast Analog to Digital Converter (FADC) modules. One ATU can control unitl 4 FADCs for a total of 32 time correlated pad channels (see Fig. 1). The system measures pulse heights of N rows of pads with a resolution of 7 bits; the time at which each pulse has occurred is also known within 100 ns(*). This electronics works in free running mode with pre-trigger

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(*) - A more refined (r. m. s. = 2 ns) determination of the arrival time of the drifting electrons is obtained sending the wire signals, after a constant fraction discriminator stage, to a modified Multiple Time Digitizer (MTD)[4].

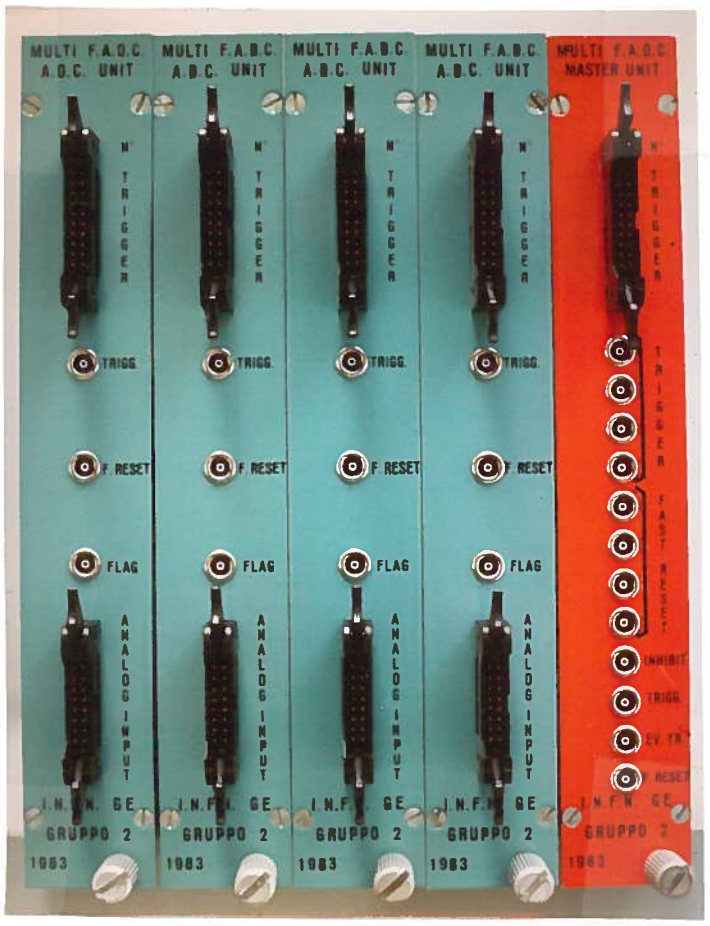


FIG. 1 - Photograph of the whole system for a row of 32 pads.

capability and can measure, at most, 14 tracks for each TPC. The mode of operation is the asynchronous one, i. e. : when the pulse on a wire triggers the acquisition, the pulse height profile of the facing pad row is sampled. In this way an automatic zero suppression is performed. Since the pad signals amplitudes and the arrival times of the drifting electrons are simultaneously measured, we get a true three dimensional readout of the tracks. In the FADC module provision is made to record until 255 samples per channel. A Synchronous Timing Unit (STU) has been developed for the prototype tests on the High density Projection Chamber (HPC)[5] of the DELPHI experiment[6] at LEP(*).

Until now 200 FADC channels and the related ATUs have been built and tested in laboratory and in the Omega' acquisition system at CERN.

2. - SYSTEM DESCRIPTION

The system can be configured connecting together a Master Asynchronous Timing Unit (ATU) module and one or more Fast Multi Analog to Digital Converter (FADC) modules. Normally the FADC modules are put, in a CAMAC crate, on the left of the related ATU module. In this way, when we read the CAMAC stations in growing order, we have first all the pulse height data and then the related timing information. The ATU provides the signal fan-out in order to drive until 4 FADC modules (32 channels).

The connections between the ATU and the FADCs are the followings:

a) Flat cable connection (2 x 10 signal wires) from No. Trigger (out) of the ATU to No.

(*) - In this case the charge profile due to a shower in the gas of the calorimeter through 255 clock cycles ($\nu_{Max} = 6$ MHz), while the zero suppression is left to a later stage of data treatment. Contrary to the ATU case, the number of FADCs that can be connected to a STU is unlimited.

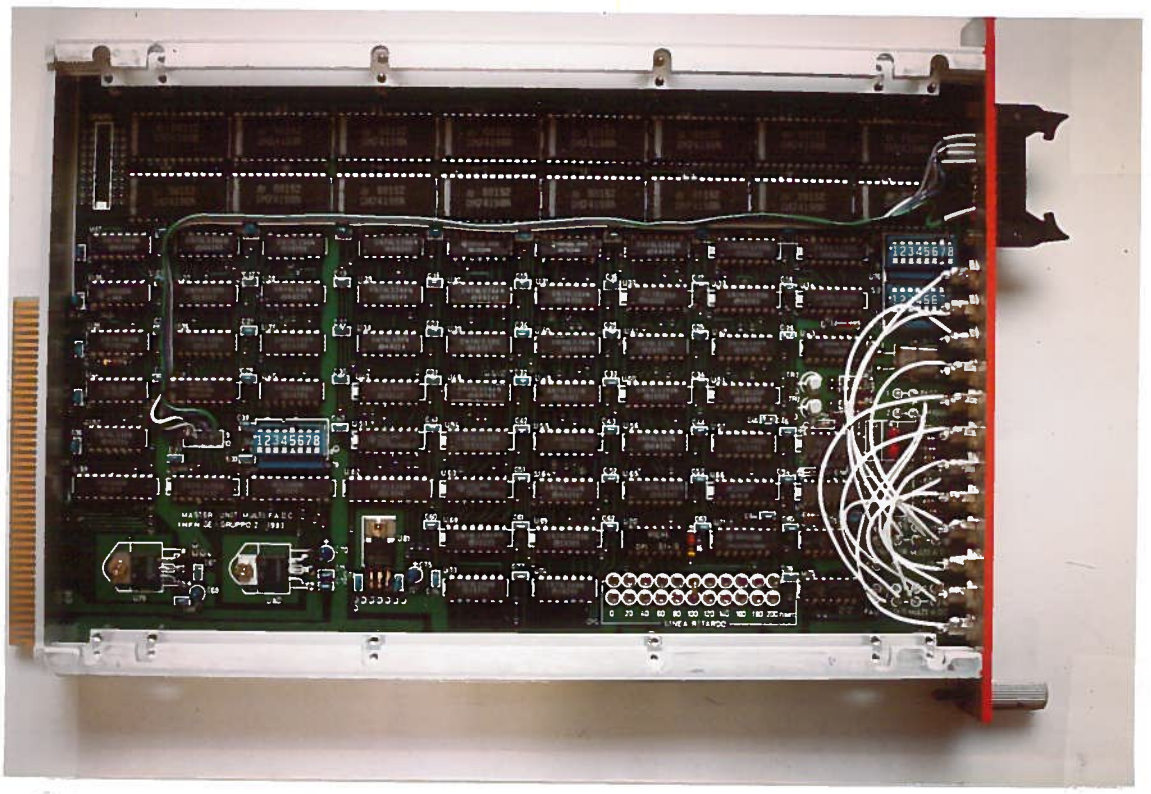


FIG. 2 - Internal view of the ATU module.

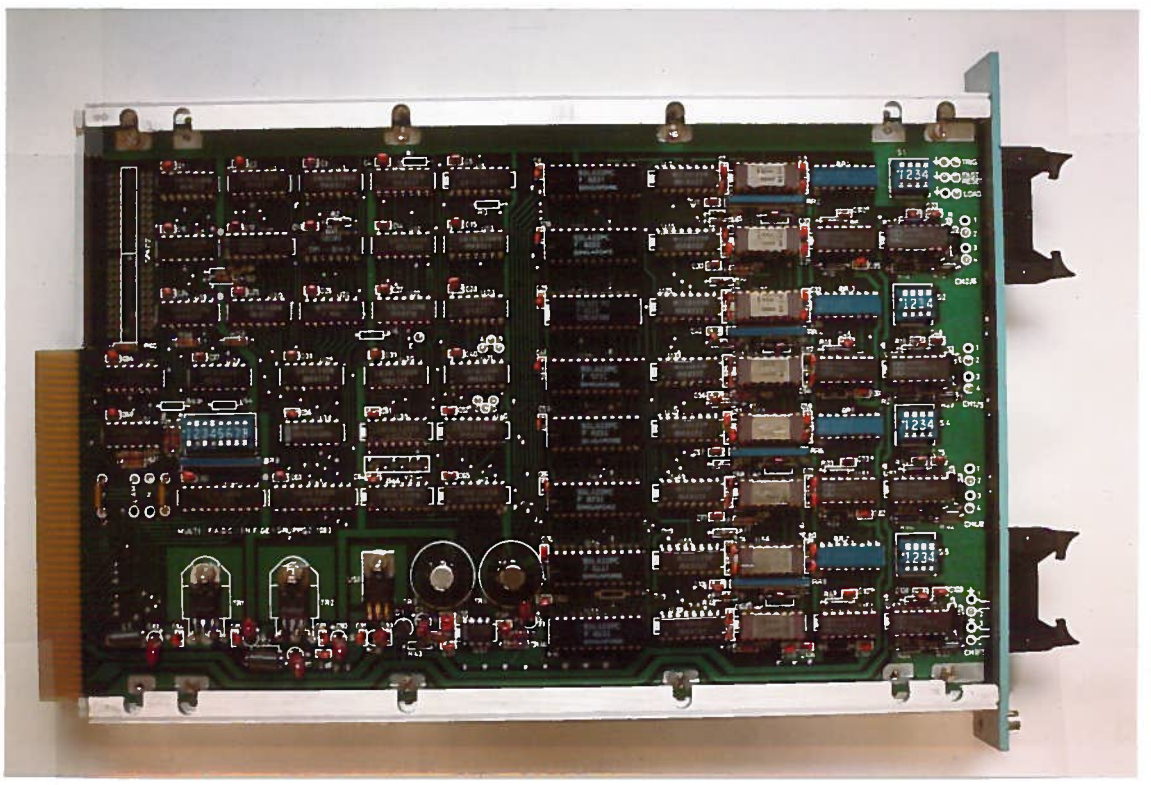


FIG. 3 - Internal view of the FADC module.

Trigger (in) of the FADCs. The cable must be kept shorter than 1 m and each connector must be less than 20 cm far from the previous one to avoid signal reflection due to the FADC input loads.

b) LEMO connection between one of four Trigger (out) of ATU to the related Trigger (in) of FADCs.

c) LEMO connection between one of four Fast Reset (out) of ATU to the related Fast Reset (in) of FADCs.

When the system is in acquisition mode each Trigger signal, coming to the ATU module, strobes, after a presettable delay (from 70 to 270 ns), the FADCs. In this way for each trigger n*8 (n = 1,..., 4) pulse heights and related time are recorded. When the Event Trigger pulse arrives to the ATU the acquisition system is stopped after a presettable digital delay (from 0 to 12.8 μs) and is prepeared for the CAMAC readout. At this point the system gives out the amplitudes and the time of signals coming in the last t nanoseconds (t is switch selectable between 0 and 12.8 μs in 100 ns steps).

A time diagram of the input signals is shown in Fig. 4. In Fig. 5 the typical differences between the eight channels of a FADC module are shown. In Fig. 6 the reconstructed signals of the 8 channels are drawn.

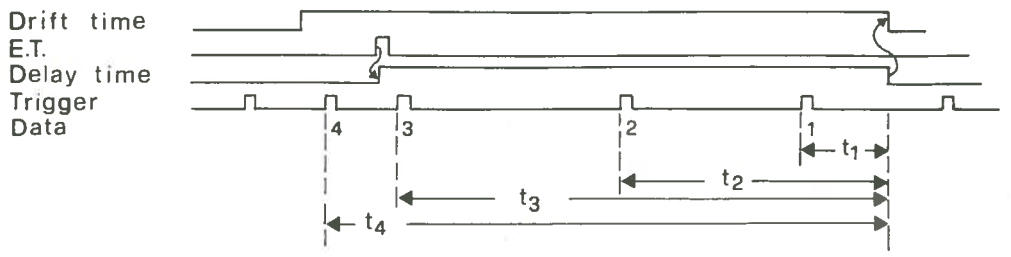
3. - CIRCUIT DESCRIPTION OF THE MASTER ASYNCHRONOUS TIMING UNIT (ATU)

In Fig. 7 the block diagram of the ATU is reported, while in Fig. 8 we present the component layout and in Fig. 9 the detailed electrical diagram. In the photograph of Fig. 2 there is an internal view of the ATU.

The internal operation of the ATU is marked by five main timing signals: Event Trigger (ET) and Borrow 1 to 4 (B1-B4). The acquisition mode of the whole system is set via CAMAC with a C, Z, F9 or via front-end with a Fast Reset (FR) NIM signal. The time digitizer (ATU) records continuously until the arrival of the ET. Every trigger after being shaped, synchronized (with the 10 MHz clock), is presented to the input of the 128 bits shift register (U1-U16). Then the bit "1", that marks the trigger, is shifted at each clock pulse; in this way we have a time record of the triggers come in the last 12.8 μs.

The acquisition mode of the ATU goes on indefinitely until ET arrives. The ET signal generates a sequence of internal signals (B1-B4) through which the ATU moves from acquisition mode to CAMAC readout. Following the B1-B4 signals we have a trace of the working way of the ATU (see Fig. 7):

FRONT–END SIGNALS



ATU CAMAC RECORD STRUCTURE

F E D C B A 9 8 7 6 5 4 3 2 1 0		word N°
F | | | N° Trig	MARKER	1
	Time 1	2
	Time 2	3
	Time n	n+1
	Total Drift Time	n+2

F = 1 ⇒ > 14 Trigger

FADC CAMAC RECORD STRUCTURE

F E D C B A 9 8 7 6 5 4 3 2 1 0		word N°
N° Trigger	MARKER	1
O Ch 2 Dt 1	O Ch 1 Dt 1	2
O Ch 4 Dt 1	O Ch 3 Dt 1	3
O Ch 6 Dt 1	O Ch 5 Dt 1	4
O Ch 8 Dt 1	O Ch 7 Dt 1	5
O Ch 2 Dt 2	O Ch 1 Dt 2	6
O Ch 4 Dt 2	O Ch 3 Dt 2	7
O Ch 6 Dt 2	O Ch 5 Dt 2	8
O Ch 8 Dt 2	O Ch 7 Dt 2	9
O Ch 2 Dt n	O Ch 1 Dt n	4(n-1)+2
O Ch 4 Dt n	O Ch 3 Dt n	4(n-1)+3
O Ch 6 Dt n	O Ch 5 Dt n	4(n-1)+4
O Ch 8 Dt n	O Ch 7 Dt n	4(n-1)+5

O = 1 ⇒overflow

FIG. 4 - CAMAC record structure of the ATU and of the FADC and the time diagram of the input signals.

Marker ADC = 36
Marker Timing Unit = 1
Maximum Drift Time = 28
Gain of Amplifiers = 20

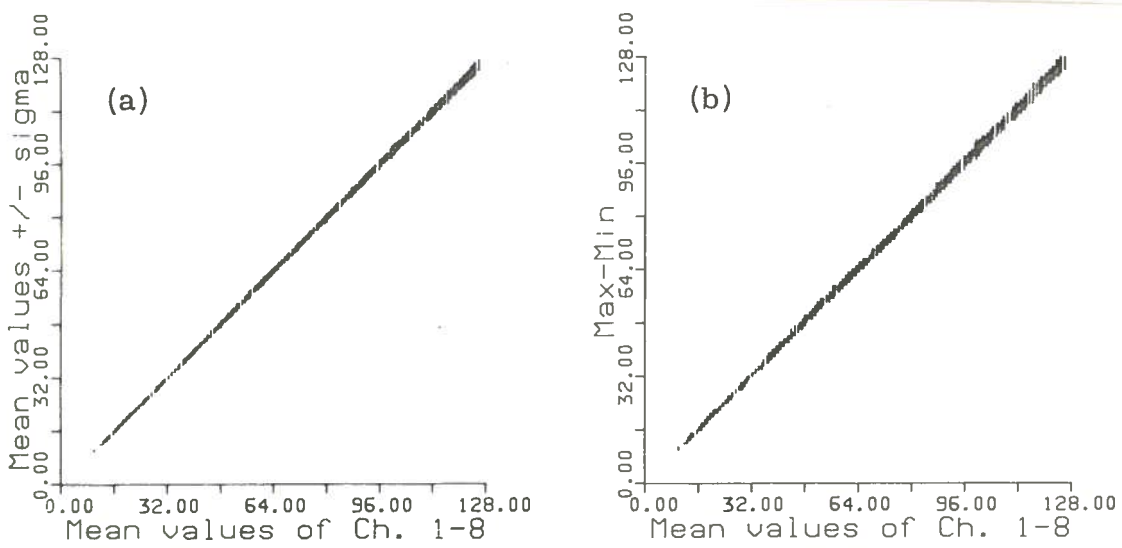
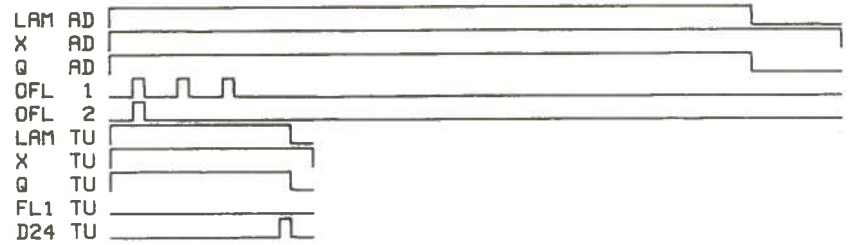


FIG. 5 - Linearity response of the 8 ADC channels of a FADC module. The band represents the 2σ fluctuation (a), or the maximum minus minimum fluctuation (b) around the mean value measured by the 8 channels. The input signal to the FADC is a ramp with a slew rate of 10 ch/μs. No correction is applied to the data.



RUN No. 5/1 INFN/GE 09-AUG-83

Marker ADC = 33
Marker Timing Unit = 1
Maximum Drift Time = 124
Gain of Amplifiers (/6.8):
Ch1=4, Ch2=5, Ch3=6, Ch4=7
Ch5=3, Ch6=3, Ch7=3, Ch8=3

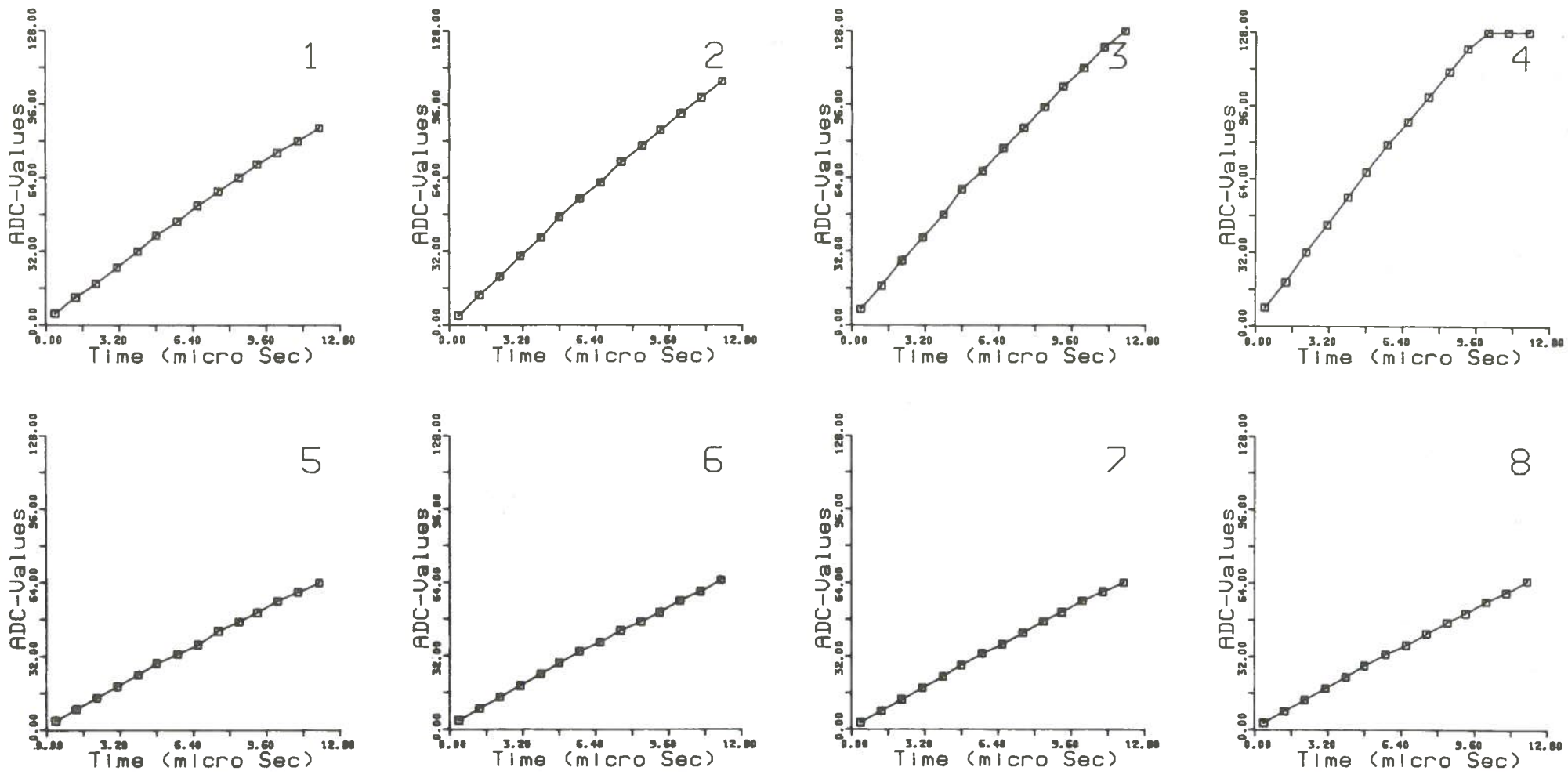


FIG. 6 - The same pulse encoded by the 8 channels of a FADC module. 14 pulse height measurements are made along the pulse profile. Channel 1 to 4 have different gains (see figure for details) while channel 5 to 8 have the same gain.

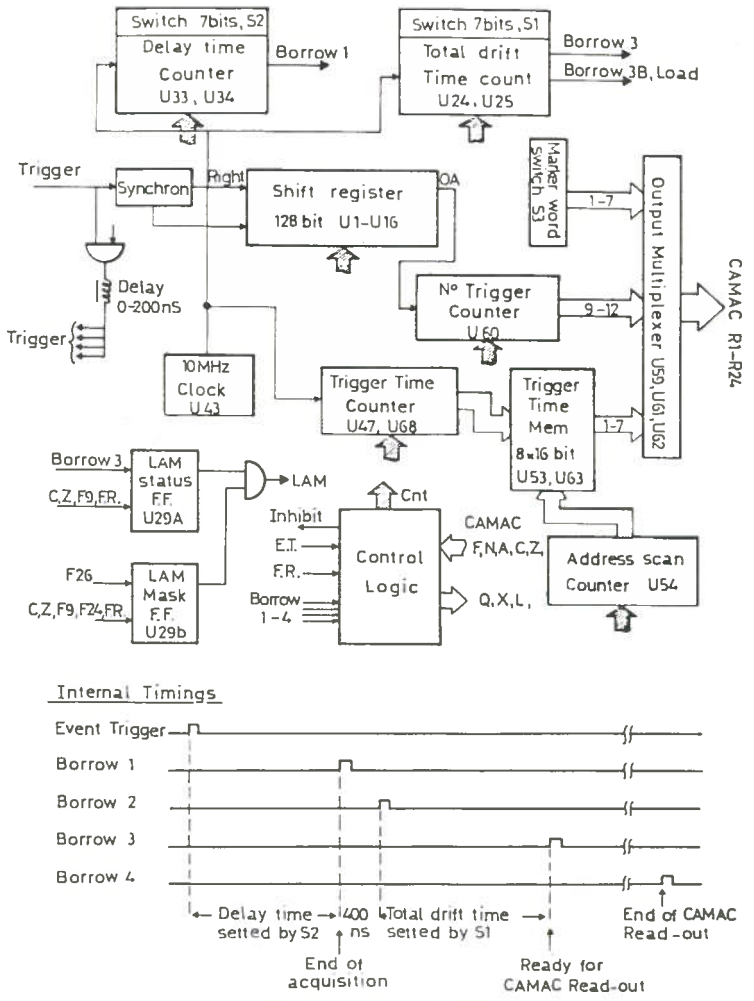


FIG. 7 - Block diagram of the Asynchronous Timing Unit module (ATU).

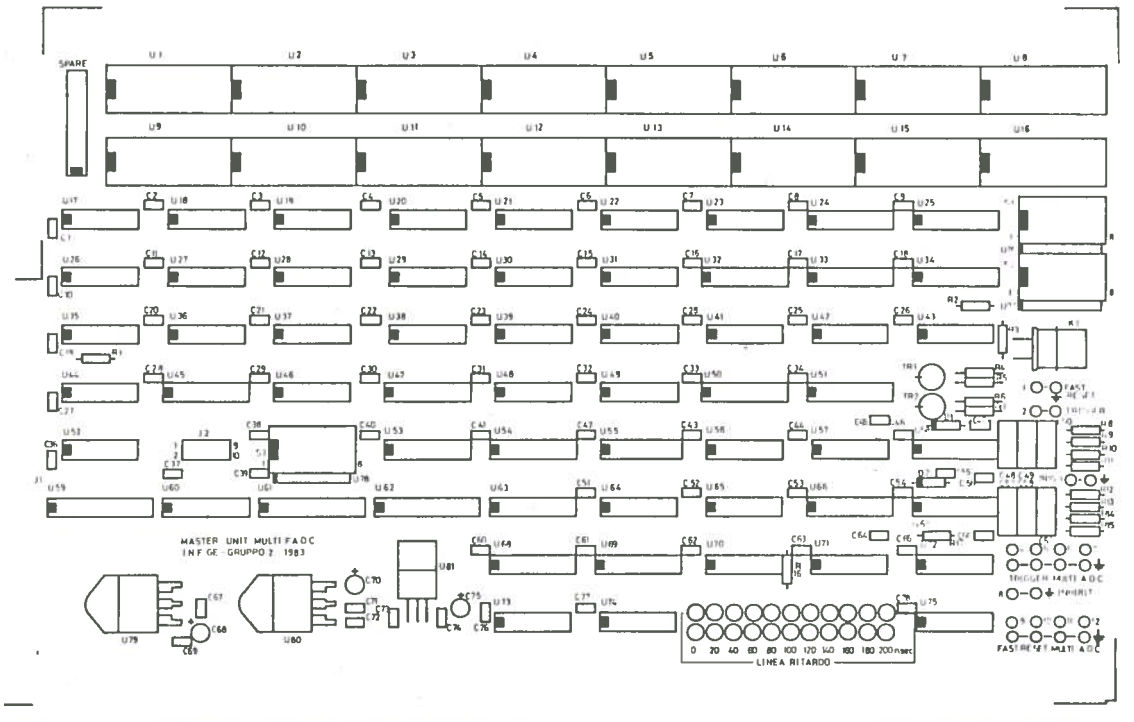


FIG. 8 - Component layout on the ATU printed circuit board.

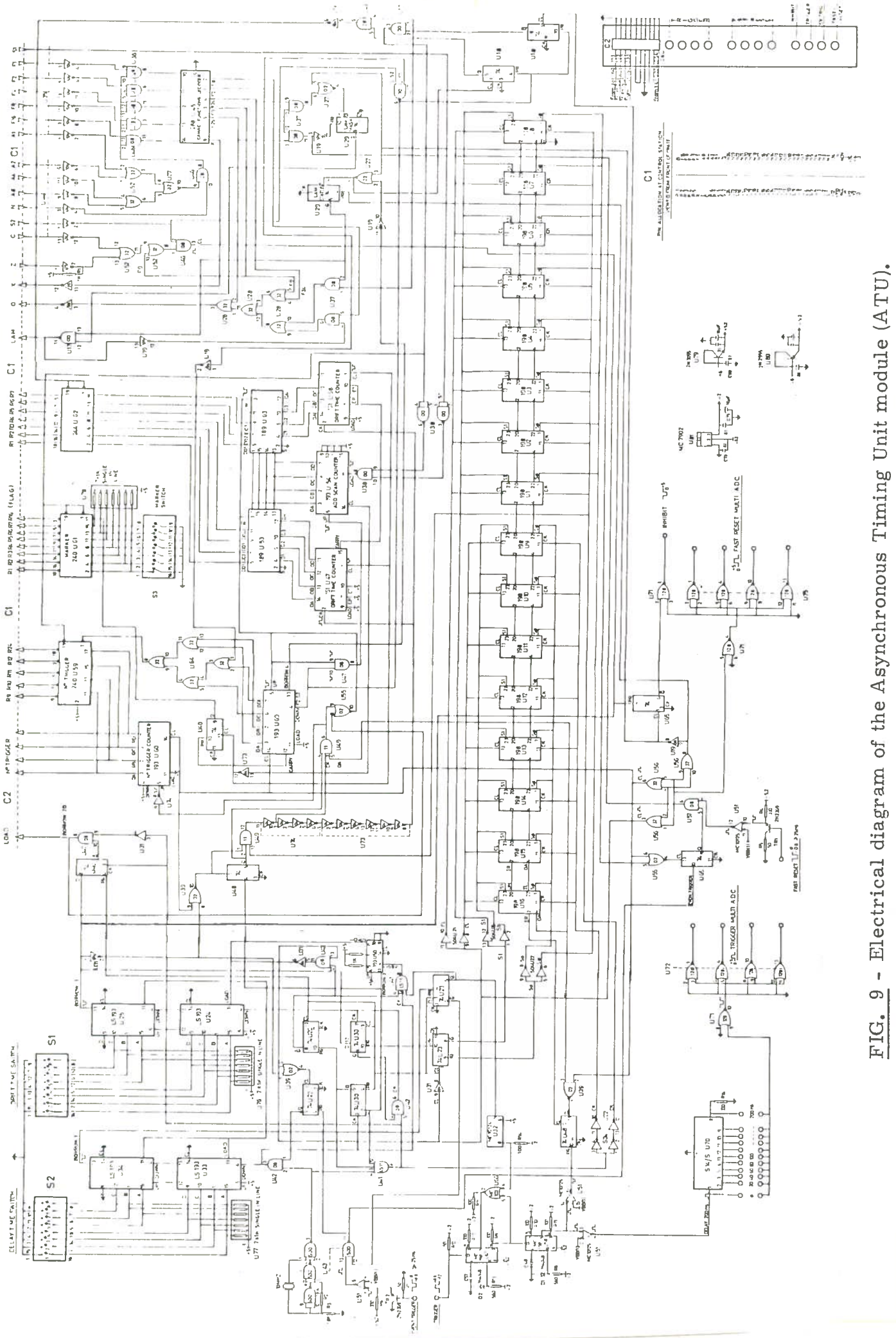


FIG. 9 - Electrical diagram of the Asynchronous Timing Unit module (ATU).

ET : The Delay Time Counter (U33, U34) begins to count down from the inital value set by S2; when zero is reached B1 is generated.

B1 : B1 stops the Trigger pulses going to the Shift Register (U1-U16) and to the Trigger Fanout. After 4 clock pulses the B2 signal is generated.

B2 : The Shift Register (U1-U16) is reversed, the Total Drift Counter (U24, U25) begins to count down from the initial value set by S1. The No. Trigger Counter (U60) begins to count the "1"s read back from the Shift Register (U1-U16), the Time Counter (U47, U68) begins to count the clock pulses and stores its content in the Trigger Time Memory (U53, U63) when an "1" comes from the Shift Register (U1-U16); then the Address Scan Counter (U54) is incremented. When the Total Drift Counter (U24, U25) reaches zero B3 is generated.

B3 : B3 sets LAM status flip-flop. After a further clock cycle (Borrow 3B) the ATU sends a strobe pulse (Load) and the number of Trigger found in the time slice selected by S1 to the No. Trigger Lines. At this moment the system is ready for CAMAC readout or to be reset for a new event.

B4 : Resets the LAM status flip-flop and marks the end of CAMAC readout.

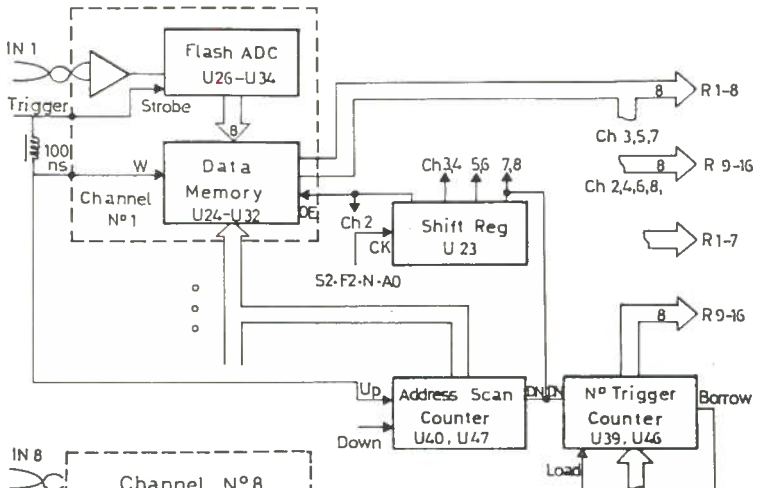
The first Trigger read by CAMAC is the last taken in acqisition (see Fig. 4). The times are measured from the end of the time slot record (see Fig. 4).

4. - CIRCUIT DESCRIPTION OF THE FAST MULTI ANALOG TO DIGITAL CONVERTER (FADC)

In Fig. 10 is reported the block diagram of the ATU, while in Fig. 11 we show the component layout and in Fig. 12 the detailed electrical diagram. In the photograph of Fig. 3 there is an internal view of the FADC.

When a Trigger arrives to the FADC module all the 8 flash ADC channels (U26, U34 for the channel 1) are sampled for 50 ns (Trigger pulse duration) and holded at the leading edge of the pulse. The same Trigger pulse, after a 100 ns delay, gives the write enable to the Data Memories (U24, U32 for the channel 1). When the converted pulse amplitude is stored in the memory, the Address Scan Counter (U40, U47) is incremented by the leading edge of the delayed Trigger pulse. Now the module is ready for another acquisition or to be read by CAMAC.

When the Load signal coming from the No. Trigger connector arrives, the number of acquired Triggers, to be read back via CAMAC, is written into the No. Trigger Counter (U39, U46) and the LAM status flip-flop is set.



DIP SWITCH 1	2	3	4	Total Amp Gain
X	X	X	ON	20.4
X	X	ON	OFF	27.2
X	ON	OFF	OFF	34.0
ON	OFF	OFF	OFF	40.8
OFF	OFF	OFF	OFF	47.6

FIG. 10 - Block diagram of the Fast Multi Analog to Digital Converter module (FADC). In the table the different gain switch configuration are reported.

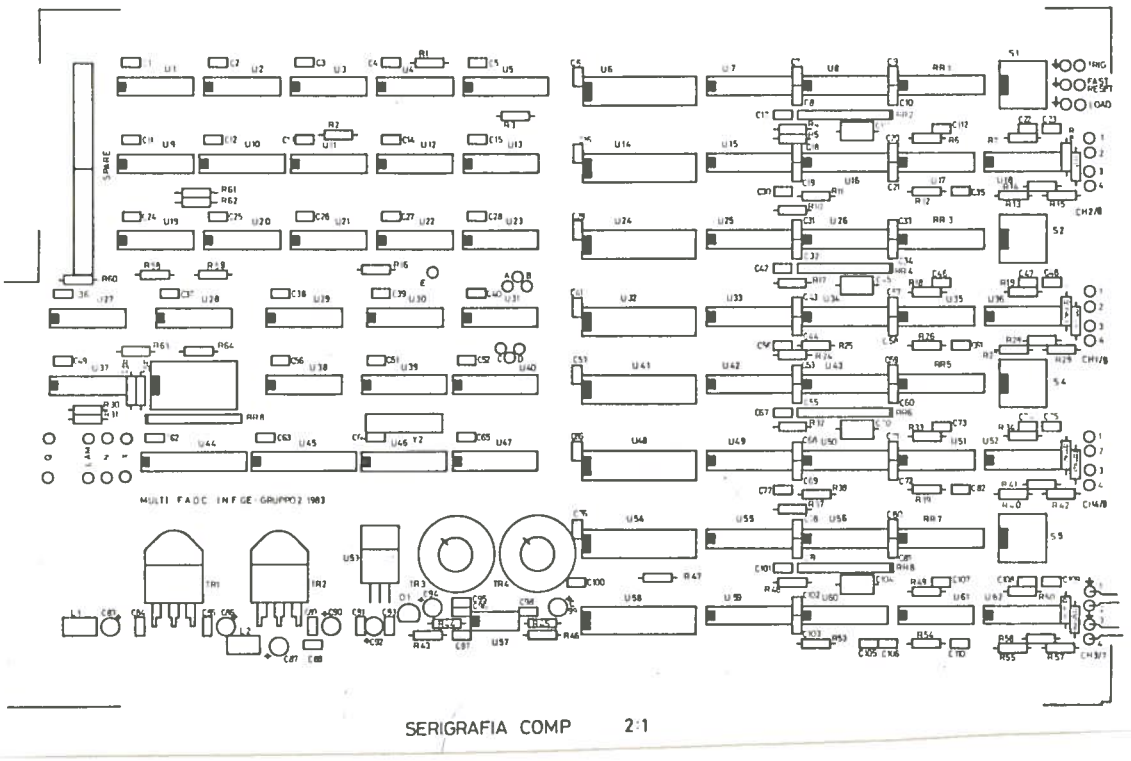


FIG. 11 - Component layout on the FADC printed circuit board.

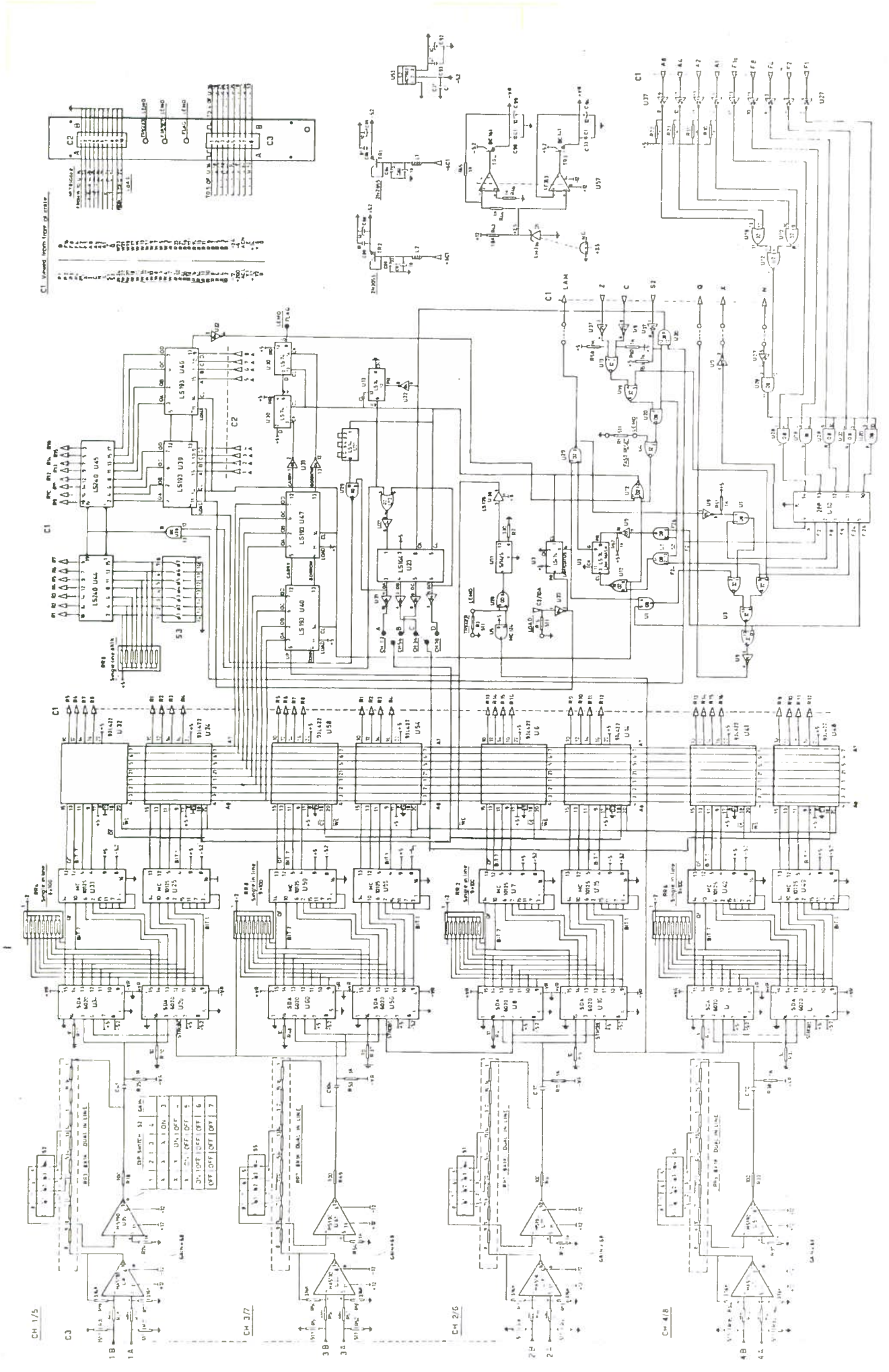


FIG. 12 - Electrical diagram of the Fast Multi Analog to Digital Converter module (FADC).

At each F2 read function two channels are read. With four F2 the eight channels corresponding to the first Trigger are read; then Address Scan Counter (U40, U41) and the No. Trigger Counter (U39, U46) are decremented. When the No. Trigger Counter (U39, U46) reaches zero the LAM status flip-flop is reset.

The input stage amplifier is made using a two stage amplifier chain: the first one is a 50 ohm differential amplifier with a fixed gain of 6.8; the second one has a programmable gain between 3 and 7 by means of a dip switch. The second amplifier and the flash ADC are AC coupled.

5. - TECHNICAL INFORMATION MANUAL FOR THE ATU AND FADC MODULES

5.1. - ATU electrical and mechanical specifications

The ATU electrical and mechanical specifications are:

Time Range : Depends on S2. Maximum time record lenght 12.7 μs (7 bits).

Time Res. : 100 ns that corresponds to a sigma of 40 ns with respect to the Event Trigger and a sigma of 30 ns with respect to the other acquired Triggers.

Pulse Separ. : Must be $\geq$ 200 ns.

Power Supply : +6 V, 1.7 A
- 6 V, 0.4 A.

5.2. - FADC electrical and mechanical specifications

The FADC electrical and mechanical specifications are:

Input Voltage : Depends on selected amplifier gain. The dinamic range of the internal ADC is 5 Volts.

Resolution : 7 bits.

Power Supply : +6 V, 2.6 A
- 6 V, 1.9 A
+12 V, 0.3 A
- 12 V, 0.3 A

Mechanics : Two CAMAC units.

In Fig. 5 the differential linearity and the gain differences between the eight channels of a FADC module are shown. In Fig. 6 the eight input signal are reconstructed using the recorded data from the ATU and FADC.

5. 3. - ATU inputs

In the ATU module we have the following front pannel inputs :

Trigger : LEMO connector, ECL logic, width ≥ 10 ns, minimum pulse separation 200 ns. Triggers the time digitizer.

Fast Reset : LEMO connector, NIM logic, width ≥ 25 ns. Active from Event Trigger until F26. Resets the module.

Event Trigger : LEMO connector, NIM logic, width ≥ 25 ns, active from C, Z, F9, Fast Reset, not active after the first one. Stops the system after the Time Delay and prepares the data for the output.

5. 4. - FADC inputs

In the FADC module we have the following front pannel inputs :

Analog Input : 8 channels flat cable connector, channels 1 to 8 from up to down. Differential 50 Ohm analog signal, positive input right side, negative input left side.

Trigger : LEMO connector, TTL logic, from ATU Trigger fanout. Strobes the ADCs.

Fast Reset : LEMO connector, TTL logic, from ATU Fast Reset fanout. Resets the module.

No. Trigger : Flat cable connector, TTL logic. System internal use.

5. 5. - ATU outputs

In the ATU module we have the following front pannel outputs :

Trigger : LEMO connector, TTL logic, fan-out for 4 FADC modules of Trigger input. The pulse can be delayed from 20 to 200 ns in 20 ns steps.

Fast Reset : LEMO connector, TTL logic, fan-out for 4 FADC modules of Fast Reset input.

Inhibit : LEMO connector, TTL negate logic, true from C, Z, F9, Fast Reset to the end of conversion started by Event Trigger.

No. Trigger : Flat cable connector, TTL logic. System internal use.

5. 6. - FADC outputs

In the FADC module we have the following front pannel outputs :

Flag : LEMO connector, TTL negate logic. The Flag becomes true when data memory locations not written after the last C, Z, F9 or Fast

Reset are read via CAMAC. This Flag can be used as system debug ging tool.

5. 7. - ATU switches

In the ATU module we have the following switches (Sx) and bridges (Bx) (their position on the printed circuit board are shown in Fig. 8):

S1 : 8 bits switch of which only bits 1 to 7 are used. S1 selects the time slot in which we look for the recorded Triggers. The time range of the S1 switch is from 0 to 12.7 μs in 0.1 μs steps.

S2 : 8 bits switch of which only bits 1 to 7 are used. S2 selects the Delay Time from the Event Trigger signal to the stop of the Trigger acquisition. The time range of the S2 switch goes from 0 to 12.7 μs in 0.1 μs steps. A fixed of set of 300 ns is added.

S3 : 8 bits switch of which only bits 1 to 7 are used. S3 sets a number between 0 and 127 in the bits 1-7 of the ATU Marker Word.

B1 : Selects the delay from Trigger (in) to Trigger fanout (out). The delay ranges from 0 to 200 ns in 20 ns steps. The ADCs of the FADCs are strobed with the selected delay added to a fixed 70 ns delay.

5. 8. - FADC switches

In the FADC module we have the following switches (Sx) (their position on the printed circuit board are shown in Fig. 11) :

S1 : Sets the gain of the amplifier chain of channel 2, in upper board, and of channel 6, in lower board. The gain can be selected between 3*6.8 and 7*6.8 in five steps (see Fig. 10 for gain/switch configurations).

S2 : Sets the gain of the amplifier chain of channel 1, in upper board, and of channel 5, in lower board. The gain can be selected between 3*6.8 and 7*6.8 in five steps (see Fig. 10 for gain/switch configurations).

S3 : 8 bits switch of which only bits 1 to 7 are used. S3 sets a number between 0 and 127 in the bits 1-7 of the FADC Marker Word.

S4 : Sets the gain of the amplifier chain of channel 4, in upper board, and of channel 8, in lower board. The gain can be selected between 3*6.8 and 7*6.8 in five steps (see Fig. 10 for gain/switch configurations).

S5 : Sets the gain of the amplifier chain of channel 3, in upper board, and of channel 7, in lower board. The gain can be selected between 3*6.8 and 7*6.8 in five steps (see Fig. 10 for gain/switch configurations).

5. 9. - CAMAC functions

In the ATU and FADC modules the following CAMAC functions have been implemented (the station N address corresponds to the higher address of the ATU and FADC two units module):

Z : Initializes the acquisition system, resets the LAM mask and LAM status flip-flop, sets the system in acquisition mode.

C : Same as Z.

F2 : F2 with N, A0 performs the reading of the data, Q and LAM status are true while there are valid data, L-line is true if LAM mask flip-flop is set. The Q and LAM status flip-flop are false if an Event Trigger is not arrived after the last Z, C or F9 functions.

F8 : F8 with N, A0 performs the reading of the LAM status flip-flop, Q corresponds to the LAM status flip-flop.

F9 : F9 with N, A0 performs the same functions as C or Z, Q is always true.

F24 : F24 with N, A0 resets the LAM mask flip-flop, Q is always true.

F26 : F26 with N, A0 sets the LAM mask flip-flop, Q is always true.

The system is organized in such a way that it is possible to use the Q and LAM signals for block data transfer read operation[7]. The implemented block data transfer modes are Q-repeat-on-LAM (used with ROMULUS[8-11]) or Q-stop.

A typical CAMAC command sequence for the ATU or the FADC module may be:

a) ROMULUS data acquisition

- C, or Z, or F9, N, A0 : Initializes the system.
- ET : An Event Trigger is arrived.
- F26, N, A0 : ROMULUS "prepare and go" that generates a DMA transfer with repeated F2, N, A0 while LAM is true.

b) CAMAC data acquisition

- C, or Z, or F9, N, A0 : Initializes the system.
- F26, N, A0 : Unmasks LAM.
- ET : The Event Trigger generates the LAM in the ATU and in the driven FADCs.
- F2, N, A0 : Repeated read command while Q is true (Q-stop).

In Fig. 4 the organization of the output data records of the ATU and of the FADC modules is shown. The Flag in the ATU Marker Word means that more then 14 Trigger have been taken. In this case the correlation between the ATU and the FADC data is wrong.

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