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THEORY AND REALIZATION OF A NEW CURRENT PULSE COMPRESSION CIRCUIT

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Abstract

In this work a new circuit to compress a pulse current utilizing transmission lines and transistor switches is proposed. It demonstrated a time compression factor of 2 on a low load impedance. A 12 m, 50 Ω coaxial transmission line provided a current pulse of 3 A, 120 ns. A 6 m, 50 Ω storage line connected to main line was able to store the 50% of the initial pulse. A fast switch was used in order to close both lines on a halved load impedance with respect to the transmission line characteristic one. We obtained a current pulse compression recording an output current of 6 A, 60 ns.

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I. Introduction

Pulsed power technology[1] is very interesting to develop devices that need of high current or voltage pulses. Some examples of applications are Marx circuits for electron beam generators[2], microwave pulse generators[3], fast X ray generators[4] and laser devices with fast charge transfer type circuits[5].

The use of transmission line pulsers composed by a single line, devoted in pulse generation, halves the output voltage in application with matched loads. In these single pulse forming lines (SPFL) the corresponding current pulse is as high as $V_0 / 2R_0$, where V_0 is the charging voltage of the line and R_0 its characteristic impedance. Fig. 1 shows a sketch of the SPFL.

To increase the current value, it is necessary to low the load impedance. This procedure will introduce reflections in the circuits owing to the mismatching of the signal and a consequence of that is the presence of many pulses along the line and an increase of the transferring time. Many efforts have been done to generate high voltage and current without reflections[6].

Anyway, considering a SPFL having a load impedance lower than its characteristic impedance, the reflections can be eliminated by connecting an extra line of the same characteristic impedance and charging voltage to the same load. This schema does not allow any current between the lines but only between the lines and the load. Therefore, we have an increase of the current. The higher current achieved into the load must counterbalance the voltage decrease due to the low load impedance used. Supposing a charging voltage V_0 and a load impedance $R_0/2$, with R_0 the characteristic impedance of the line, we expect a matched output pulse of current V_0/R_0 and voltage $V_0/2$. The latter is the output voltage value yielded by a matched line. Figure 2 shows a sketch of the current pulse forming line (CPFL).

To assess the analytic value of the voltage and current, and the absence of reflections, we study the behaviour of the signals along the lines. The pulser of Fig. 2 can be considered as two different lines, *a* and *b*, closed on the same load.

Let us consider only the line *b*. The voltage and current along the line are governed by the following equations[7]:

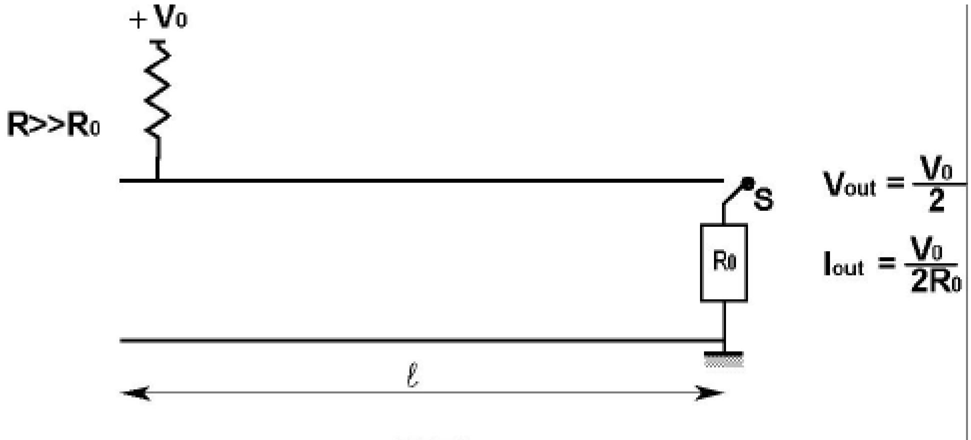
$$V(x,p) = a_1 e^{-ptx} - a_2 e^{ptx} + V_0/p \qquad (1)$$

$$I(x,p) = \frac{a_1}{R_0} e^{-ptx} + \frac{a_2}{R_0} e^{ptx} \qquad (2)$$

where $V(x,p)$ and $I(x,p)$ are the Laplace transforms of voltage and current, t is the delay per unit length of the line, a_1 and a_2 are coefficients due to the boundary conditions. At $x=l$ the current is zero, while at $x=0$ the voltage on the load is the sum of the product of line *a* and *b* currents times the load impedance *R*:

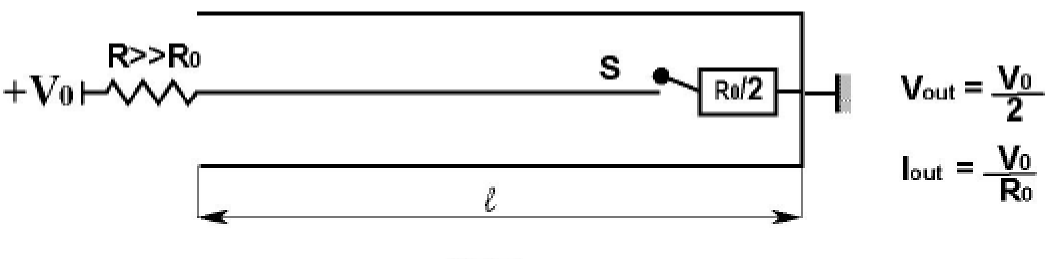
$$\frac{a_1}{R_0} e^{-ptl} + \frac{a_2}{R_0} e^{ptl} = 0 \qquad (3)$$

$$a_1 - a_2 + V_o/p = 2I(0,p)R = -2(a_1 + a_2)R \qquad (4)$$



SPFL

Fig. 1. *Schematic sketch of a SPFL closed on its characteristic impedance R_0. S: fast switch; R: charging resistor.*



CPFL

Fig. 2. *Schematic sketch of a CPFL, closed on its load impedance $R_0/2$. S: fast switch; R: charging resistor.*

Supposing $R = R_o/2$ and solving the above equations, we obtain the expressions of:

$$a_1 = -V_0 / 2p \quad \text{and} \quad a_2 = V_0 / 2p\, e^{-2pt l}$$

Substituting the found coefficients into the Eqs. (1) and (2) and antitransforming, the space-temporal expression of the voltage and current along the lines becomes:

$$v(x,t) = V_0[u(t) - \frac{u(t-tx)}{2} - \frac{u(t-t(2l-x)}{2}] \qquad (5)$$

$$i(x,t) = \frac{V_0}{2R_0}[-u(t-tx) + u(t-t(2l-x)] \qquad (6)$$

while the voltage and current on the load is obtained putting $x=0$ and considering the boundary condition $i_R = -2i(0,t)$, that is:

$$v_{out}(t) = \frac{V_0}{2} \quad \text{for} \quad 0 < t < 2tl$$

and

$$i_{out}(t) = \frac{V_0}{R_0} \quad \text{for} \quad 0 < t < 2tl$$

At the moment, a simple method able to generate rectangular pulses of V_0 voltage but with a V_0 / R_0 current, does not exist and many applications require high current pulses of short time duration.

In this note, we realize a novel compression circuit (NCC) studied in Ref. 8, utilizing transmission lines having characteristic impedance R_0, fast transistor switches and a load impedance of $R_0/2$. That is, a transmission line (TL) l long is used as a pulse forming line charged at V_0 and a transmission line (SL) $l/2$ long is used as a storage line. Two fast high voltage transistors (S1, S2) are used as switches. Fig. 3 shows the schema of the novel circuit. At $t \le 0$ the switches S1 and S2 are open and the TL line is charged at V_0 voltage. At the time $t = 0$, S1 switches on the line TL on SL and a leading edge of voltage $-V_0/2$ and current $I_o = V_0/2R_0$ travels in the TL with velocity $v = 1/t$, while a pulse of voltage $V_0/2$ and current I_0 travels in the SL with the same velocity for $0 \le t \le l/2\, t$, see Fig. 4a. For $l/2\, t \le t \le tl$ a reflected pulse of voltage $V_0/2$ and current $-I_0$ is generated in the SL due to its open end. This pulse travels along the line with opposite velocity with respect to the injected one (see Fig. 4b). Fig. 4c shows the voltage and current waveforms at $t = tl$. Now, S2 switches on and both TL and SL currents are led on the $R_0/2$ load. The shape of the voltage and current pulses are shown in Fig. 4d for $tl < t < 3/2tl$ and in Fig. 4e for $3/2tl < t < 2tl$, after the reflection at the SL open end. Consequently, the propagating current in the TL, I_0, as well as the upstream current pulse in the SL, $-I_0$, add themselves in the $R_0/2$ load producing a voltage pulse $V_0/2$ and a current pulse V_0/R_0 for a time $tl < t < 2tl$. One can note that the current is doubled, the pulse duration halved and the absence of reflections.

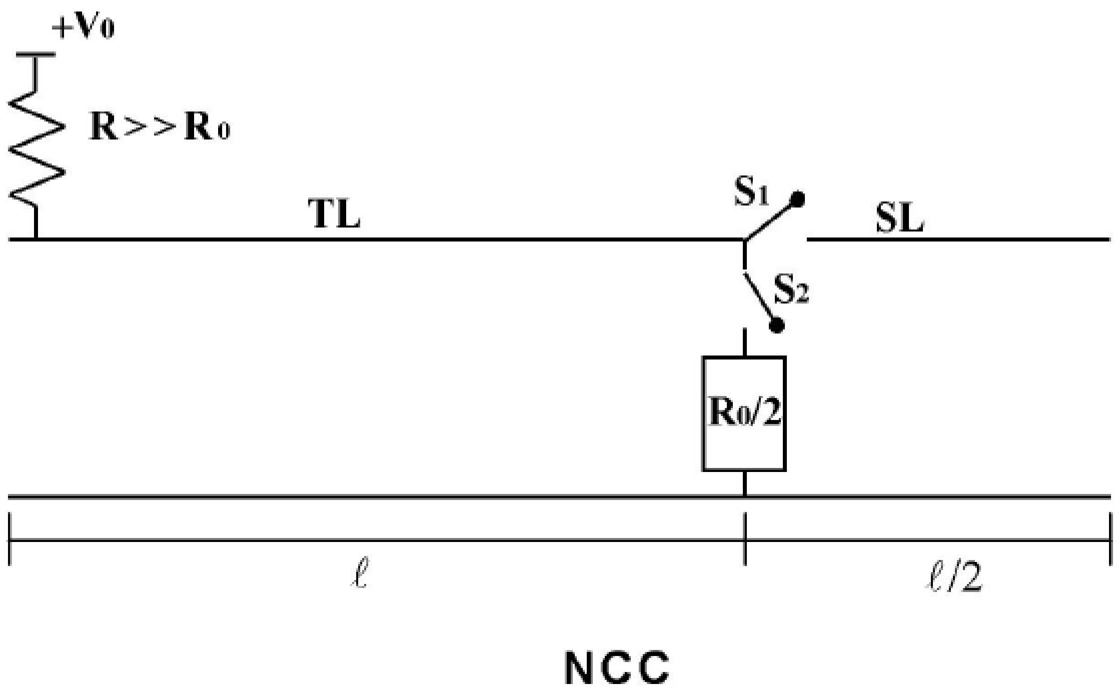


Fig. 3. *Schematic sketch of the current compression circuit, NCC. TL: R_0 characteristic impedance transmission line; SL: R_0 characteristic impedance storage line; R_0/2: load impedance; R: charging resistor; S1 and S2: fast switches.*

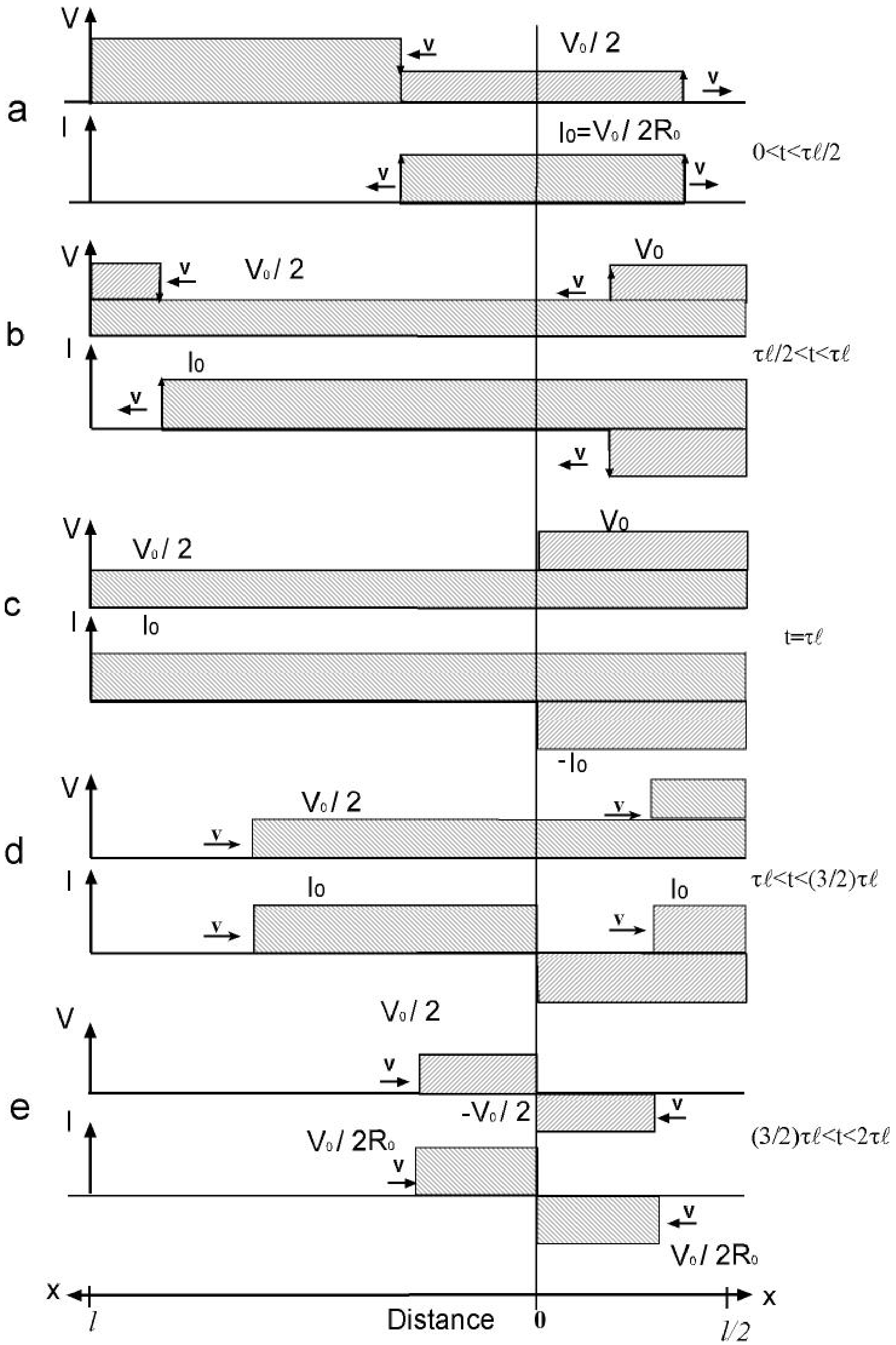


Fig. 4 *Diagram of the voltage and current along the line at a)* $0 < t < \frac{l}{2}t$ *; b)* $\frac{1}{2}tl < t < tl$ *; c)* $t = tl$ *; d)* $tl < t < \frac{3}{2}tl$ *; e)* $\frac{3}{2}tl < t < 2tl$*.* ***v*** *is the pulse velocity.*

II. Experimental apparatus and results

In our NCC experimental set-up we used a 12 m and 6 m long 50 Ω coaxial cable as TL and SL, respectively; $t = 5$ ns/m for both transmission lines. Two fast transistor switches (TS1, TS2) (Behlke HTS 21-14) were utilized as the S1, S2 switches and consequently a 25 Ω resistor as load impedance. The charging voltage V_0 (300 V) is given by means of a power supplier and a charging resistor R much larger than *Ro*. Fig. 5 shows a sketch of the circuit, where the voltage signals are measured by means of two high impedance probes, P1 and P2.

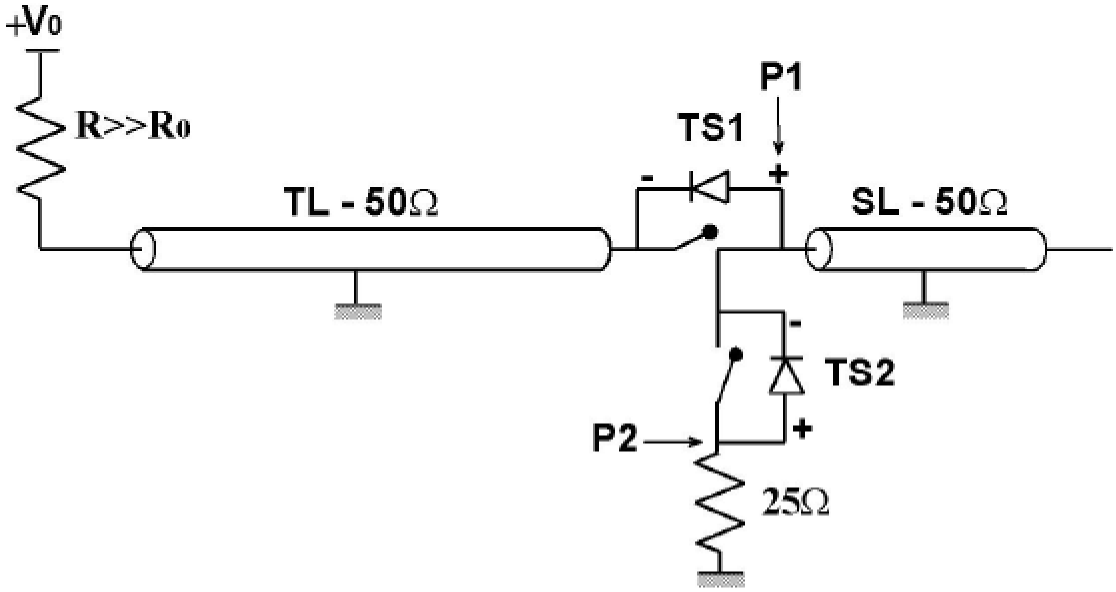


Fig. 5. *Schematic sketch of the NCC apparatus. TL: 50 W, 12 m long transmission line used as SPFL; SL: 50 W, 6 m long storage line; R: charging resistor: TS1 and TS2: (Behlke HTS 21-14) fast transistor switches; 25 W: load impedance; P1 and P2: high impedance oscilloscope probes.*

At $t = 0$, TS1 switched on injecting a pulse of $V_0 / 2$ voltage and $V_0 / 2R_0$ current value into the SL line. After 60 ns the SL line resulted charged at V_0 and then also TS2 switched on by means of an external trigger circuit. The experimental results are shown in Fig. 6. The lower trace shows the voltage pulse at the exit of the TL line. Its duration was about 120 ns (FWHM) and its amplitude 150 V. It presents a little peak over its plateau after 60 ns its onset time, owing to capacity effect of the

TS2 transistor during its closing. The upper trace shows the compressed output pulse on the load impedance, with amplitude of about 150 V, duration of 60 ns and current of 6 A.

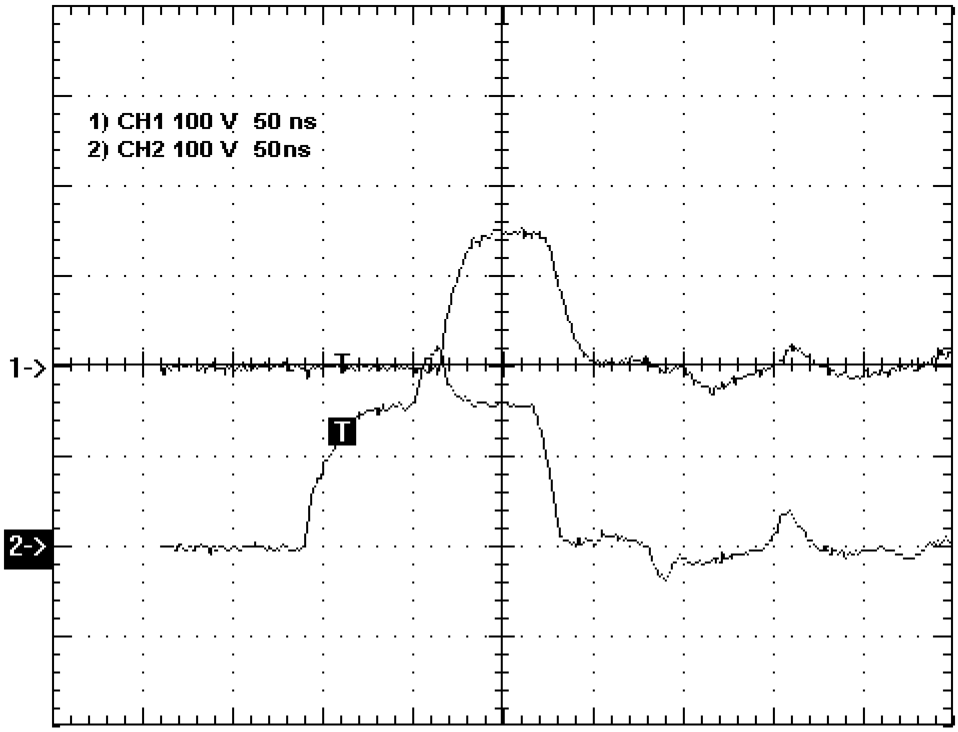


Fig. 6: *Waveform of the voltage pulse obtained by the NCC with a charging voltage of 300 V. Lower trace shows the waveform voltage at the exit of the TL line; Upper trace shows the voltage waveform on the 25 W load resistor. The maximum output current was 6 A.*

We have compared the above results with the ones obtained by a CPFL circuit. It was formed by two 12 m long 50 Ω coaxial cable transmission lines (TL) coupled to a 25 Ω?load resistor by a fast transistor switch (TS) (Behlke HTS 21-14), see Fig. 7. The cables were charged by means of a power supplier at 300 V and a charging resistor much larger than R_0. The voltage signals were measured by means of an high impedance probe (P) as shown in Fig. 7. A TTL signal triggered the transistor switch connecting both lines to the load, providing a voltage and current pulse of about 150 V, 6 A and 120 ns (Fig. 8, lower trace).

The upper trace of Fig. 8 shows the experimental result of the circuit having only one line TL. In this case the signal is mismatched and more pulses are present after the first one. We can observe that the current intensity of the first pulse is as large as about 4 A and the output voltage 100 V.

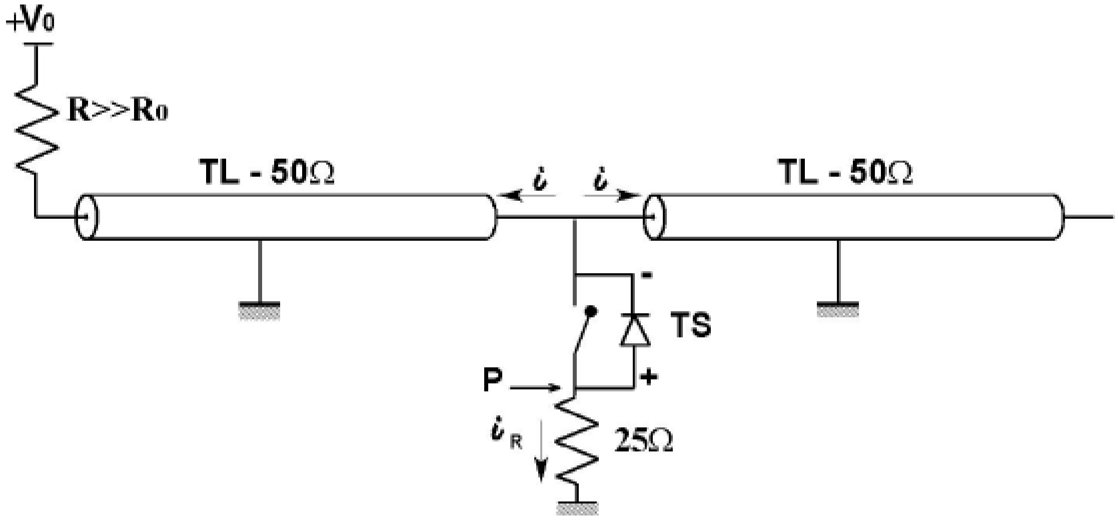


Fig. 7. *Schematic sketch of the CPFL apparatus. TL: 50 W, 12 m long transmission line; R: charging resistor; TS: Behlke HTS 21-14 fast transistor switch; 25 W: load impedance; P: high impedance oscilloscope probe.*

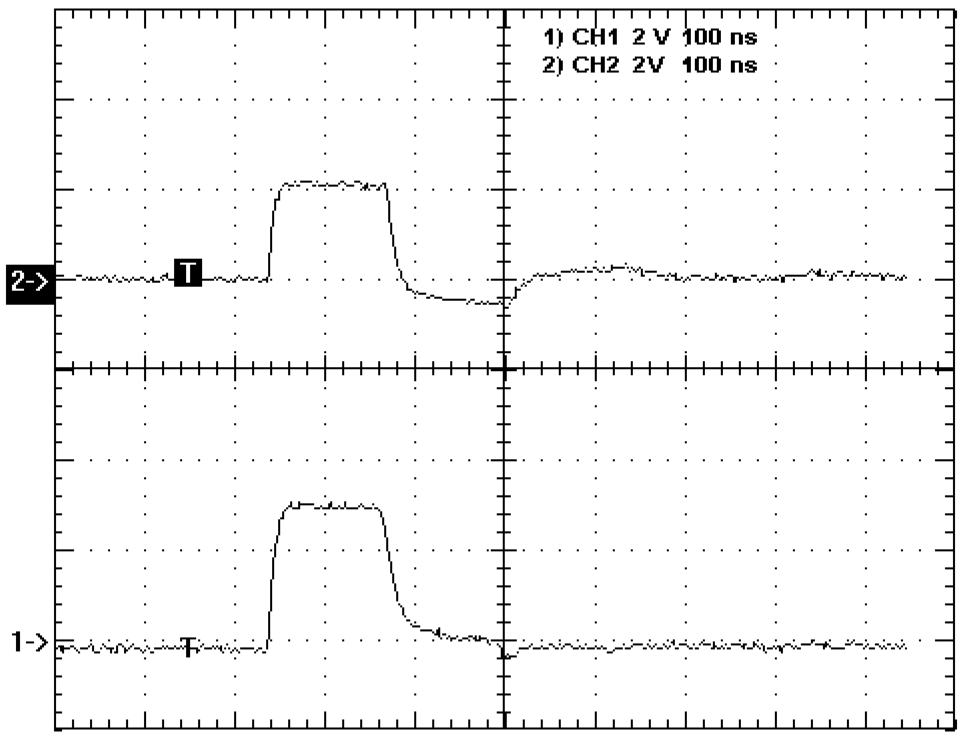


Fig. 8: *Waveform of the voltage pulse obtained by the CPFL circuit with a charging voltage of 300 V. Upper trace shows the voltage waveform of only one TL line closed on 25 W load resistor; Lower trace shows the matched voltage pulse.*

A potential application of the NCC circuit could be high current electron beam or X-ray production. In fact, applying a field emission diode and varying its cathode-anode distance in order to get a load impedance corresponding to $R_0/2$, it was possible to match the output pulse. The maximum output current can be calculated by the following Langmuir-Child law, $I = pV^{3/2}$ where the diode perveance value, p, increases of a factor 2.

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