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Method of punch-through voltage stabilisation in silicon detectors.

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Abstract

Dealing with large-scale application of semiconductor detectors, one of the keystones is to ensure the robustness and long-term electrical stability. A phenomenon that can compromise the performance of a system based on these detectors is the dependence of the *punch-through* effect on the environmental conditions. In this paper we investigated the influence of humidity on the *punch-through* in microstrip and drift silicon detectors. Simulations and laboratory measurements on different prototypes were performed. Data analysis allowed to determine a special solution for the design of the cathode metallisation mask that reduces in a substantial way the evolution of the *punch-through* voltage due to humidity influence.

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1 Punch-through.

Let us consider a simple structure composed by two p^+ cathodes implanted on a n-type substrate, as shown in figure 1. Applying to both cathodes the same negative voltage with

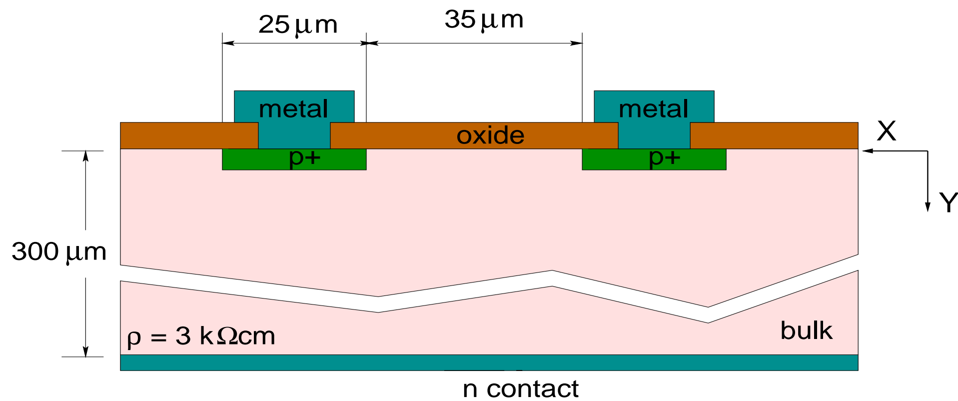

Figure 1: Sketch of the structure used for the simulations.

respect to the n-bulk contact, we obtain the potential distribution represented in figure 2. This is the result of a simulation carried out with ATLAS Device Simulator [1] solving both the Poisson's equation and the carrier continuity equations. This approach allows to get a full description of the structure in terms of electrical quantities.

The potential saddle between the cathodes is clearly visible in the plot. Its height de-

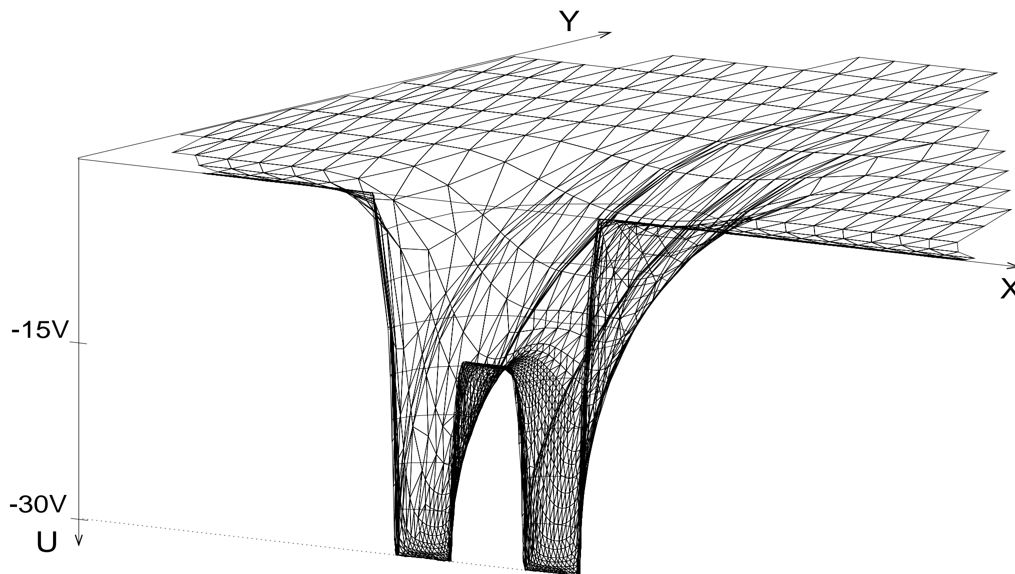

Figure 2: Potential distribution when the cathodes are at the same potential.

pends on many parameters: the bulk resistivity, the presence of field-plates, the distance between the cathodes and the oxide charge density. The saddle acts as a potential barrier when, starting from this bias condition, we further decrease the potential of one cathode. Indeed, it avoids the flowing of holes from one cathode to the other. This condition is preserved until the voltage difference exceeds the barrier height, as shown in figure 3. In this

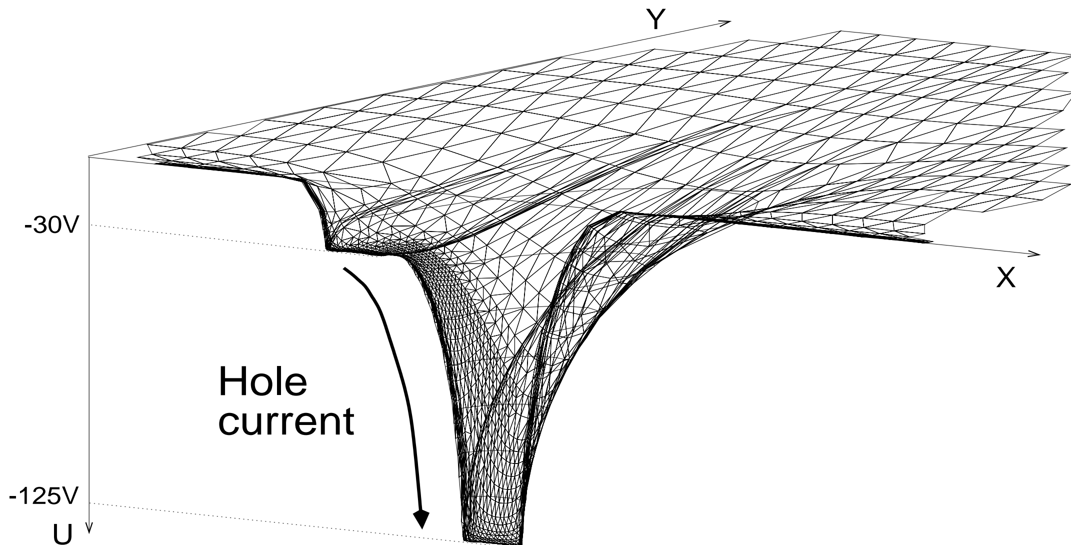

Figure 3: The potential saddle is compensated by the voltage difference.

situation a hole current is allowed to flow from the more positive cathode to the negative one following a path that depends on the position of the weakest point of the barrier. In

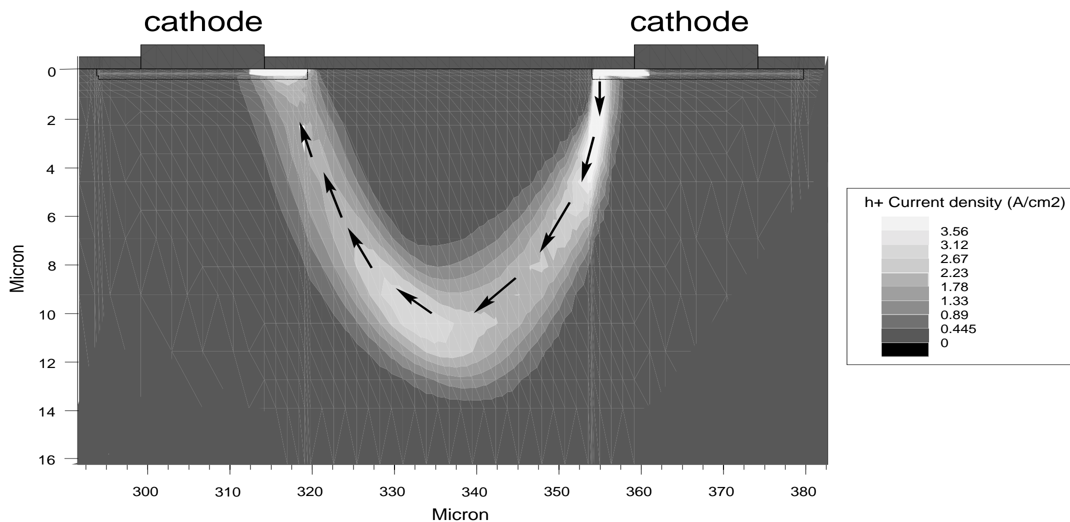

Figure 4: Hole current density.

particular, for a given structure, the higher is the oxide charge density the longer is the

trajectory. In this specific case the density is $Q_{ox} = 1 \times 10^{11}\ q/cm^2$ and the resulting path is shown in figure 4.

The graphs in figure 5 show the current of the two cathodes as a function of the voltage

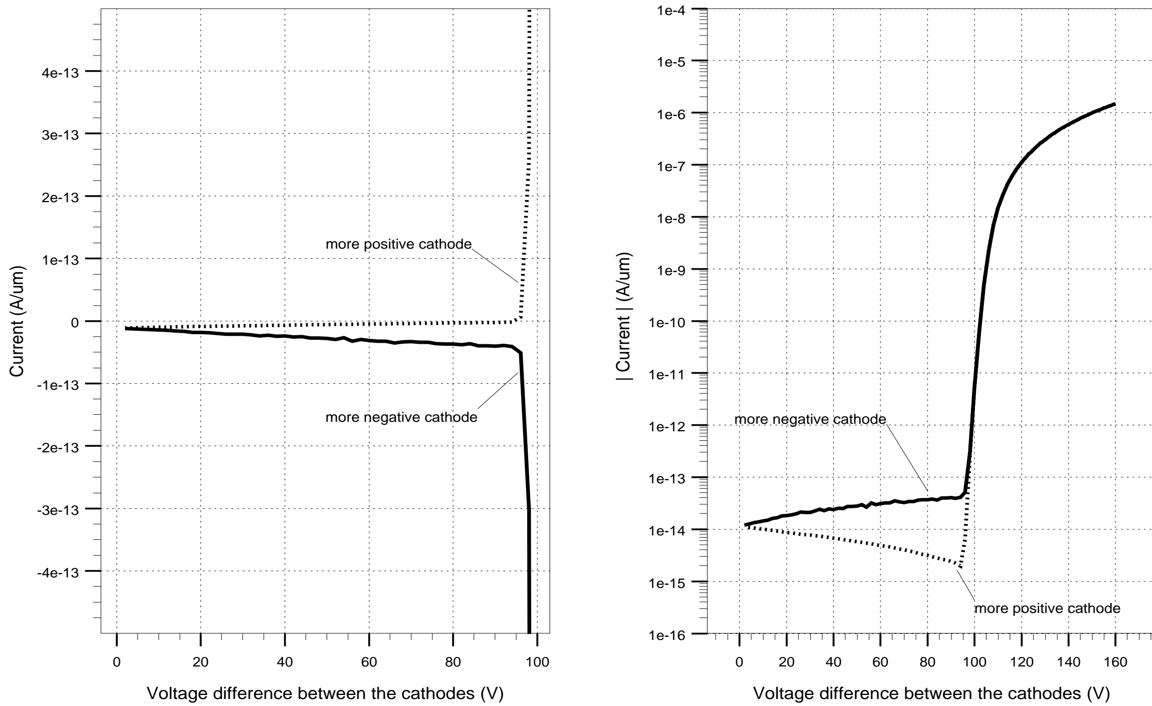

Figure 5: Cathodes current as a function of the voltage difference between them.

difference between them. When the electrodes are at the same potential the number of holes collected by the two cathodes is the same and it is determined by the generation lifetime in the depleted region. Then, as the voltage difference grows, the current of the more negative cathode slightly increases because of the more extended depletion volume. Around $95V$ there is an abrupt rising of both currents. At this point the more positive cathode starts to emit holes towards the other and its current changes the sign. We refer to this voltage as *punch-through voltage (V_{pt})*, and we call this phenomenon *punch-through*.

Since the *punch-through* process is related to the potential saddle between the cathodes, the parameters which determine the barrier height will affect also the *punch-through* voltage. At this point we have to note that a real device usually contains a large number of cathodes and the example proposed above serves only to illustrate the *punch-through* phenomenon. In case of many cathodes the depletion dynamics is different and this affects the *punch-through* voltage. As an example, figure 6 displays V_{pt} as a function of the fixed oxide charge for two geometries. One is the two-cathode structure previously described,

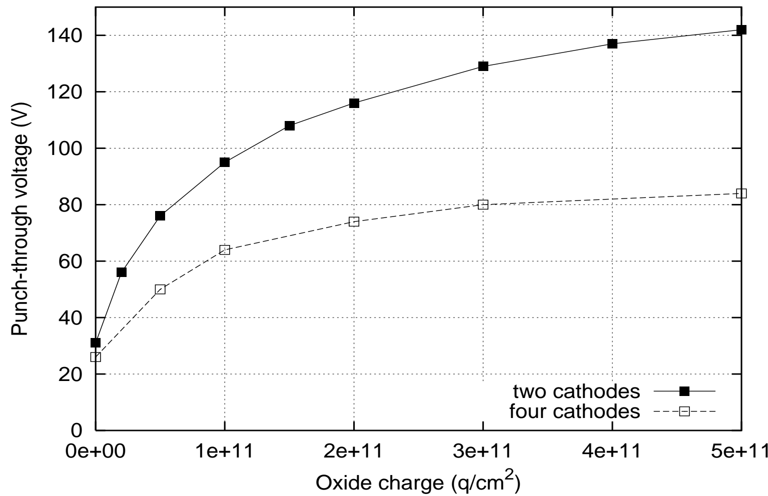

Figure 6: *Punch-through* voltage as a function of the oxide charge density for a two-cathode structure and for a four-cathode structure.

while the other is a structure with four cathodes which is a good approximation of a real situation. Since the values calculated for the two cases are substantially different, in the

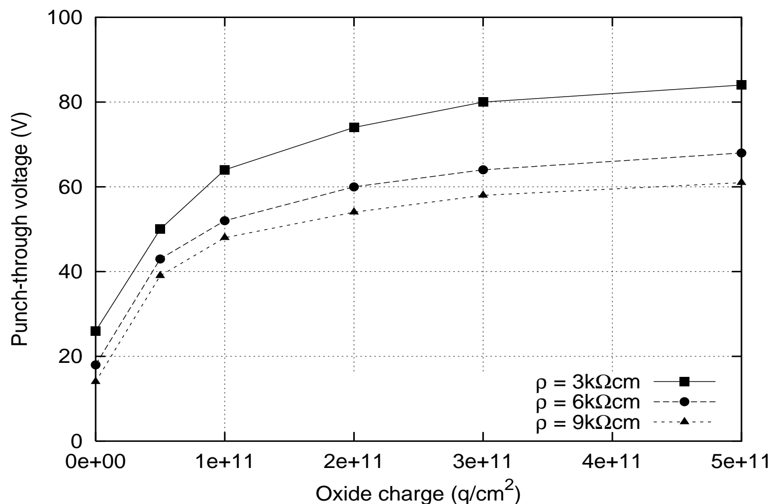

Figure 7: *Punch-through* voltage as a function of the oxide charge density for different bulk resistivities.

following considerations we will use the structure with four cathodes.

As it was mentioned above, the *punch-through* voltage depends on different parameters. Figure 7 shows the *punch-through* voltage as a function of the oxide charge density for different bulk resistivities typical for silicon detectors. The behaviour of V_{pt} is clear considering that the increase of both the oxide charge density and the bulk dopant concentration make deeper the potential saddle between cathodes.

2 Measurements.

In order to confirm the simulation results we performed *punch-through* voltage measurements using silicon structures with the geometry employed in the calculation. All samples had a bulk resistivity of $3\,k\Omega \cdot cm$.
The measurement technique is shown in figure 8. We used a probe station with five probe

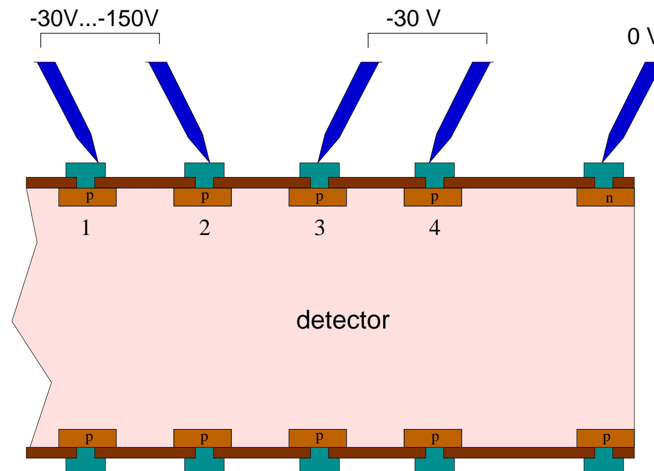

Figure 8: Sketch of the measurement technique.

needles. One gives the ground potential to the bulk, two are kept at $-30V$, while a voltage ramp, starting from $-30V$, is applied to the remaining two needles. The *punch-through* voltage is the potential difference between cathodes n.2 and n.3 at which the current of the strip n.3 changes sign. As an example, figure 9 depicts the absolute value of the cur-

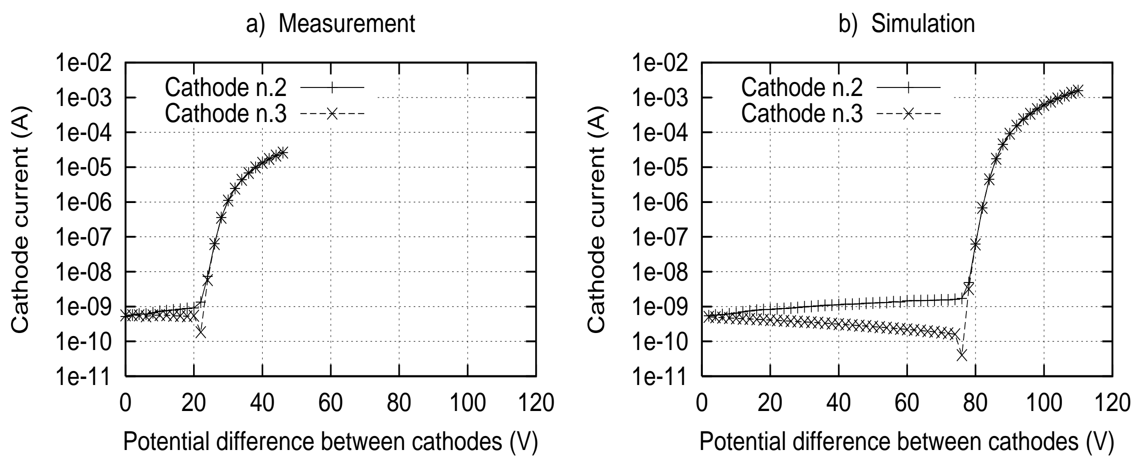

Figure 9: Absolute value of the current for the cathodes n.2 and n.3 as a function of the voltage difference between them.

rent for the cathodes n.2 and n.3 as a function of the voltage difference between them. A comparison between simulation and measurement reveals the similar shape of the current curves while the measured *punch-through* voltage is significantly lower than the simulated one.
Investigating the origin for this discrepancy we found that the measured *punch-through* voltage is time dependent. To illustrate this we implemented the following measurement procedure. We raise the negative potential of the cathodes n.1 and n.2, by steps of $1V$, up to the *punch-through* voltage. At this point we retrogress one step and wait for the coming of the *punch-through*. This is repeated till the *punch-through* voltage is stabilised.

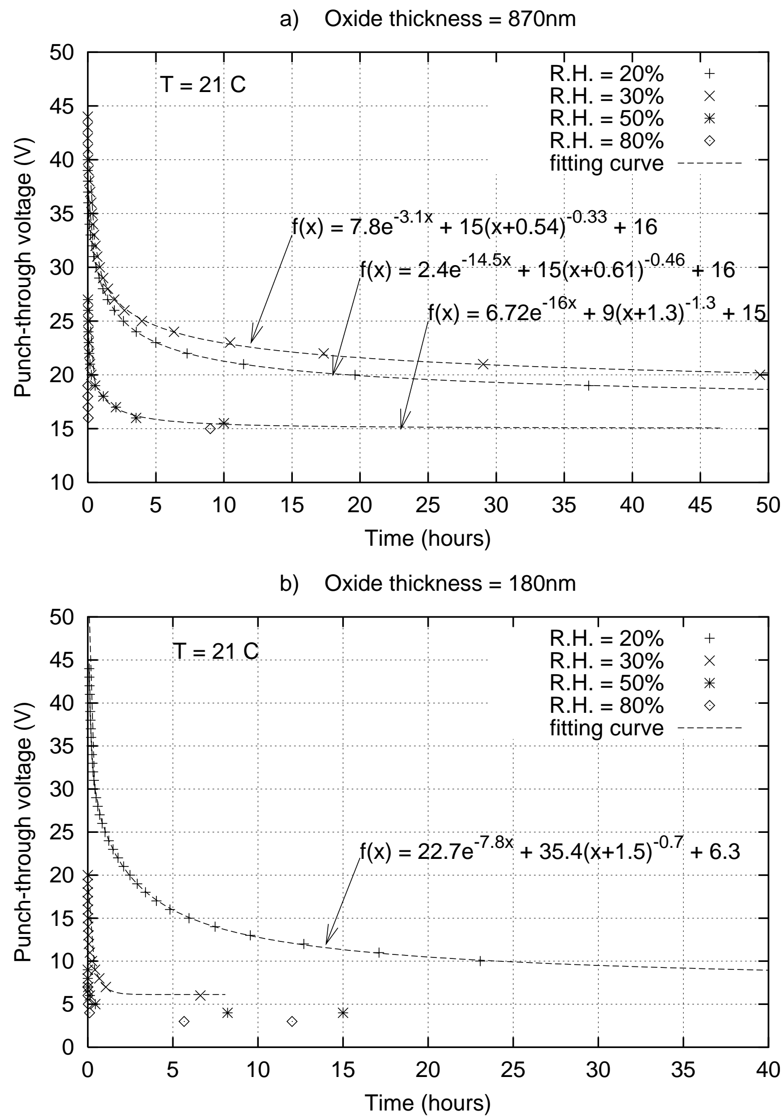

Figure 10: Time dependence of the *punch-through* voltage for devices having an oxide thickness of $870\,nm$ (a), and $180\,nm$ (b).

We performed a set of measurements at different values of relative humidity, on samples with different oxide thickness and fixed oxide charge density. A summary of the measurements is given in figure 10. The *punch-through* voltage is plotted as a function of the elapsed biasing time. The general transient behaviour is characterised by the superposition of two different decays: a fast exponential component and a slow power function. The transient time depends on the environmental conditions: it can be either minutes in a high humidity ambient (R.H. more than 80 %), or days in a low humidity atmosphere (R.H. less than 20 %). Anyway for a given sample the asymptotic limit of V_{pt} is the same. We found that with a thicker oxide the asymptotic limit gets higher. We observed also, that a $1\mu m$-thick polyimide passivation layer deposited on the oxide, has no influence neither on the transient time nor on the final V_{pt}.

The physical reason of this "strange" behaviour of the *punch-through* voltage can be a charge surface migration [2,3]. In particular the humidity acts on the mobility of both ionised contaminants deposited on the outer oxide surface and negative charges coming from the electrical contacts. When bias is applied to the device, a negative charge flow progressively builds up a potential on the surface affecting the electrical properties of the device. Getting back to the plots in figure 10, we note that the V_{pt} value measured just after the voltage ramp-up is quite high and close (anyway always lower) to the simulated value. Then, as the charge migrates along the surface, the *punch-through* voltage decreases reaching the asymptotic value when the potential of the more negative cathode is spread all over the oxide surface. In a thicker oxide, this process is less effective because the potential built up on the oxide surface is more distant from the silicon underneath.

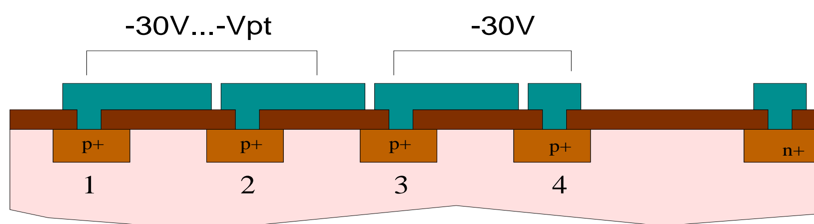

Figure 11: Sketch of the model with enlarged metallisations used for the simulations of the environmental perturbations.

In order to verify this hypothesis we used a simulation model where the metallisation of the more negative cathode is extended up to the other cathode, imitating the final status of the potential built up on the outer oxide surface (figure 11). Figure 12 reports both the simulation results (lines) and some experimental data for different oxide characteristics (dots). The agreement is quite good, supporting the physical explanation

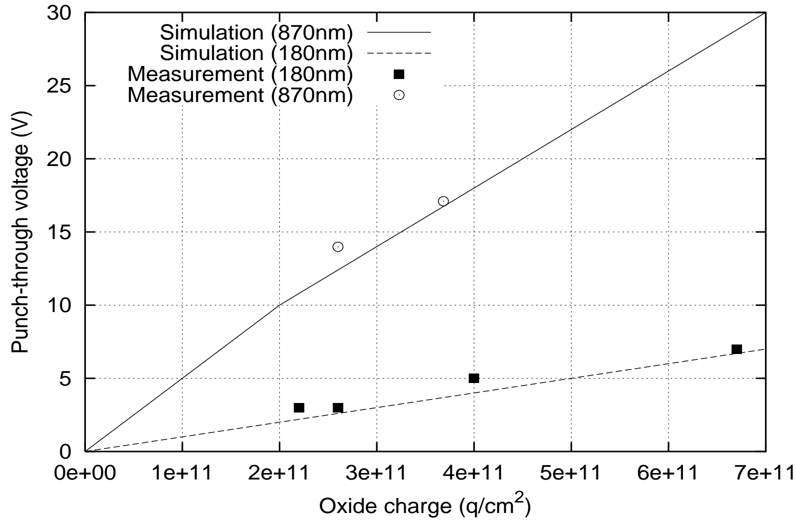

Figure 12: *Punch-through* voltage as a function of the oxide charge density for the structure shown in figure 11.

proposed above. Comparing the plots of figure 6 and 12 one can appreciate the dramatic reduction of the *punch-through* voltage, especially for thin oxides. It is notable that the

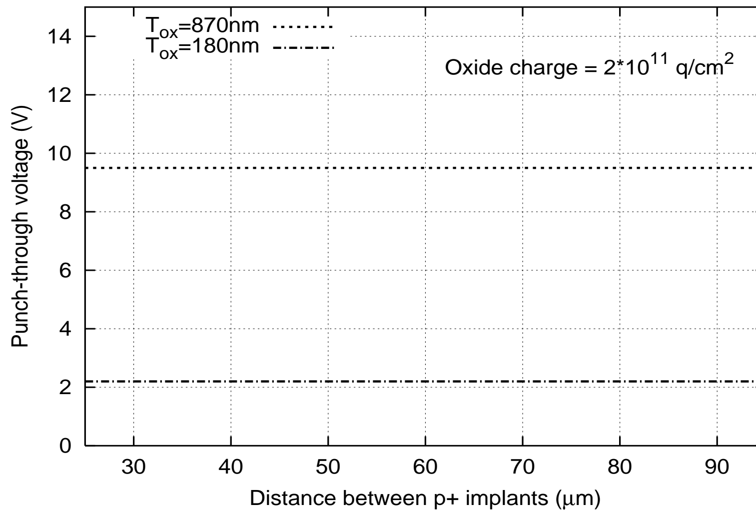

Figure 13: *Punch-through* voltage as a function of the distance between the p^+ implants for the structure shown in figure 11.

distance between the p^+ implants does not play any role on the V_{pt} value in such conditions, as proved by the simulations shown in figure 13.

As far as the experimental data are concerned, we should point out that the asymptotic *punch-through* voltage is affected by the conformation of the cathode metallisation. So far we have considered a structure in which the metal completely covers the under-

neath p^+ implant, as shown in figure 14b. In this case the negative charges produced

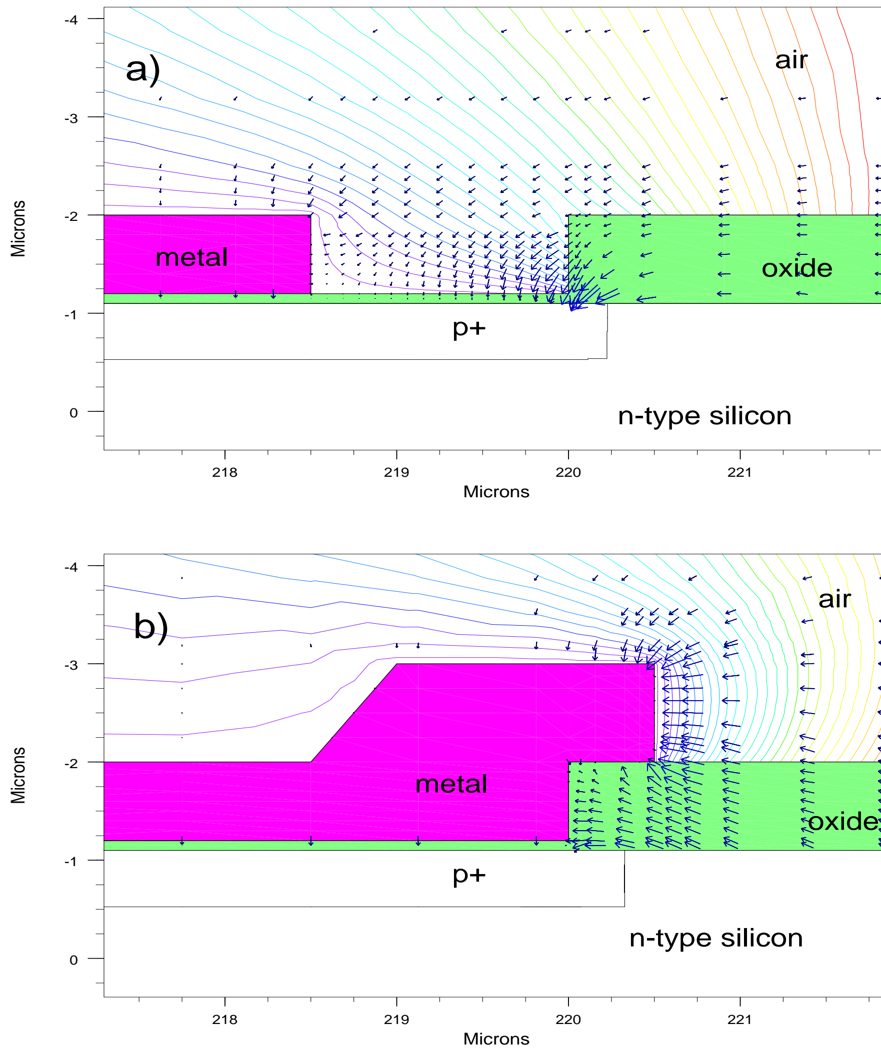

Figure 14: Electric field (vectors) and equipotential lines at the metal edge of the more negative cathode for two different cases: a) implant not completely covered by the metal, b) implant completely covered.

at the border of the metal are subjected to a strong horizontal electric field and they are forced to drift to more positive potentials. This is represented in figure 14b showing both the electric field vectors (the vector length is proportional to the intensity) and the equipotential lines as a result of a simulation. Instead, in the case shown in figure 14a, in which the metal ends before the border of the junction, the electric field has no horizontal component. Thus, the charge migration phenomenon is less pronounced and the asymptotic

value can be higher.

In certain cases it is necessary to maintain high and stable values of the *punch-through* voltage in order to avoid a current flow between the cathodes at the working bias voltage. We have shown that a conventional structure, as the one presented in figure 1, can not provide *punch-through* voltages higher than $15\,V$ for typical oxide charges. To solve this problem we implemented a new design of the cathode metallisation. This is shown in figure 15. We can see that the metal edge of the more positive cathode has been extended

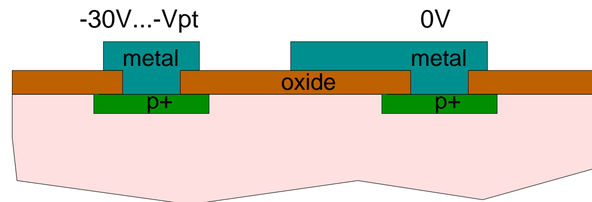

Figure 15: Sketch of the device with an enlarged metallisation of the more positive to higher the *punch-through* voltage.

over the oxide well beyond the metallurgical junction. The purpose of this approach is to protect the covered oxide against the accumulation of negative charges and to build up a “positive” potential in that shielded region. Figure 16 shows the simulated values of the *punch-through* voltage as a function of the length of the metal overhang for two oxide thicknesses and different values of the fixed oxide charge density. It is important to note that the simulations are carried out accounting for the negative charge effect as we have previously presented in figure 11. We can readily appreciate the positive role of the field-plate as its length increases. These results are confirmed by the measurements performed on three devices having a different field-plate length. Comparing figure 16 and figure 17 we note that the asymptotic value of the *punch-through* voltage is in a perfect agreement with the simulations.

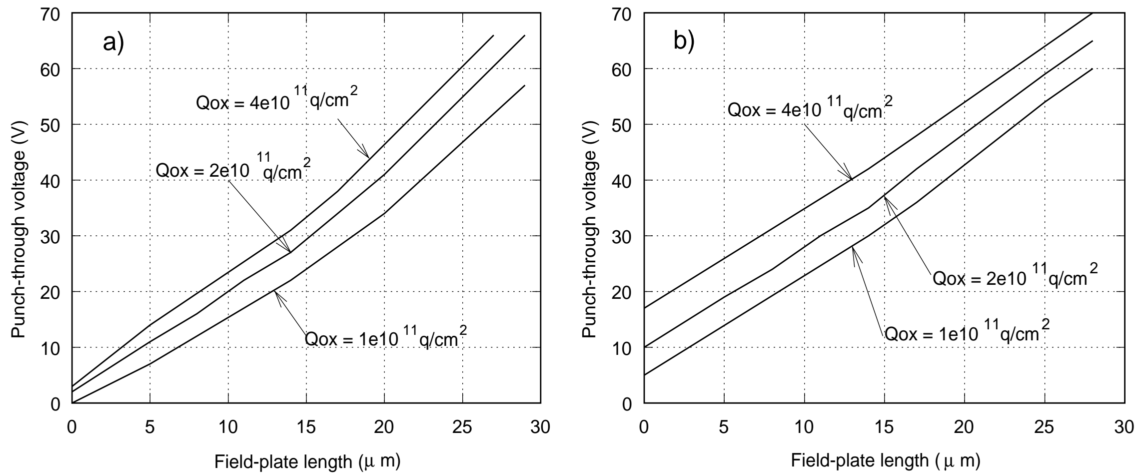

Figure 16: *Punch-through* voltage as a function of the "positive" field-plate length: a) $180nm$-thick oxide and b) $870nm$-thick oxide.

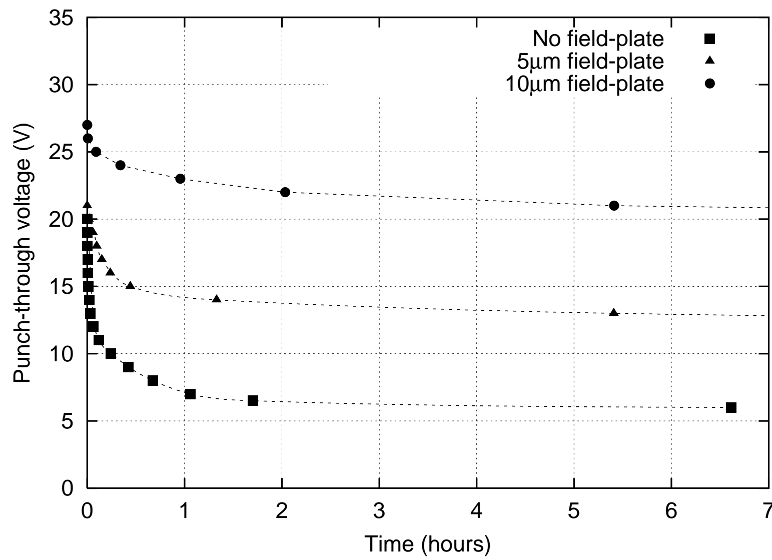

Figure 17: Measurement of the *punch-through* voltage for three structures having a field-plate length, respectively, of 0, 5 and $10\mu m$. The oxide thickness is $180\,nm$, while the oxide charge density is $2 \times 10^{11}\,q/cm^2$.

3 Practical example: the Silicon Drift Detector

The results of the above discussion can be applied fruitfully to the case of the Silicon Drift Detector (SDD). As a practical example, let's consider the SDD to be employed in the ITS of the ALICE experiment at LHC [4]. A detailed description of this detector can be found in [5]. As most of the linear SDDs, the ALICE detector presents on both sides a series of parallel p^+ implant drift cathodes (figure 18) that serve to fully deplete the volume and to provide a constant electrostatic field parallel to the wafer surface. At the flanks

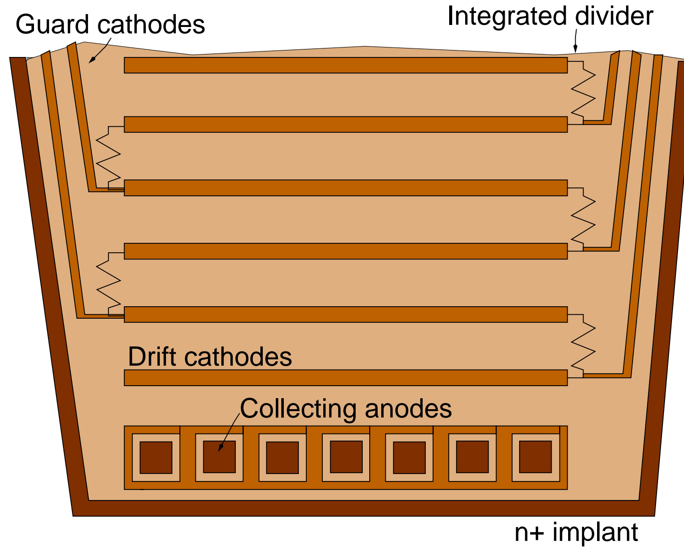

Figure 18: Schematic view of the ALICE Silicon Drift Detector.

there are two triangular areas constituted by the guard p^+ cathodes. There is one guard cathode every two drift cathodes, so the potential difference between adjacent guards is twice that between adjacent drift cathodes. The drift cathodes have a $70\mu m$-wide implant and a pitch of $120\mu m$. Since it is desirable to maintain a high sensitive-to-total-area ratio, the geometry of the guard zone is very tight: the $12\mu m$-wide p^+ implants are located with a pitch of $32\mu m$. Both the drift and guard cathodes are biased through an integrated voltage divider. The detector is planned to work at a potential difference of about $8\,V$ between adjacent drift cathodes, thus, $16V$ between adjacent guard cathodes. It is clear that the guard zone can be affected by the *punch-through* phenomenon if one does not foresee dedicated solutions in the detector design. An eventual *punch-through* acts as a parasitic resistor inserted in parallel to the implanted resistor of the divider, altering, thus, the linear potential distribution on the cathodes. As an example, figure 19 presents a detector in which, at a bias voltage of $1200V$ (about $4\,V$ between neighbouring drift cathodes), a *punch-through* current starts to flow across the guard cathodes.

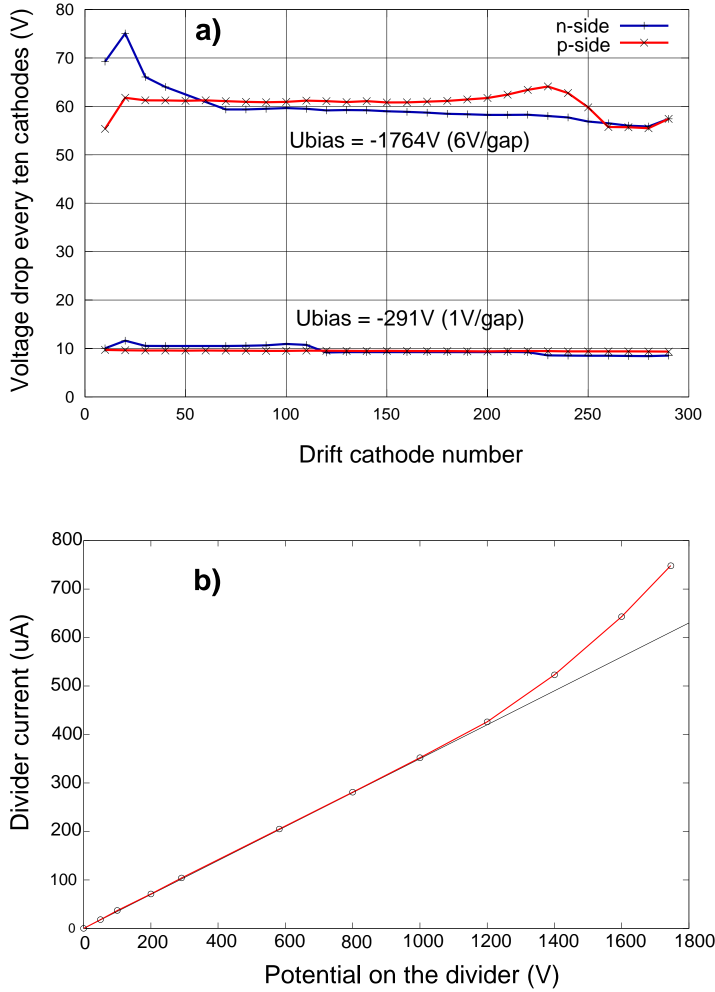

Figure 19: Voltage distribution on the divider (a) and divider current (b) of a detector that at a certain bias voltage starts to be affected by the *punch-through* phenomenon.

The guard cathodes of the detector used in the example have a field-plate of $3\,\mu m$ on both edges of the implant. The measured value of the *punch-through* voltage is in agreement with the results of the simulation performed for that geometry.

Following the conclusions drawn in the previous section, the final design of the ALICE detector presents an enlarged "positive" field-plate for both the guard and the drift cathodes. Since the guard pitch is only $32\,\mu m$ it was not possible to realize a "positive" field-plate wider than $9\,\mu m$. This width ensures a full functionality of the device under the working conditions ($16\,V$ between consecutive guards), though it does not provide a large safety margin for low values of oxide charge. Indeed, according to the simulations performed for an oxide having a thickness of $180nm$ and a positive fixed charge of $2 \times 10^{11} q/cm^2$ the *punch-through* voltage is $18\,V$. Figure 20 shows the potential distribution on the divider and the divider current up to a bias voltage of $2328\,V$ for a detector with the

enlarged field-plate. No *punch-through* occurs for a potential difference between guard

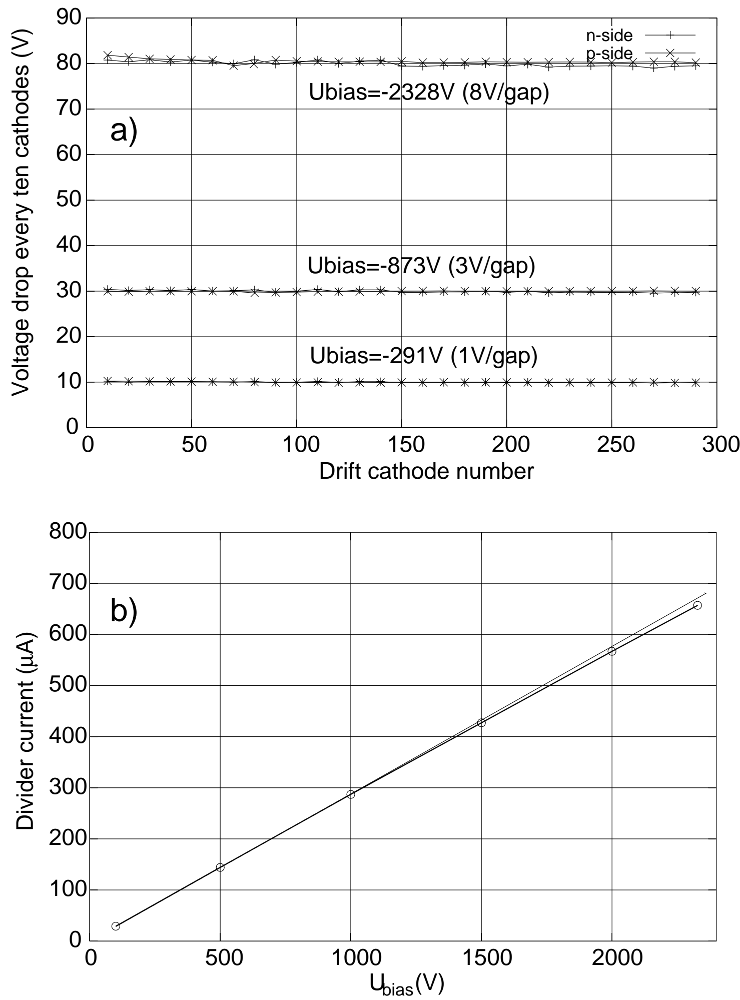

Figure 20: Voltage distribution on the divider (a) and divider current (b) of a *punch-through*-free detector.

cathodes of $16\,V$. Indeed, the potential distribution is perfectly linear. It is interesting to note that the divider current slightly deviates downwards from the linear fit, since the power dissipated in the integrated divider causes a mobility reduction.

4 Acknowledgements

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