

THE ARGO LEVEL-I DAQ SYSTEM

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Abstract

The ARGO-YBJ experiment has been designed in order to study the cosmic rays, mainly cosmic gamma-radiation, at an energy threshold of ~ 100 GeV, by means of the detection of small size air showers. This goal will be achieved by operating a full coverage array detector in the Yangbajing Laboratory (Tibet, China) at 4300 m a. s. l.

1. INTRODUCTION

The ARGO-YBJ experiment [1-2] will investigate a wide range of fundamental issues in Cosmic Rays and Astroparticle Physics, including gamma-ray astronomy and gamma-ray bursts physics in the range 100 GeV – 500 TeV.

The detector (Fig. 1) consists of a single layer of RPCs (Resistive Plate Counters) covering an area of $\sim 6500 \text{ m}^2$ and providing a detailed space-time picture of the shower front. The building block of the detector is a 12-chambers module called cluster (the rectangles shaded in figure 1).

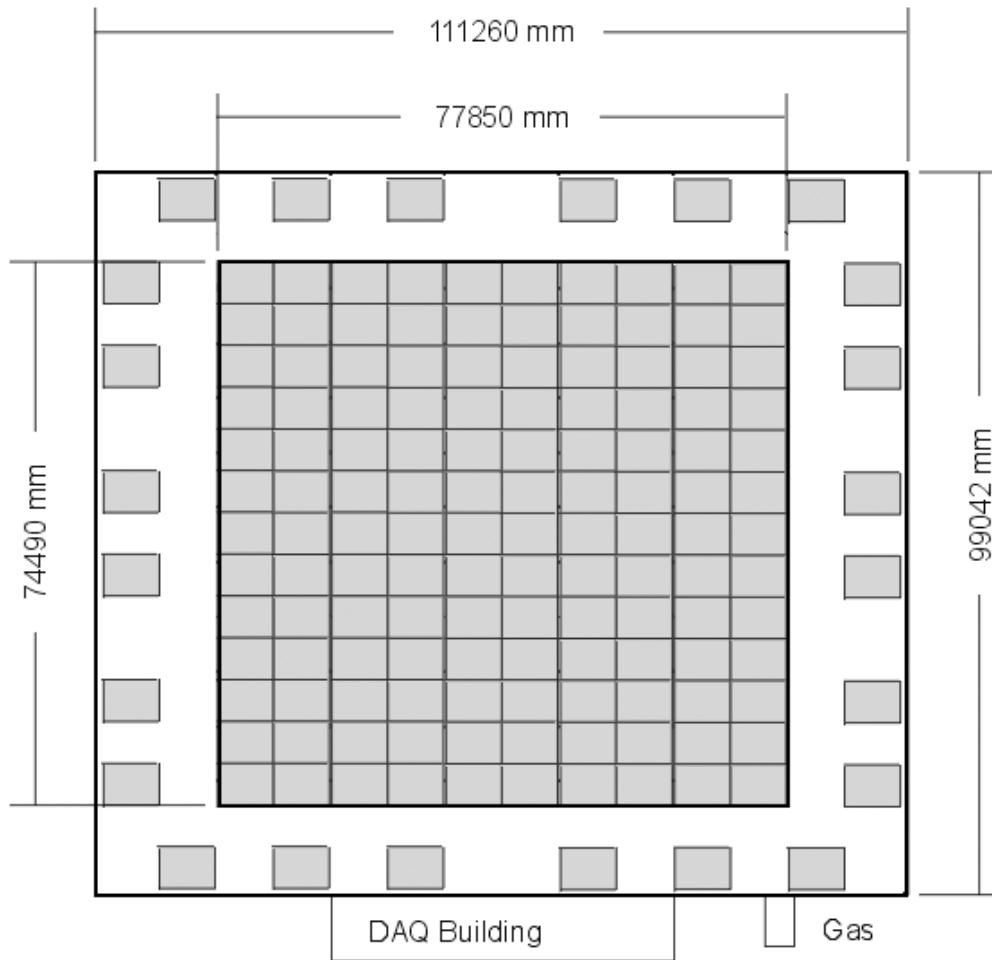


Fig. 1: ARGO detector layout.

As shown, the detector consists of 130 clusters in the inner part and 24 clusters in the guard ring for a total of 1740 RPCs. The proposed layout covers an active area of about 95 % .

The ARGO DAQ architecture is structured in five layers: Front End Electronics (FEE), Cluster Logic (CL), Level-I Readout (RO-I), Level-II Readout (RO-II), Farm and Event Builder (EB). The Front End Electronics (FEE) is placed directly onto the detector and is built around a custom chip designed to amplify and shape the RPC's strip signals. The FEE drives the Cluster Logic (CL) located seven meters away.

The CL boards [3] manage multi-channel and multi-hit TDC custom chips [4-5] to extract timing information of the hits, acquire strips coordinates, generate high and low level multiplicity and build data frames. Each CL serves four groups of three chambers and consists of four Signal Processing Cards plus one Control and Communication Card. Data from the clusters is transmitted to Level-I which is located at the center of the detector.

In the RO-I environment the Argo Memory Board (AMB) collects data from the clusters, controlling data integrity and also formatting data according to their event number. Custom controllers [6-7] implement reading the AMBs via an application specific backplane [8-9].

At the upper level (RO-II) data is formatted according to the event number and sent to the Farm to perform the final event building and mass storage. The trigger supervisor enables the trigger generation and distribution.

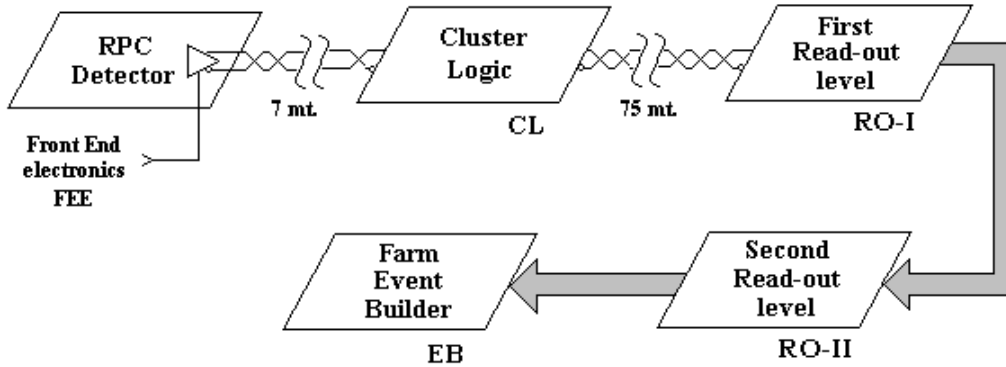


Fig. 2: ARGO DAQ Architecture.

2. SYSTEM ARCHITECTURE

The ARGO DAQ system deploys the event-driven architecture already developed for the KLOE detector, extending its modularity to fulfill the requirements of the detector.

For each trigger an incrementing trigger number word is produced by each CL controller and inserted in the frame to be transmitted to the RO-I electronics. In the RO-I environment each AMB collects data from 4 clusters and it is interfaced to the ROCK Readout controller [7] via a high speed proprietary bus, the AUXBUS [8-9].

The AMB boards are housed into VME crates (Fig. 3) equipped with the VME bus and the AUXBUS.

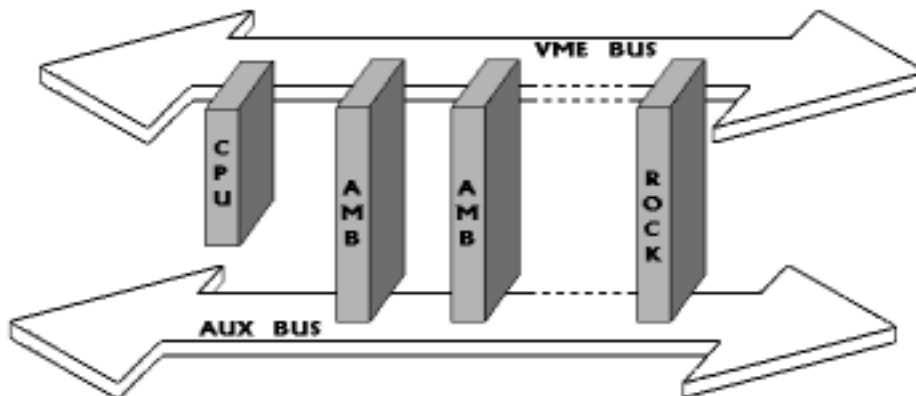


Fig. 3: RO-I crate layout.

Up to 8 RO-I crates can be equipped in this way and chained via a parallel bus (CBUS) to the Level-II read-out.

The CBUS is mastered by the ROCK Manager [10] which gathers data from the ROCKs installed in the chain. A VME CPU in the RO-II crate initializes the whole chain using a VIC interconnection, runs diagnostic tests and samples events from time to time in order to monitor the read-out performances. The CPU is also in charge of moving the acquired data from the ROCK Manager internal memory to the Farm and Event builder.

A block diagram of the Level-II crate layout is depicted in Fig. 4

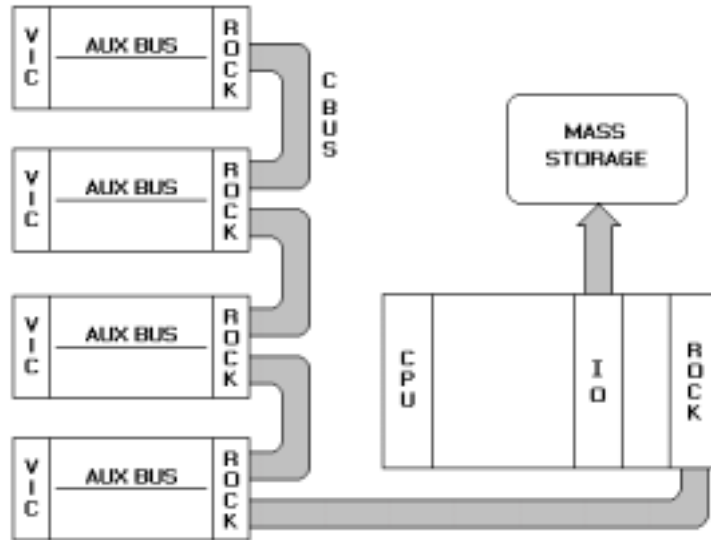


Fig. 4: Chain and RO-II crate layout:

Data from a cluster of crates is collected by the ROCKM (ROCK Manager module) through the CBUS. The ROCKM controller finally transmits data to the Farm Event Builder (EB) and then to a mass storage medium, via high speed standard data concentrators.

3. THE ARGO MEMORY BOARD

When a trigger is issued the CL electronics will transmit data at a peak data rate of 20 Mbytes. Each AMB module acts as a frequency buffer between CL electronics and the RO-I incorporating a FIFO memory bank.

Each AMB (Fig. 5) serves four clusters.

Onto each input channel data will be first pre-processed. If data are found to be consistent than a bit indicating that no failure has been found is set.

At the output of the FIFO two post-processors will add two bits to the FIFO outputs thus allowing the DAQ to distinguish between the four input channels.

The VME controls the functionality of the board by injecting a test pattern at the input of the FIFO and performing a consistency check at the output. Furthermore the CPU has the task of initializing the AMB board setting the control bits for debugging purposes.

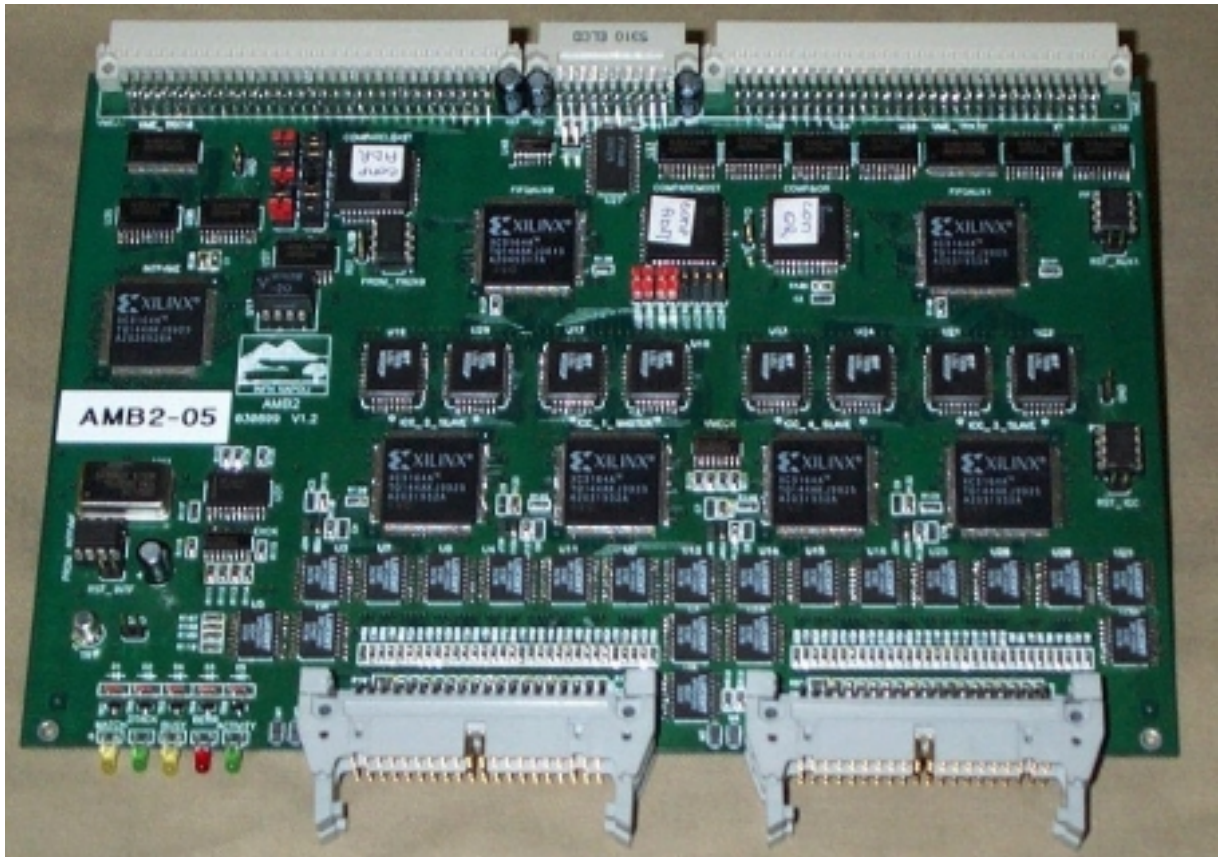


Fig. 5: AMB module.

4. THE TRIGGER SUPERVISOR

The Trigger Supervisor of the ARGO experiment dispatches trigger pulses to all the controllers, handles BUSY conditions, sets and monitors dead-time, manages the Sync Cycles, detects DAQ faults, generates “soft” triggers for debugging and masks trigger pulses for a specific DAQ unit (partitioning). A block diagram of the trigger distribution network is shown in Fig. 6

The Trigger Supervisor (TS) interacts with the ROCK and the ROCK Manager board via 5 NIM signals: Trig, Busy, Halt, SyncR, SyncF.

The Trig signal is produced in the trigger box and is an input to the Trigger Supervisor which transfers it to all the DAQ components with a star-like network.

Each ROCK in the RO-I crate and the ROCKM in the RO-II environment may generate a Busy or Halt flag to control the data trigger flow. Busy is asserted when the ROCK event queue goes full or when one of the AMB FIFO buffer exceeds the half full threshold. All the Busy flags are handled by the TS which suspends the trigger production meanwhile a Busy condition is detected.

The HALT flag is asserted in case of event number mismatch between the ROCK and CL internal event counters or a protocol error onto the CBUS chain link.

The TS uses the SYNCR lines in order to start an event number consistency check in all the DAQ controllers. Each unit asserts the SYNC Failure (SYNCF) flag in case of discrepancies.

The generation of trigger is inhibited during either a SYNC cycle and also when a SYNC Failure condition is detected.

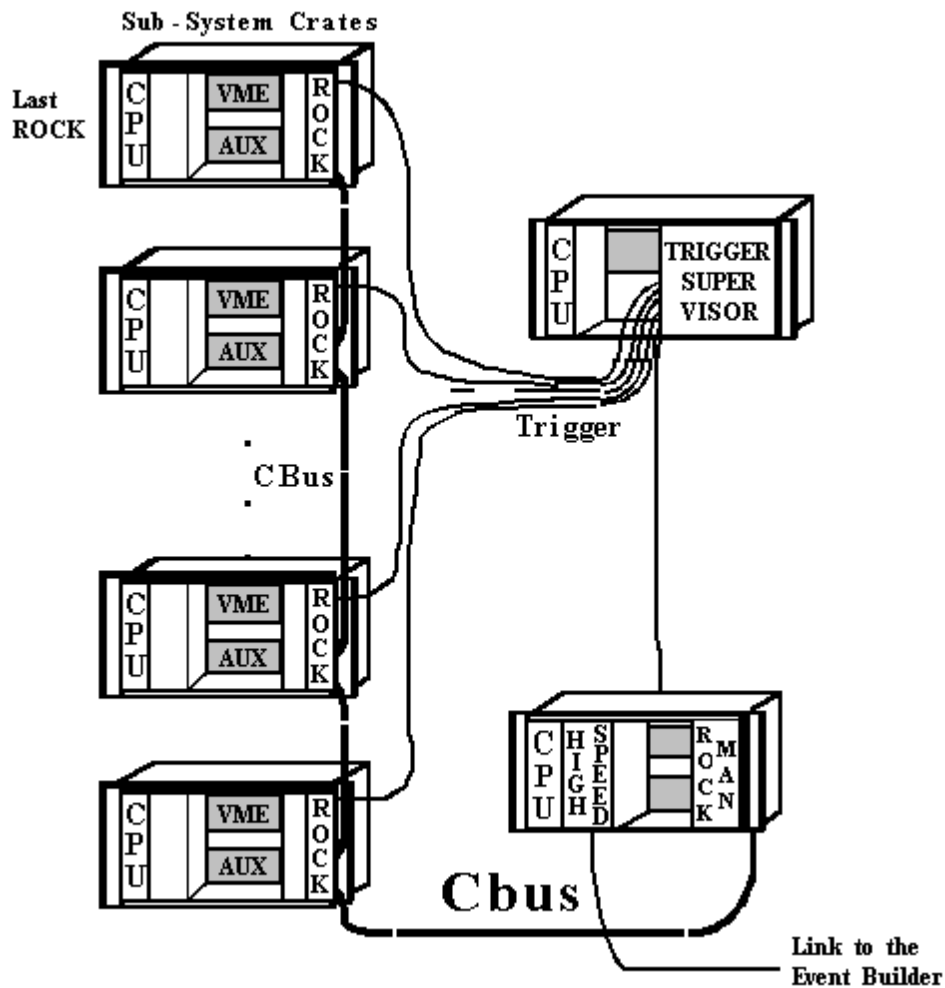


Fig. 6: Trigger Distribution Network:

Conclusions

All of the modules described in this note have been already implemented and fully tested. A test station is presently taking data using the outlined architecture.

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