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The AGILE Silicon Tracker: architectural design and prototype testbeam results

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Abstract

AGILE (Light Imager for Gamma-ray Astrophysics) is a small scientific satellite for the detection of cosmic γ-ray sources in the energy range 30 MeV-50 GeV with a very large field of view (1/4 of the sky). It is planned to be operational in the years 2003-2006, a period in which no other γ-ray mission in the same energy range is foreseen.

The AGILE scientific instrument is made of a silicon-tungsten Tracker, a CsI(Tl) Minicalorimeter, an Anticoincidence system and a X-ray imaging detector sensitive in the 10-40 keV range.

We present here a detailed description of the architectural design of the Silicon Tracker with its trigger and readout logic, and the performance of the detector prototype during a testbeam period at the CERN PS in May 2000. The Tracker performance is described in terms of position resolution and signal to noise ratio for on-axis and off-axis incident charged particles. The measured 40 μm resolution for a large range of incident angles will provide an excellent angular resolution for cosmic γ-ray imaging.

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1 Introduction

Cosmic gamma rays are a manifestation of the most energetic phenomena in our Universe. Among the γ-ray emitting sources, we can list relativistic compact stars, massive black holes in active galactic nuclei, γ-ray burst sources and the Sun during intense flares. Gamma rays reach the Earth also from remote regions of the Universe providing fundamental information on the cosmological evolution of energetic sources. Many γ-ray sources are transients on timescales ranging between seconds and several days, showing a Universe in turmoil and subject to catastrophic events. The understanding of these phenomena is still preliminary and a tremendous amount of work both from the experimental and the theoretical point of view is necessary to understand all the details.
ASI (Agenzia Spaziale Italiana - Italian Space Agency) has promoted in 1997 a new program of small scientific missions.
In December 1998 AGILE (Astrorivelatore Gamma a Immagini LEggero - Light Imager for Gamma-ray Astrophysics) was selected as the first small mission among 8 proposals that ASI supported for the phase A study.
At the moment AGILE is entering the phase C/D, which is the construction and assembly phase of the satellite.
The AGILE mission will provide a powerful Observatory for γ-ray astrophysics in the energy range 30 MeV-50 GeV, during the years 2003-2006. No other γ-ray mission in this energy range is planned in the same period.
The instrument is light ($\approx$80 kg) and effective in detecting and monitoring γ-ray sources within a large field of view ($\approx$1/4 of the whole sky). The instrument consists of a silicon-tungsten Tracker, a 1.5 X_0 deep CsI Minicalorimeter, an Anticoincidence system made of segmented plastic scintillators, a X-ray detector in the range 10-40 keV with a coded mask system, fast readout electronics and processing units.
The AGILE team currently includes scientists from CNR and INFN laboratories and the Universities of Trieste, Roma La Sapienza and Roma Tor Vergata.
The working principle of AGILE is shown in fig. 1: the photon converts in an electron-positron pair in the Tracker tungsten layers, which is detected by the silicon strips. The CsI(Tl) Minicalorimeter measures the energy released by the electron and the positron while the Anticoincidence AC is used to reject charged particles.
Fig. 2 is a 3D sketch of the instrument; the overall dimension is $61\times61\times58$ cm^3.
For a detailed description of the scientific performances of AGILE, see (1).

In the following, we present the architectural design of the Silicon Tracker (section 2) and the testbeam results we have obtained with the final silicon prototypes (section 3).

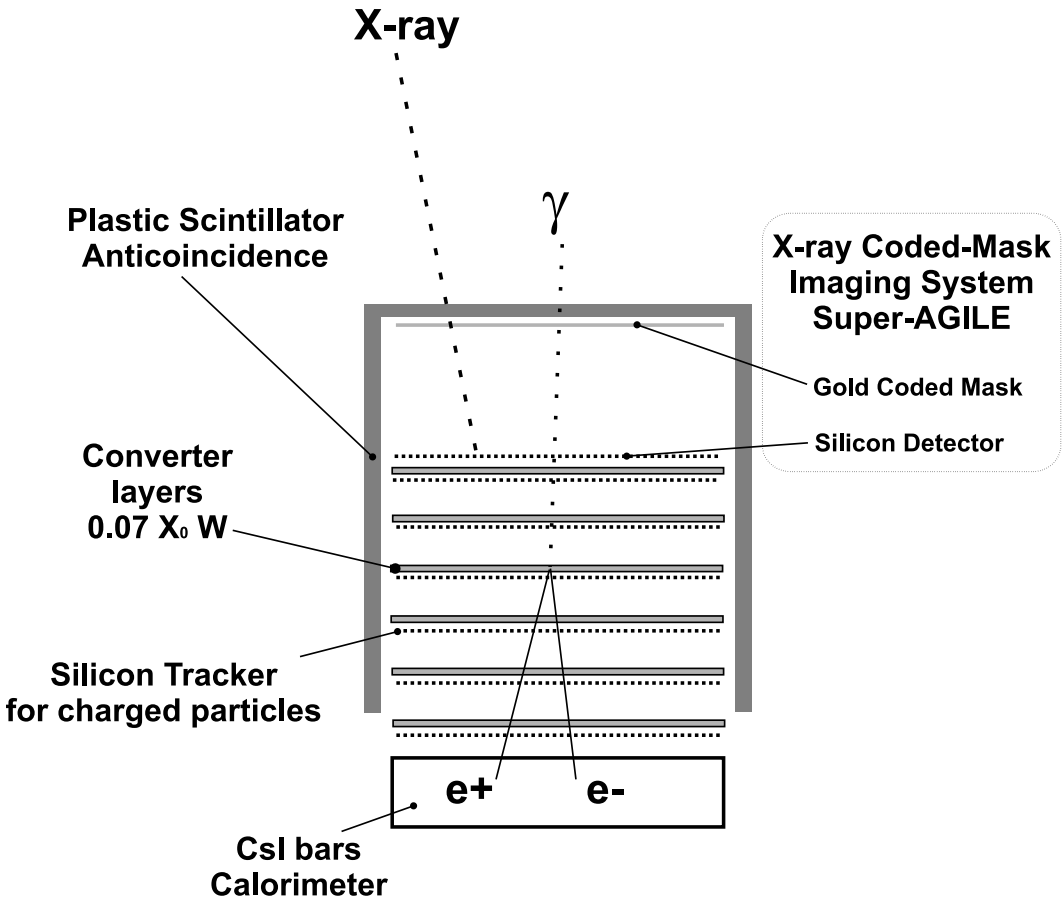

Figure 1: Working principle of the AGILE instrument.

2 The AGILE Silicon Tracker

The Silicon Tracker is the heart of the AGILE mission. It has a twofold purpose:

- to provide the trigger to the whole instrument when a γ-ray has converted inside the Tracker itself
- to provide a complete representation of the event topology, allowing the reconstruction of the momentum and direction of the electron-positron pair produced by the photon conversion and thus the incoming direction of the γ-ray itself.

Together with the Minicalorimeter, the Tracker constitutes the AGILE Gamma Ray Imaging Detector (GRID).

The AGILE Tracker is made of 14 planes of silicon strip detectors. Each plane is configured as follows:

- active part: two views of 16 silicon pads each, whose features are described in the

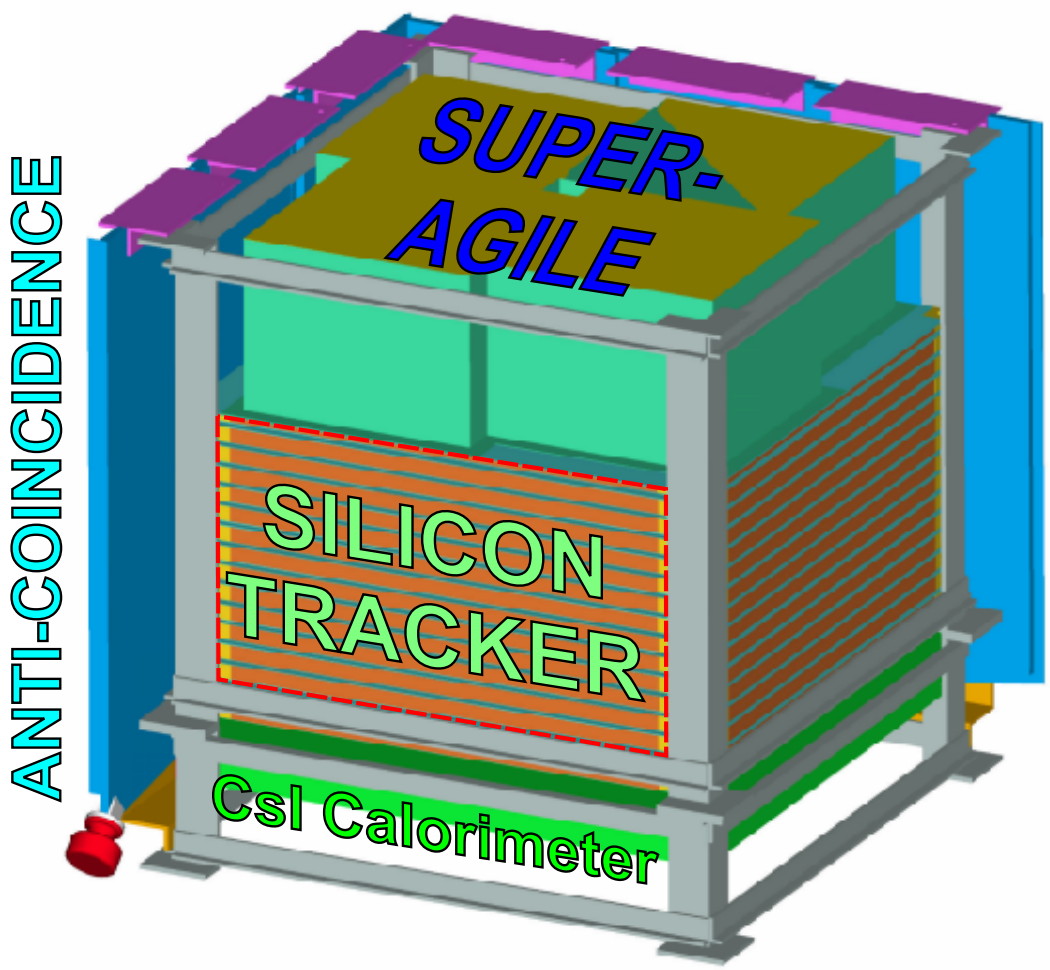

Figure 2: 3D sketch of the AGILE instrument without the top and two of the lateral sides of the anticoincidence; the overall dimension is $61 \times 61 \times 58$ cm^3.

next subsection; the strip orientation of the first view is perpendicular to the one of the second view resulting in a *x*-*y* detector.

- passive converter: one tungsten layer 245 μm thick (corresponding to 0.07 radiation lengths) positioned above the silicon layer; the last 2 planes do not have this converter layer due to the trigger configuration

Fig. 3 shows the structure of the 14 silicon planes. They are organized in trays, each of them containing 2 silicon views, with the exception of the first and last tray. Starting from the top of the plane, the structure consists of:

- a 410 μm silicon detector view glued on a 100 μm kapton layer (except the first tray);
- a 500 μm thick carbon fibre layer;

- a 12 mm thick layer of aluminum honeycomb;
- a 500 μm thick carbon fibre layer;
- a 245 μm thick tungsten layer (except the trays from 12 to 15);
- a 410 μm silicon detector view glued on a 100 μm kapton layer (except the last tray);

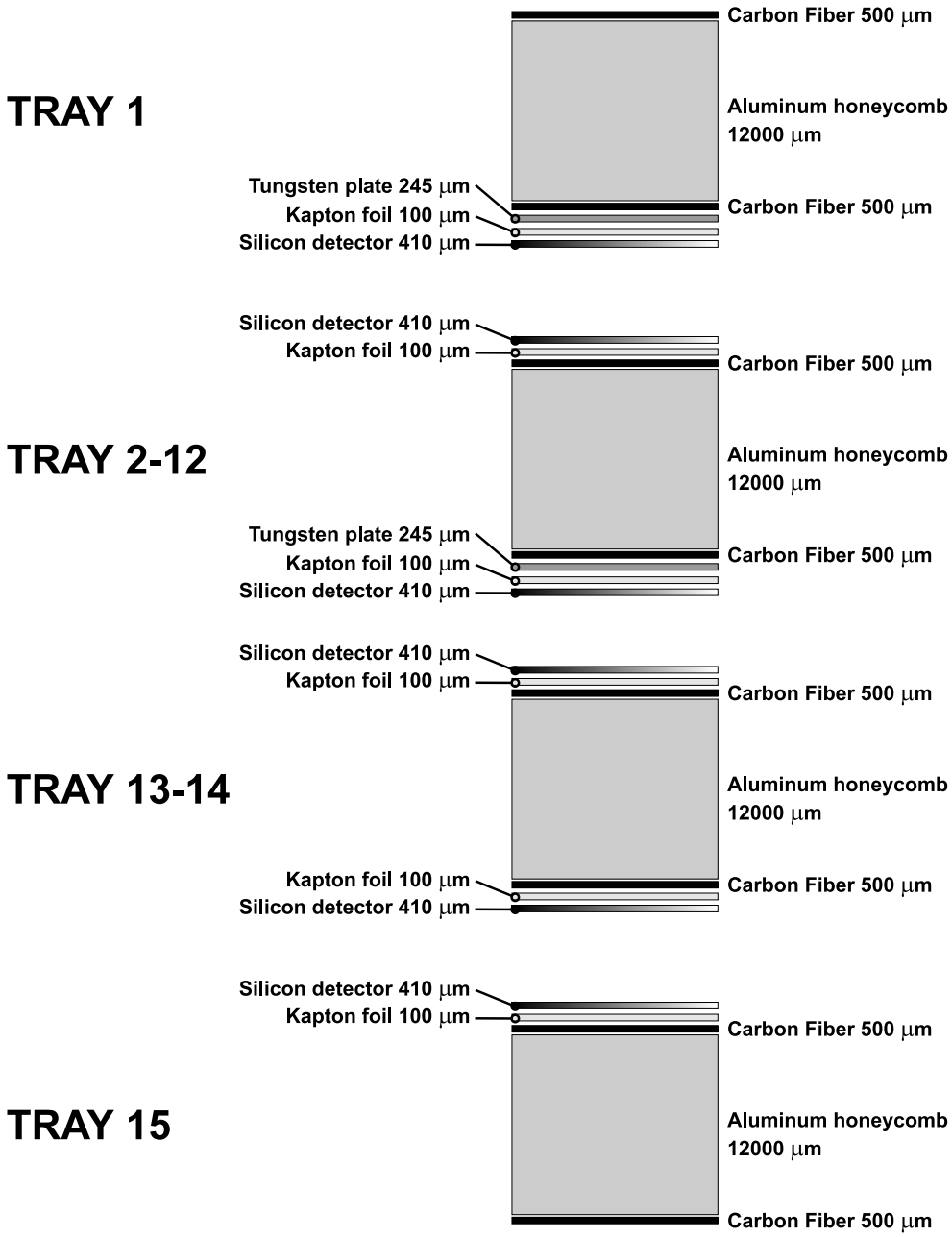

Figure 3: Silicon Tracker trays configuration (not to scale).

Four silicon detectors are bonded together to create a “ladder”. Each view is thus made of four ladders. Fig. 4 shows a sketch of the Silicon Tracker tray with all its components.

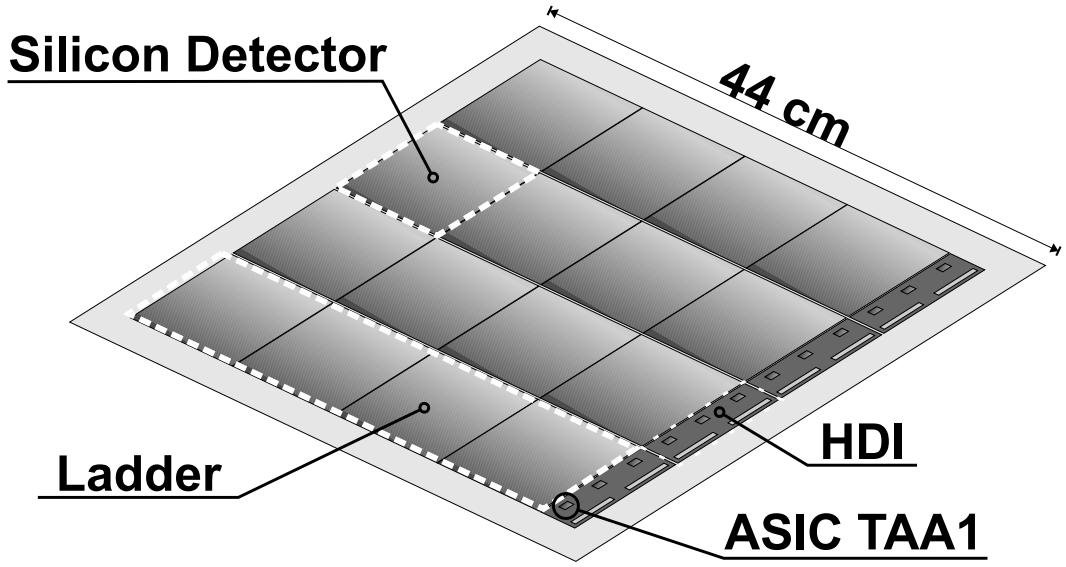

Figure 4: Silicon Tracker tray sketch.

As far as the electronics is concerned, the 28 views are divided into 14 logic blocks (FrontEnd Block, FEB) of 2 views each (2 *x* or 2 *y* views).
The Tracker FrontEnd Electronics (FEE) is made of 2 Frontend and Trigger Boards (FTBs) (1 for the *x* and 1 for the *y* views) positioned on 2 of the 4 lateral sides of the Tracker itself.

2.1 Silicon Detectors

The silicon detectors are single-side AC-coupled strip detectors, built on high resistivity ($\geq$4 kΩ·cm) 6” substrate by HAMAMATSU PK. Their size is 9.5$\times$9.5 cm^2 while their thickness is 410 μm. The biasing of the detector is achieved through polysilicon resistors. The detector is used with a “floating strip” configuration (2); the physical strip pitch is 121 μm and the readout one is 242 μm.
This configuration has been chosen in order to have an excellent spatial resolution while keeping under control the number of readout channels and hence the detector power consumption.

The prototype production consists of 10 detectors with the following electrical characteristics:

- bias resistor value: 40 MΩ
- coupling capacitance value (measured at 10 kHz): 527 pF

- AC coupling Al resistance value: 4.5 Ω/cm
- leakage current density at a biasing voltage 20% higher than the depletion one (V_{FD}=75 V): 1.5 nA/cm^2

Fig. 5 shows one of the AGILE silicon detectors, while fig. 6 is a picture of the ladder built for the AGILE May 2000 testbeam at the CERN PS area.

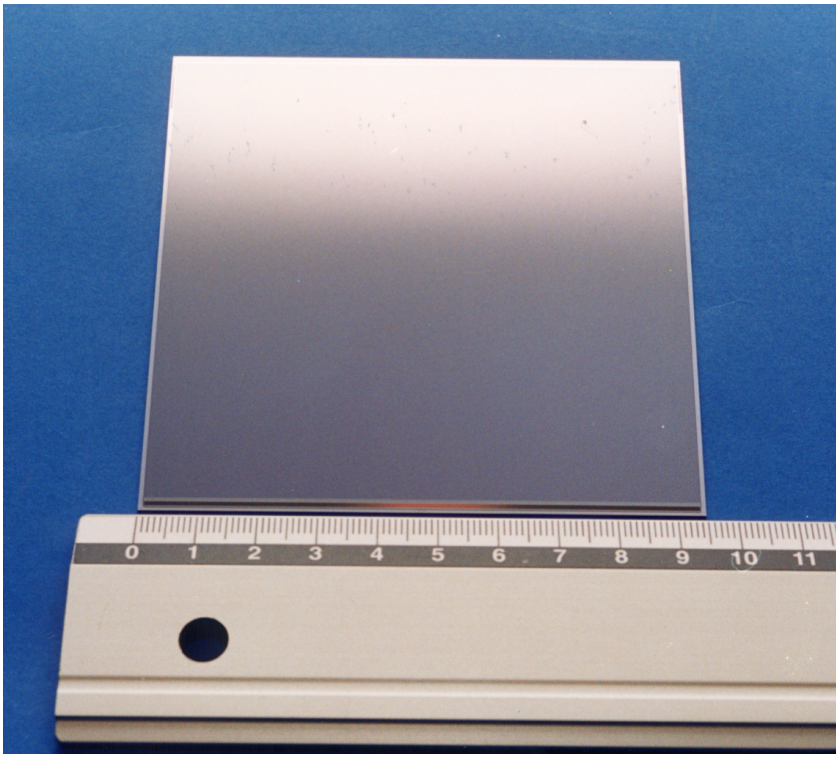

Figure 5: The HAMAMATSU final prototype for the AGILE silicon detector

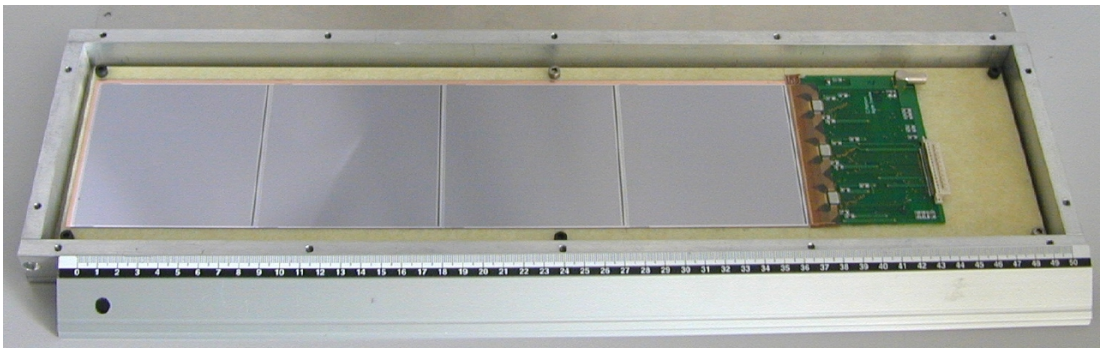

Figure 6: Prototype ladder tested during the May 2000 testbeam at the CERN PS area.

2.2 Frontend Electronics

The Tracker Frontend Electronics consists of:

- 2 Frontend and Trigger Boards (FTBs), one per each view type
- a hybrid (HDI, High Density Interconnection) per ladder for a total of 56 HDIs per FTB
- 3 frontend ASICs (TAA1) per HDI for a total of 168 TAA1s per FTB

The total number of the Tracker readout channels is 43008.
The logic unit of the FTB is the FEB, for a total of 7 FEBs per FTB.
In the following, we describe the main characteristics of each component.

2.2.1 The TAA1 ASIC

The TAA1 ASIC is a 128 channel, low noise, low power, self triggering ASIC designed by IDE AS [1] and produced by AMS [2] with 0.8 μm N-well BiCMOS, double poly, double metal on epitaxial layer technology.
The TAA1 is the evolution of the TA1 ASIC and it has been designed on purpose for the AGILE project.
The version we have used in the testbeam is the TA1, made on 1.2 μm technology.

Each channel is made of a folded cascode charge sensitive preamplifier, a CR-RC shaper, a sample & hold circuit, a level sensitive discriminator (see fig. 7). The discriminator input is the shaper output filtered by a high pass filter with a very low cutoff frequency (set internally) to eliminate the fluctuations in the DC working point of the preamplifier+shaper folded cascode topology.

The discriminator threshold has to be set from outside the ASIC and it is unique for the 128 channels. In the TAA1 ASIC, a 3-bit trimming DAC per channel is implemented in order to guarantee a threshold uniformity better than 10%. A trigger signal is produced by the discriminator each time the shaper output is above threshold. The trigger output of the ASIC is the OR of the trigger signals of the 128 channels. In the TAA1 version, the trigger output width can be chosen in the range from 0.5 to 4 μs, while in the TA1 this width is given by the time the signal is above the threshold.
Noisy channels can be disabled by loading a bit-pattern in a shift register ("trigger mask").

Once the trigger has been received, the logic has to generate a hold signal which samples the signal pulse height at the shaper output. The time distance between the trigger and the hold is a function of the peaking time of the signal itself and of the threshold setting.

[1] IDE AS, Oslo, Norway
[2] Austria Mikro Systeme International AG, Austria

The readout is a multiplexed analog readout. The maximum readout clock frequency is 10 MHz. We plan to use the ASIC with a 5 MHz clock.

The TA1 ASIC has a calibration feature. Applying a voltage step to a capacitor which is in parallel with the calibration input, it is possible to check the behaviour of the ASIC itself in terms of gain and noise. When using the test mode, an additional noise has to be taken into account due to the series resistance and additional loading capacitance to the channel. The calibration signal can be injected into one channel in a given ASIC at a time, selecting the channel via a 128-bit shift register. We plan to use this facility during the ladder tests and the Assembly, Integration and Verification phase (AIV), while this type of calibration is not foreseen during the satellite flight. In the TAA1 version, a calibration capacitor of 0.5 pF per channel is integrated in the ASIC itself.

To limit the power consumption of the Tracker, we have decided to operate the ASIC in a very low power configuration. Tab. 1 shows the main features of the TA1 ASIC, while tab. 2 shows the power consumption when the nominal values for the input bias currents are used and the one corresponding to the chosen values. Fig. 8 plots the output signal shapes corresponding to the nominal parameter settings (curve a) and to the chosen ones (curve b).

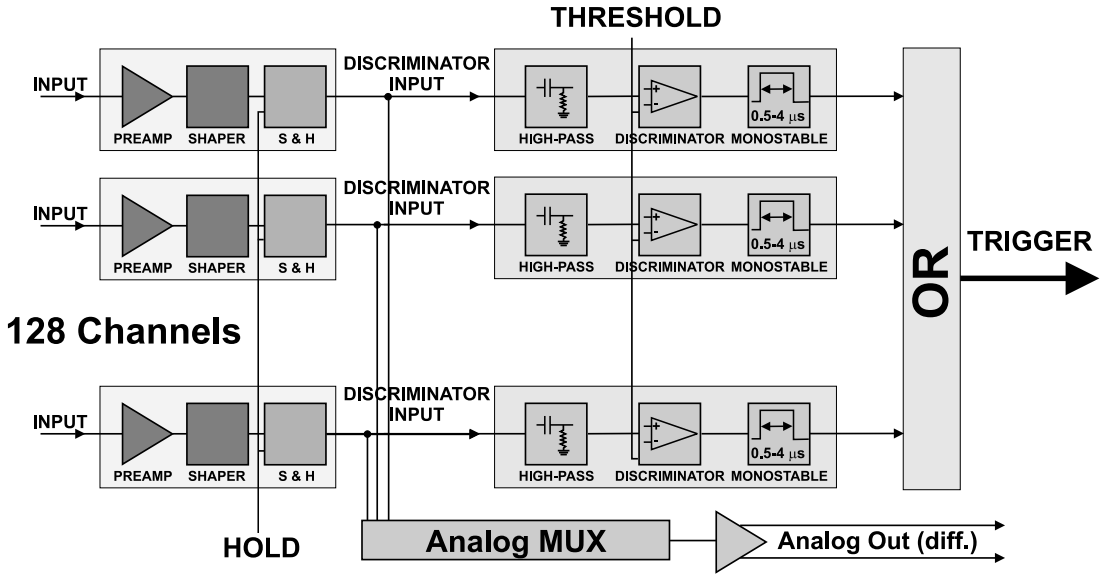

Figure 7: Schematic view of the TAA1 ASIC.

2.2.2 The HDI

The Tracker HDI with the frontend ASICs is positioned on the tray to avoid the presence of delicate cables and boards such as upilex fanouts and the HDIs themselves on the lateral walls of the structure.

To adapt the detector pitch (242 μm) and the TAA1 input pad pitch (100 μm, keeping in

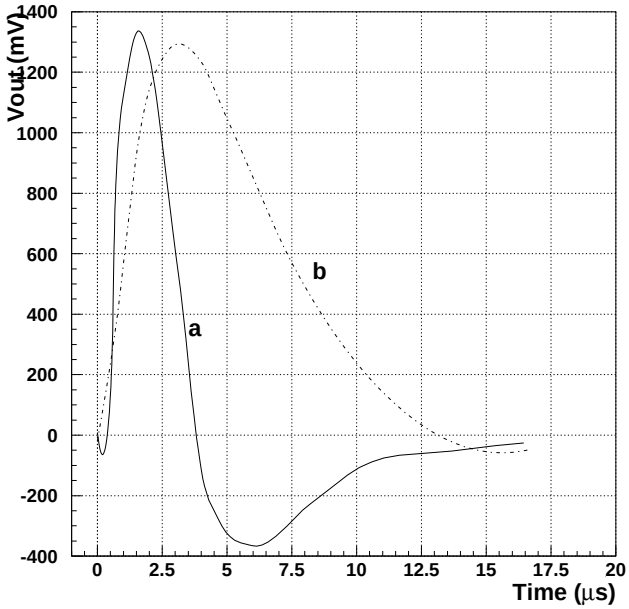

Figure 8: Output signal shape corresponding to the nominal parameter settings (curve a) and to the AGILE ones (curve b). The signals have been measured with the VA-TA DAQ board (IDE AS).

Dimension (mm^2)	4.85×6.9
Thickness (μm)	≈600
Channels	128
Gain (mV/fC)	25
Noise (e^- rms)	165+6.1/pF for T_p=2 μs
Peaking time (μs)	1-3
Nominal power consumption (mW/channel)	1.3
Range (fC)	±18
Input pad size	50 μm×90 μm
Input pad pitch	100 μm
Control pad size	90 μm×90 μm
Control pad pitch	140 μm
Power rails	Vdd=+2 V, Vss=-2 V (separate for digital and analog sections)
Back contact	connect to analog Vss

Table 1: Main features of the TA1 ASIC.

mind that the TAA1 input pads are positioned on three sides of the TAA1 itself), we have decided to use the HDI itself.

	IVss (mA)	IVdd (mA)	Power consumption (mW/channel)
Nominal parameters	70	11.2	1.27
AGILE parameters	17.6	5.2	0.360

Table 2: Power consumption when the TA1 is operated with the nominal values and with the AGILE parameters; IVss and IVdd are the currents drawn on the -2 V and +2 V power supplies.

In the testbeam HDI, the pitch adaption is still made through a upilex fanout.

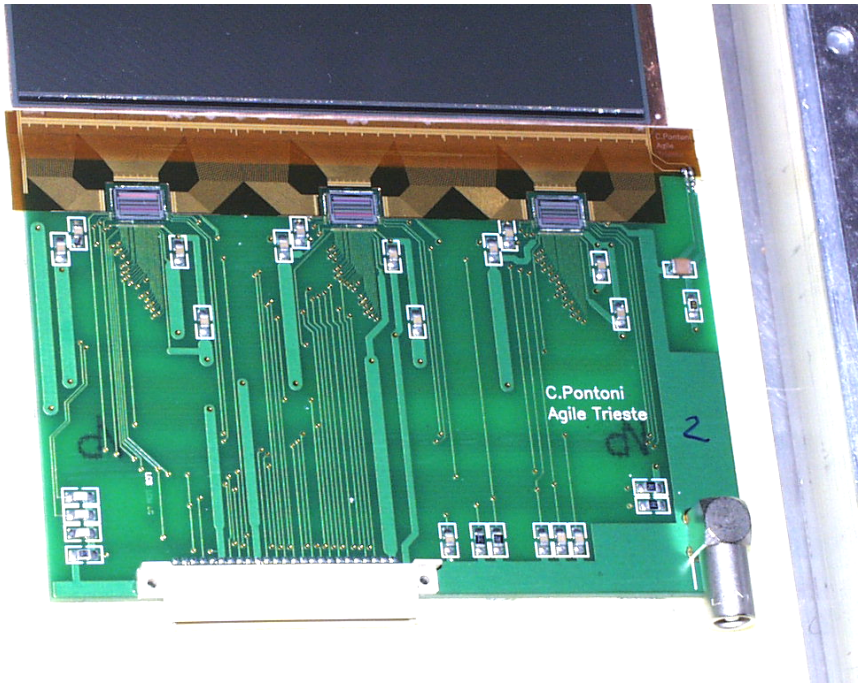

Figure 9: Picture of the testbeam HDI.

Fig. 9 is a picture of the testbeam HDI:

- in the lower part, there is a 50-pin ERNI connector for the digital/analog signals and the low voltages and a lemo connector for the detector bias voltage; all the voltages are decoupled close to the ASICs;
- in the upper part there are the three TA1s: the bonding pads for the control signals are positioned on the lower side of the ASIC and partly on the left and right sides while the input pads for the silicon signals are positioned on the front of the ASIC (64 pads) and on the sides (32 per side).

The testbeam HDI, which is a two layer PCB card, has been manufactured by TecnoMas-

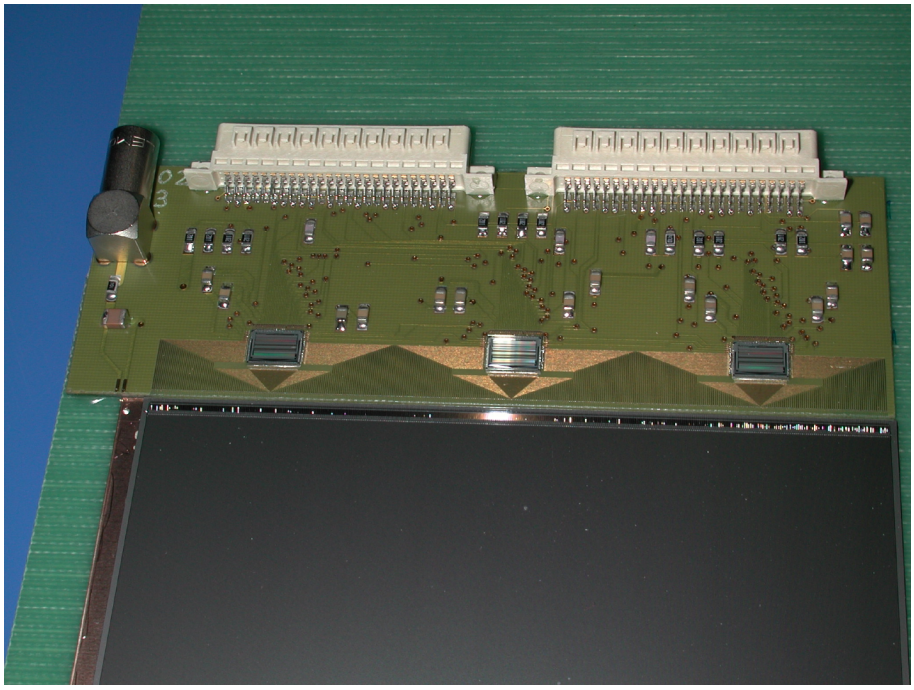

Figure 10: Picture of the new version of the HDI, with the pitch adapter included on the HDI itself.

ter [3] and assembled by Mipot [4].
The final HDI will have a dimension of 9.5×3 cm^2 to be compared with the testbeam one (10×6 cm^2). Fig. 10 shows the 4-layer version of the HDI with the pitch adapter included on the HDI itself, manufactured by the CERN EST Division.

2.2.3 The Frontend and Trigger Board - FTB

The FTB is the supervisor board of the Tracker frontend (see fig. 11); it has to interface the silicon detectors to the readout system and to handle properly the trigger signals, the power lines and the Tracker housekeepings (currents and temperatures used to check the operational status of the Tracker). Each FTB corresponds to a board of 39×27 cm^2 located on one of the Tracker lateral sides.
The Tracker FEE for the x (y) views is organized into 7 logic units (FEBs). Each FEB controls 2 views (2 x or 2 y views). Each FTB handles 7 FEBs. The two FTBs are connected with a flat cable. The connection between the FTB and the HDIs is done with suitable flexible cables.
A block diagram of the FTB functions is shown in fig. 11. Starting from the top, the FTB goals are:

[3] Tecnomaster, Italy
[4] Mipot S.p.A., Cormons (GO), Italy

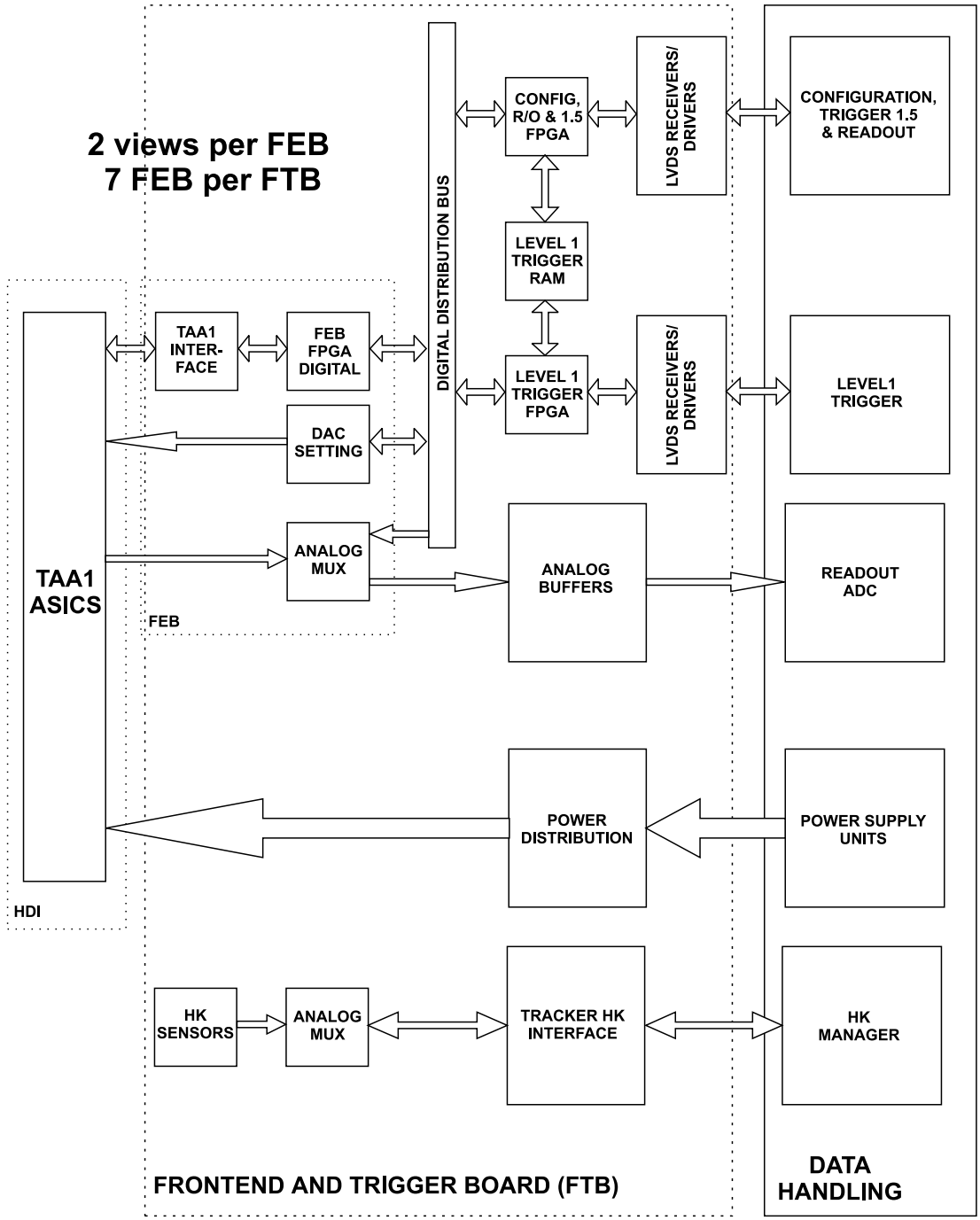

Figure 11: Schematic representation of the FTB.

- to configure the various parts of the Tracker FEE;
- to distribute the digital signals needed for the Tracker readout phase;
- to serialize the trigger bits for the Level 1.5 trigger (see next subsection);
- to generate the Tracker Level 1 trigger signals and send them to the data acquisition

box (Data Handling box, DH);

- to handle the analog signals coming from the triggered TAA1s during the readout phase;
- to distribute and filter power;
- to handle the housekeepings.

The comunication between the FTBs and the DH box is implemented through a set of serial buses, power lines and analog outputs.

2.3 The trigger and readout electronics

The AGILE-GRID trigger is divided into 3 levels, two hardware ones (Level 1 and 1.5) and a software one (Level 2) (3).
The Tracker readout system consists in a synchronous part and an asynchronous one to reduce the dead time of the instrument.
A detailed description of the trigger and readout system of the satellite is given in (4).

2.3.1 The hardware triggers: Level 1 and 1.5

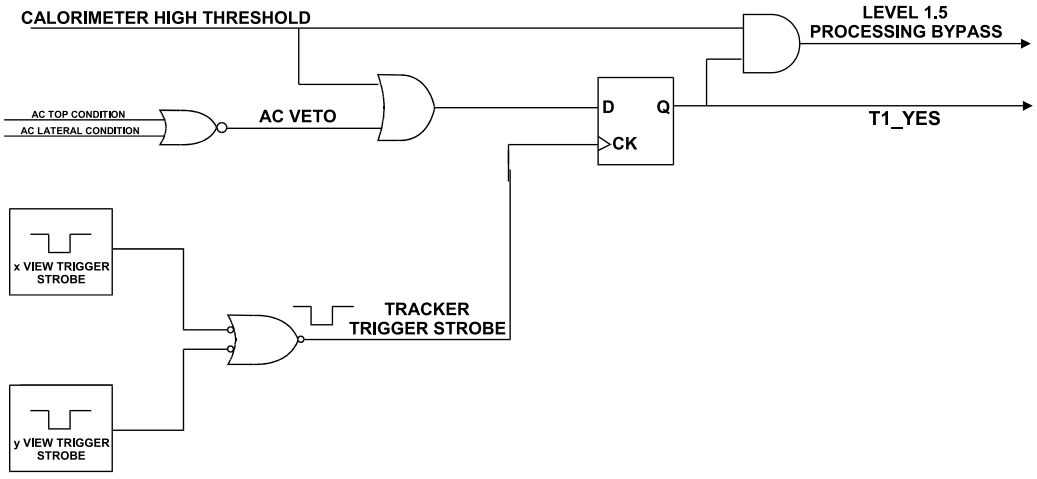

Figure 12: Schematic representation of the baseline Level 1 trigger philosophy.

For the AGILE orbital environment, we expect a ratio of cosmic γ-rays to total background (charged particles and albedo photons) event rates near 10^{-4} for γ-ray energies larger than 100 MeV.
The main goal of the two hardware trigger levels is to identify the γ-rays and avoid the

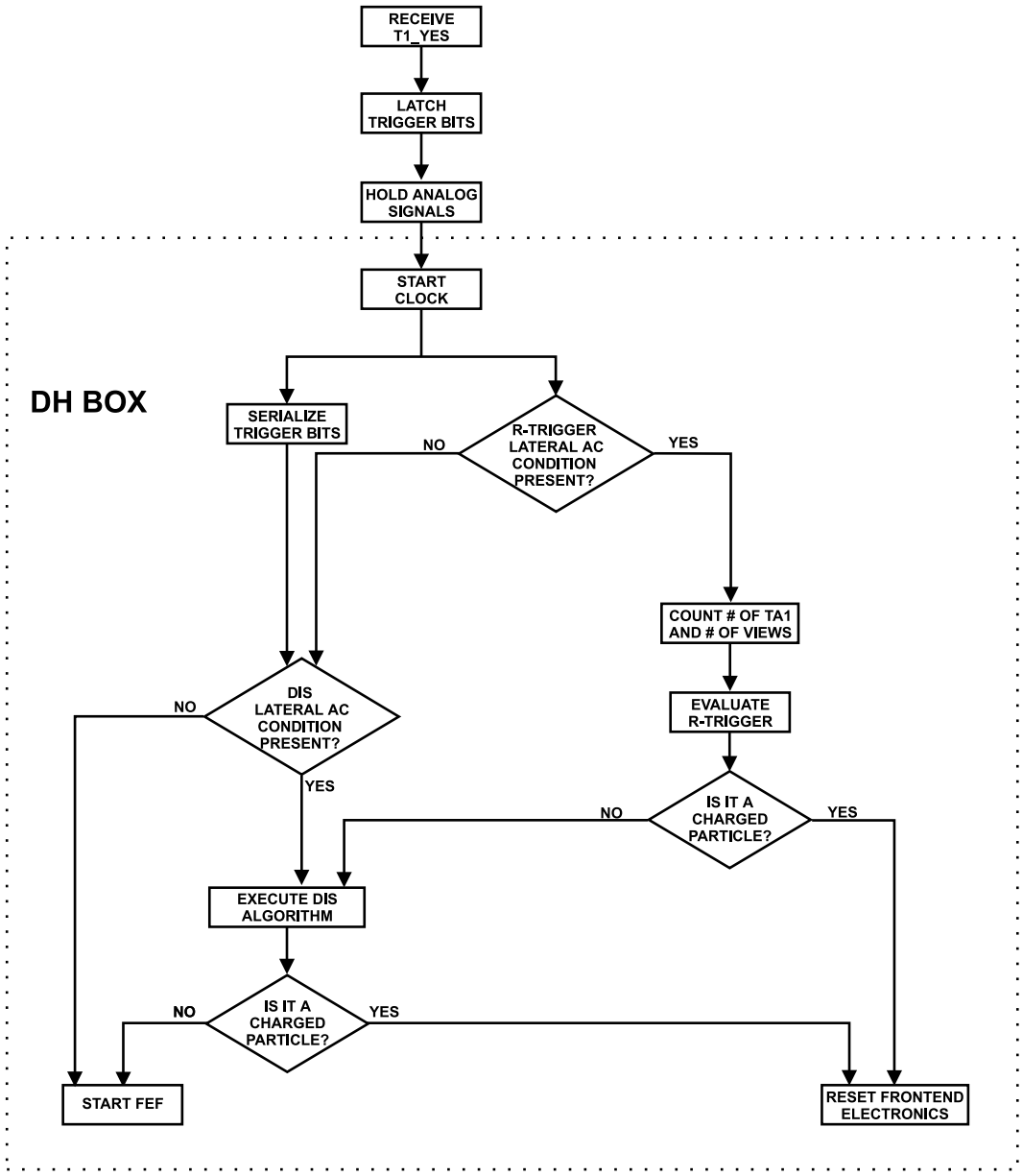

Figure 13: Flow diagram of the Level 1.5 trigger operations.

frontend freeing procedure for background events, thus reducing these events of a factor near 100. In the following, we summarize the basic ideas of the two trigger stages:

- Level 1:
  - baseline philosophy (fig. 12): the Level 1 trigger is given by the coincidence of 3 out of 4 consecutive Silicon Tracker views (x and/or y view trigger strobe in fig. 12), indipendently for the x and the y views. Veto signals from the top AC and a suitable combination of the lateral ACs are foreseen (AC veto in fig. 12). For energetic photons ($E >1$ GeV), an indipendent trigger can be

generated by a high energy release in the minicalorimeter (calorimeter high threshold in fig. 12).

- time available for the decision: $<$1-1.3 μs; if the decision is positive a T1_YES signal is generated, otherwise the detector is kept blind for $<$10 μs (T1_NO status)
- expected deadtime: a T1_NO rate of 1 kHz corresponds to a deadtime of 1%.

- Level 1.5:
  - baseline philosophy: once the T1_YES has been generated, all the trigger bits are latched and, upon receipt of the hold signal, all the analog signals (TAA1s) are set to "hold"; a clock (24 cycles at 5 MHz) generated by the DH box serializes the trigger bits on one line per FEB for the Level 1.5 processing.
    The same clock, while transferring the bits, if there is a lateral AC condition, enables the DH to count the number of x (y) triggered ASICs and the number of x (y) triggered views and, by using a RAM, to evaluate the so called "R-trigger", that is the ratio of the number of triggered ASICs and the number of triggered views; this ratio has a value of the order of 1 for a background event such as a single charged particle (1 ASIC per view) and greater for a cosmic γ-ray (if a photon has converted, two particles are produced which can trigger more than one ASIC per view).
    If the R-value indicates the presence of a charged particle, the Level 1.5 processor discards the event before starting the distance-algorithm processing (see flow diagram in fig. 13).
    The distance-algorithm processing is done by comparing the relative position of the triggered ASICs with respect to the hit lateral AC as shown in fig. 14. If only one of the lateral ACs gives a signal, the distance of the triggered ASICs from that AC is computed. This distance increases if the event is a charged particle which has entered the AC (right part of fig. 14) and decreases if one particle of the pair created by the photon hits the AC (left part of fig. 14).
    This algorithm is in practice a veto of the frontend freeing phase.
  - required time for the decision: for the R-trigger, it is $<$5 μs (essentially the clocking phase duration); for the Level 1.5 processing it is $\approx$20 μs. The time needed to reset the Silicon Tracker FEE is 10 μs.
  - expected deadtime: from the simulation we estimate to have a T1_YES rate of 500 Hz and to cut 400 Hz with the R-trigger and 30 Hz more with the Level 1.5 processing; the total deadtime in case of a negative decision, after Level 1.5 processing, is then

$$(5\mu\text{s} \times 500\text{Hz} + 20\mu\text{s} \times 100\text{Hz} + 10\mu\text{s} \times 400\text{Hz}) \times 10^{-6} = 0.85\%$$

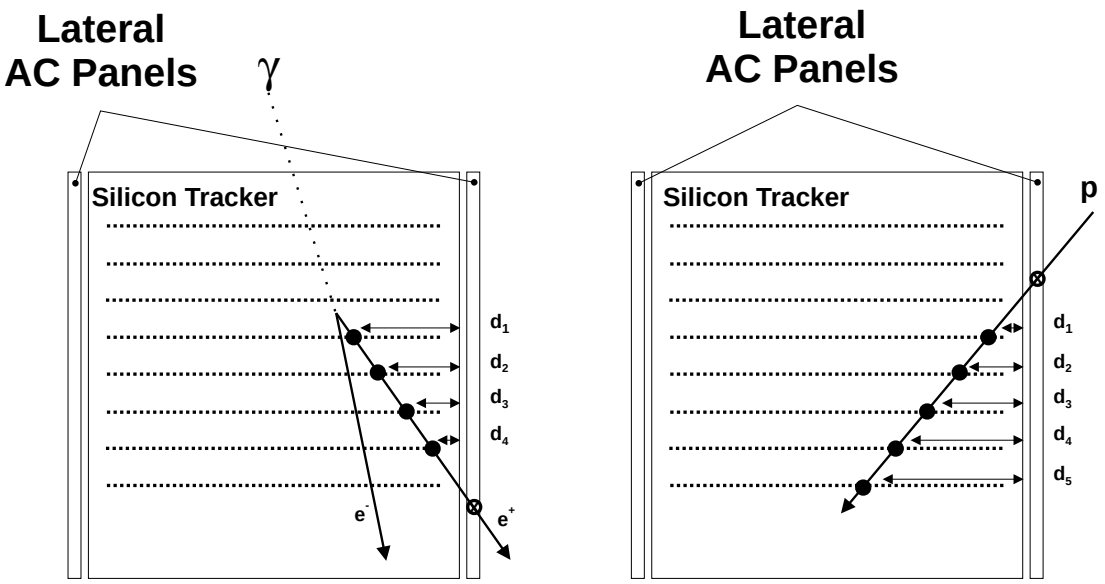

Figure 14: Distance-algorithm processing in the Level 1.5 phase.

2.3.2 The frontend freeing

To reduce the time needed by the readout phase, a sparse readout will be implemented. Thus, only the TAA1s that have given a trigger signal will be read.
Each ASIC trigger bit is latched upon receipt of a T1_YES signal and stored in a shift register on the FTB itself. The frontend freeing phase is controlled by a 5 MHz clock, so that each TAA1 needs 25.6 μs to be readout. Each ADC board controls two views (24 ASICs). The maximum number of TAA1s that can be read for each ADC is 8 for a maximum dead time of 200 μs.
The total number of 12-bit ADCs is 14, organized in 4 boards (TAB, Tracker Acquisition Board). Fig. 15 describes the working principle of the Tracker readout board, which is controlled by a FPGA: the four signals coming from four FEBs are digitized by four 12-bit ADCs with a 5 MHz clock. The four digital ADC outputs are multiplexed with a 20 MHz clock and stored in a static RAM.
The frontend freeing is the last operation of the synchronous phase of the Tracker readout.

2.3.3 The data preprocessing and the Level 2 trigger

The data preprocessing and the Level 2 trigger are asynchronous with respect to the system timing and thus they do not introduce dead time.
The data preprocessing compresses the event information in order to transfer it to the payload CPU. It consists of the following phases:

- pedestal subtraction: each channel pedestal is computed before each observation phase and stored in a dedicated memory region

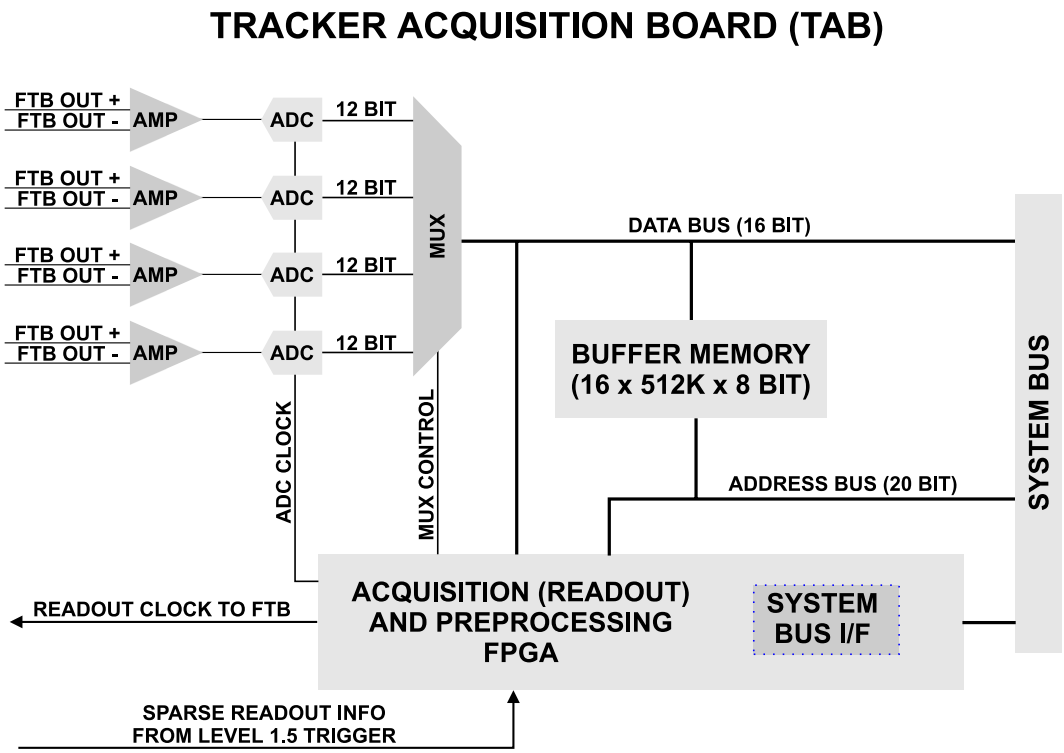

Figure 15: Schematic representation of the TAB.

- common mode subtraction: for each ASIC the mean value of the strip ADC counts is computed and then subtracted from the strip pulse height. The noisy and the dead channels are not used in this operation, which is implemented in hardware.

- zero suppression: the strips which have a pulse height lower than a chosen threshold (expressed as a function of the channel noise rms; e.g. 2 σ) are suppressed. The data compression factor is estimated to be 96%.

The Level 2 processing is a software-only process performed by the CPU. For each Tracker view the clusters are identified and their information (position, charge, number of strips) is stored.
The algorithms used for the Level 2 are based on the same criteria of the Level 1.5 trigger with a higher modularity, since they are performed at the cluster level. These algorithms are still under study and they will be described in a forthcoming publication.
The time needed for the Level 2 phase is of the order of 5 ms. The input event rate is 70 Hz while the output one (corresponding to the events that are transmitted to ground) is 10-20 Hz.

3 The silicon detector performance

The final prototype of the silicon detector has been tested with the TA1 version of the frontend ASIC during a testbeam period at the T11 beamline at the CERN PS (East Hall, May 1-11, 2000).
The main features of the beam are summarized in tab. 3; for a detailed description, see (5).
As far as the beam particle composition is concerned, the relative fraction of the differents types is shown in fig. 16.

Maximum design momentum	3.5 GeV/c
Theoretical momentum resolution	1.9%
Calculated beam cross-section	18(h)$\times$10(v) mm^2
Production angle	149.2 mrad
Angular acceptance	$\pm$6.2(h) mrad, $\pm$19.2(v) mrad

Table 3: Main features of the T11 beam (h = horizontal, v = vertical).

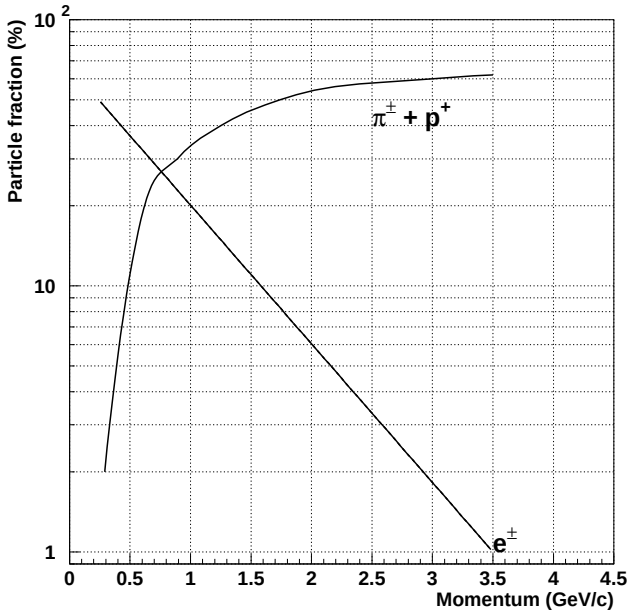

Figure 16: Particle composition of the T11 beam as a function of the energy.

The main goal of the test was to confirm and/or suggest changes to the design of the detector in order to start the final production. In the following subsections, we describe the testbeam and the detector setup and the main results we have obtained.

3.1 Testbeam setup

Fig. 17 shows the testbeam setup, which consists of:

- a Cherenkov counter for particle identification, which is part of the T11 beam instrumentation, followed by the last magnet of the T11 beamline;
- a system of two plastic scintillators (S1 and S2) of 3×5 cm^2 and 1 cm thick, for the trigger;
- a couple of delay wire chambers (6) for the beam characterization and monitoring;
- a system of 3 *x-y* silicon telescopes (7) for the tracking. Each telescope is made of two single-side AC-coupled silicon detectors of 3.2×3.2 cm^2 with a readout pitch of 50 μm and a floating strip configuration; the detector is readout by VA2 ASICs (8);
- the detector under test which is shown in fig. 6; it is an AGILE ladder made of four HAMAMTSU prototypes connected together with 17 μm wire bondings and readout by TA1s;
- the AGILE top anticoincidence scintillator and two of the bars of the CsI (Tl) minicalorimeter; the test results of these items will be the subject of other publications.

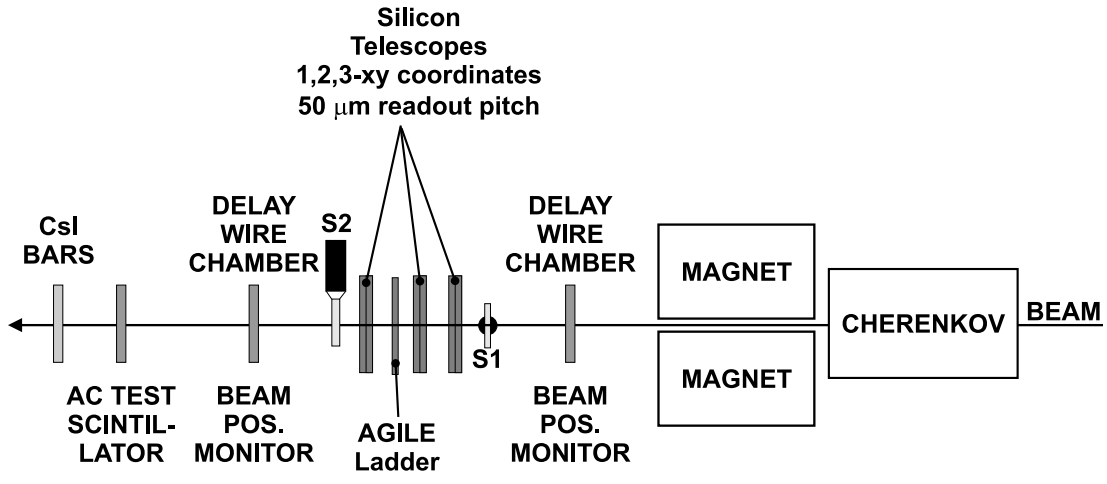

Figure 17: Testbeam setup on the T11 beamline at the CERN PS for the May AGILE run.

Fig. 18 shows the testbeam data acquisition system, which can be divided into three blocks:

- trigger logic: the signals from the scintillators and the Cherenkov counter are discriminated and sent to the trigger logic for the generation of the DAQ trigger needed by the main acquisition board, the Viking Sequencer [6]; the same logic treats the TA1 trigger signals when digitized;
- beam monitoring: the signals from the DWCs and the Cherenkov counter are readout by a set of TDCs (LeCroy 1176 and 2228A) and used in the offline analysis;
- detector test: the silicon strip signals (the 1280 strips of each of the three telescopes and the 384 ladder strips) are readout by four 10 bit VME ADCs (Sirocco [6]) while the information of the CsI bars is read by a 10 bit ADC CAEN V550.

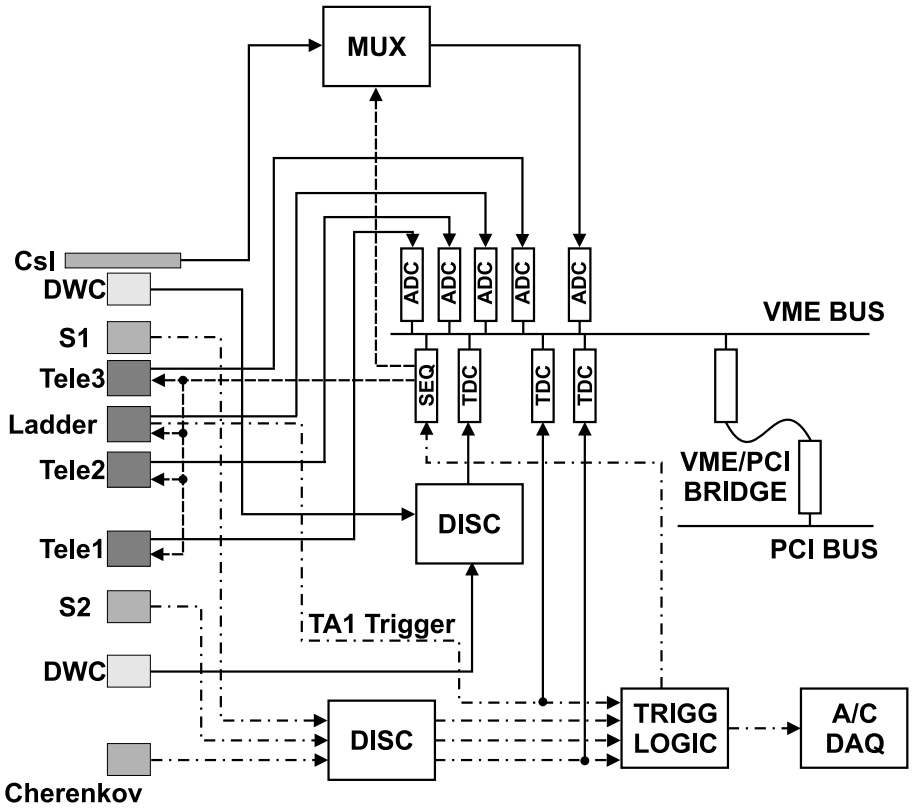

Figure 18: Testbeam data acquisition system.

The anticoincidence had an indipendent data acquisition system which is not shown in fig. 18.
As far as the hardware is concerned, we adopted the VME standard while the CAMAC is accessed by means of a CES CBD8210 branch driver.

The DAQ system has to fulfil the following tasks:

- generate the timing sequence for the readout when a trigger signal is present;

[6] LEPSI, Strasbourg, France

- get the information from the detectors (the DWCs, the telescopes, the ladder and the CsI bars) and write it on disk;
- check the run conditions and the working parameters of the TA1s;
- display the monitor histograms.

The DAQ system has been developed so that each task is controlled by a separate process. The inter-process communication is performed via TCP/IP using the RPC protocol (9).
This approach would allow the distribution of the available resources in a trasparent way across the different machines connected to a network.
In the present setup, all the processes run on a PC with an Athlon 500 MHz processor with the Linux operating system. The access to the VME is done through a Bit3 Mod. 617 controller (10).
The data acquisition frame relies on the Tcl/Tk package (11), which provides a flexible structure to implement the different functions and to control them via a GUI. The addition of the Tcl-DP package (12) has given the possibility to easily distribute the functionalities across the network. Each elementary action of each task has been implemented as a Tcl command that can be executed locally or remotely via Tcl-DP.

Fig. 19 shows the relationship among the different processes for what concerns the data and command flow, while fig. 20 presents the graphical interface of the processes:

- DAQ CONTROL: it is the main client-only process and it is the supervisor of the activity of the different tasks. It sends commands to the VME SERVER to configure the system and to start the acquisition run. It receives information on the run itself (run number, number of events, run status) from the DAQ MONITOR.
- DAQ MONITOR: it is a server-only process. It stores the run status and the number of the last processed event and it fills the histograms with the data coming from the VME SERVER. The DAQ CONTROL has access to the status data to start/stop the run.
- VME SERVER: it is a client process with respect to the DAQ MONITOR, to which it sends the data for the monitoring, and a server one with respect to the DAQ CONTROL, from which it receives commands. Since it is the only process which has physical access to the VME bus, it is responsible both of the readout system configuration and of the readout itself. It is also the process which writes the data on disk (DATA LOGGER).

The DAQ code is written in C and C++ while the histogramming part is built using HPLOT (13).

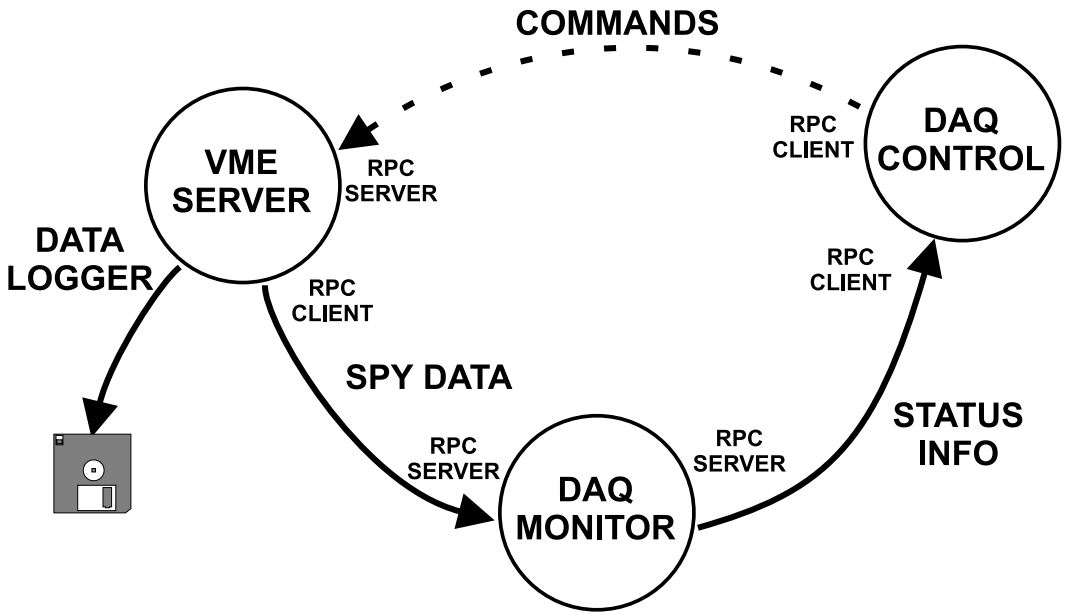

Figure 19: Schematic of the testbeam data acquisition system.

3.2 Testbeam results

More than 2.3 million events have been collected in order to study:

- the ladder behaviour according to the region hit by the beam (different silicon tile or different region inside the tile);
- the ladder behaviour as a function of the angle of incidence of the beam with respect to the silicon strips, in terms of cluster pulse height, signal to noise ratio, number of strips per cluster. The incidence angle is the angle between the beam and the plane of the silicon strip tile. The range between 30° and 90° (that is the interesting region for AGILE) has been scanned in steps of 15°. Fig. 21 defines the incidence angle of the beam: the tracks have been chosen using the *y* telescope information in order to guarantee that the beam is contained in a horizontal plane and the *x* information to select tracks with the same angle.
- the trigger efficiency of the ladder as a function of the incidence angle of the beam.

Pedestal data for all the strips are collected in dedicated runs and then analized offline to compute the pedestal value for each strip (mean value of the distribution of all the events) and the noise rms before and after the subtraction of the common mode.

All the results presented in the following sections have been obtained with a positive charged particle beam (mostly pions) characterized by a momentum of 2 GeV/*c*.

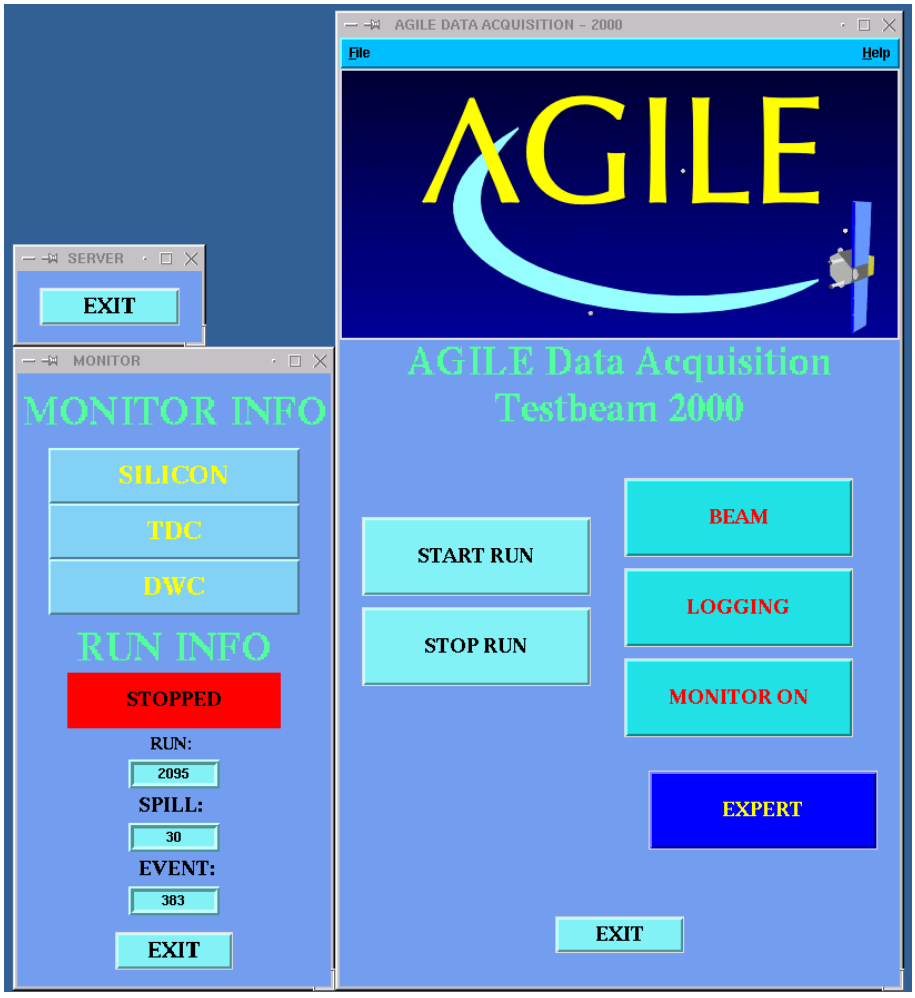

Figure 20: Graphical interface of the testbeam DAQ system, representing the 3 processes described in fig. 19.

3.2.1 Noise

Given the characteristics of the detectors under test, it is possible to compute the expected noise for the AGILE ladder.
From (14), the different noise contributions are:

- from the leakage current:

$$ENC_{leak} = \frac{e}{q}\sqrt{qI_{leak}T_p/4}$$

  with e natural logarithm base, q electron charge, I_{leak} total strip leakage current and T_p shaper peaking time (in our case 5 μs);

- from the polarization resistors:

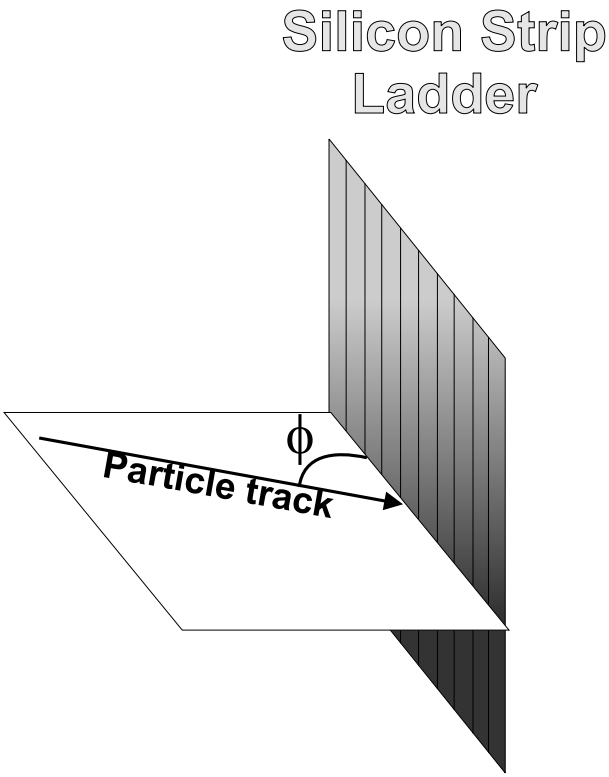

Figure 21: Definition of the incidence angle of the beam with respect to the detector plane.

$$ENC_{res} = \frac{e}{q}\sqrt{\frac{kTT_p}{2R_p}}$$

with kT=0.025 eV at T=300 K and R_p biasing resistor;

- from the resistance of the metal strip:

$$ENC_{ms} = \frac{C_t e}{q}\sqrt{\frac{kTR_{ms}}{6T_p}}$$

with R_{ms} total resistance of the metal strip end to end and C_t total strip capacitance;

- from the readout ASIC:

$$ENC_{TA1} = 165 + 6.1 \cdot C_t$$

as given by IDE AS.

The total noise is computed as the sum in quadrature of the different components:

$$ENC_{tot} = ENC_{TA1} \oplus ENC_{ms} \oplus ENC_{res} \oplus ENC_{leak}$$

Tab. 4 shows the different noise contributions expressed in rms electrons for an AGILE Silicon Tracker ladder.

Noise Contribution	Value (rms e-)
ENC_{leak}	227
ENC_{res}	508
ENC_{ms}	45.5
ENC_{TA1}	490
ENC_{tot}	743

Table 4: AGILE Silicon Tracker noise contributions for a ladder expressed in rms electrons.

Fig. 22 shows the distribution of the rms noise of all the ladder channels before (13 ADC) and after the common mode (CM) subtraction (5.9 ADC). The common mode component is given by the fluctuation of all the channels at the same time and is mainly due to pickup on the detector bias voltage. A too high CM could prevent the possibility of setting the trigger threshold at 1/4 of a MIP.

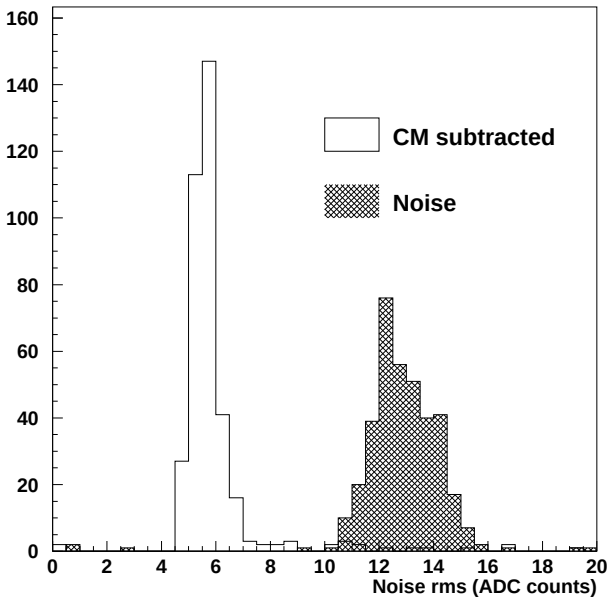

Figure 22: Ladder noise rms before and after the CM subtraction.

3.2.2 Ladder behaviour

Some of the main features of the silicon detector (implant width, interstrip capacitance) have been chosen in order to have more than one strip per cluster, thus obtaining a better position resolution, while at the same time maintaining the signal high enough on the readout strips to generate a trigger even when the particle crosses the floating ones.

Fig. 23 shows the beam profile measured by the ladder (upper plot) and the correlation between the ladder and one of the *x* telescope position (lower plot).

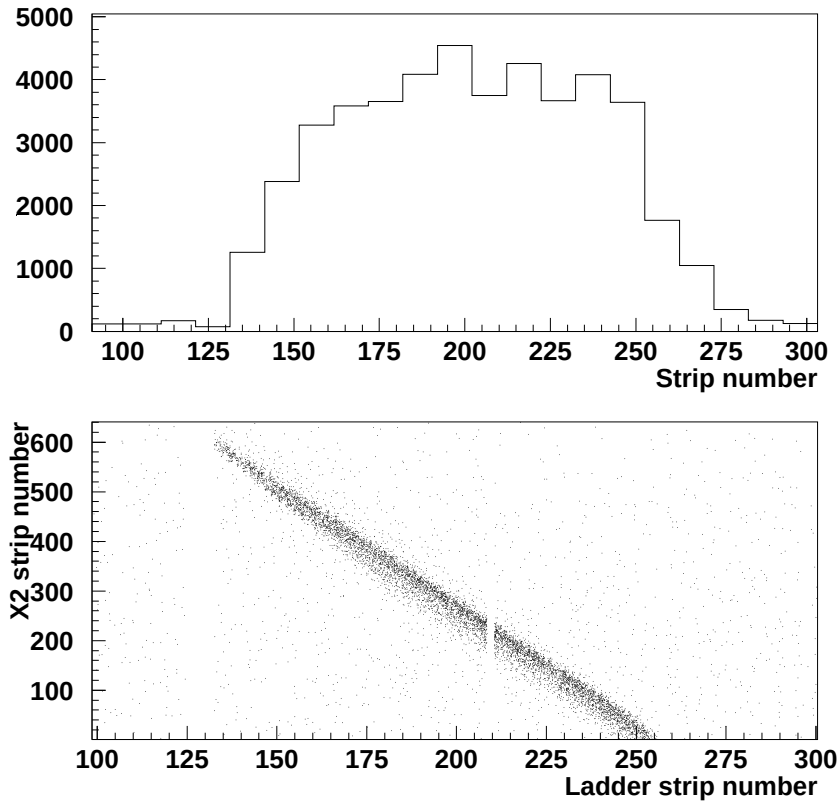

Figure 23: Ladder beam profile (upper plot) and correlation between the ladder and one of the *x* telescope position (lower plot); two of the ladder strips have been excluded in the offline analysis because of their high noise.

The following method has been used to define a cluster in each event:

- the pulse height of each strip PH_i is defined as:

$$PH_i = raw_i - ped_i - CM$$

where raw_i is the raw content of the readout channel in ADC counts, ped_i the channel pedestal as computed using the pedestal run and CM the common mode contribution for the event;

- for each event a procedure searches for the strip with the maximum signal, which has to be greater than 5 times the noise rms of the strip itself (σ_i);
- for each event the same procedure considers the strips contiguous to the one with the maximum signal which are characterized by a ratio $PH_i/\sigma_i > 3$. The group of strips obtained is called a cluster.

The choice of the cuts for the strip with the maximum signal (5 σ) and for the nearby ones (3 σ) is explained by fig. 24, where the "pull" (defined as the ratio of the strip *PH* and its noise) for the strip with the maximum signal (upper plot) and for the noise (lower plot) is represented.

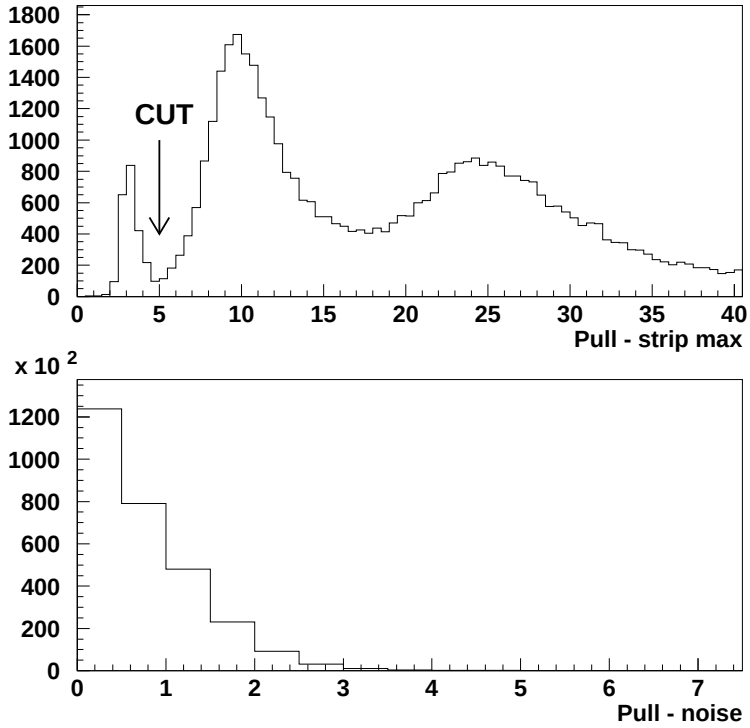

Figure 24: Upper plot: pull distribution for the strip with the maximum signal; the peak on the left is the one due to the noise while the other two correspond to the case in which the particle crosses a readout strip (higher signal) or a floating one (lower signal). Lower plot: pull distribution for the noise.

Fig. 25 shows the cluster pulse height as a function of the incidence angle of the beam. The fit with a 1/cosθ function is superimposed.

Fig. 26 shows the cluster pulse height in ADC counts (upper plot) and the signal to

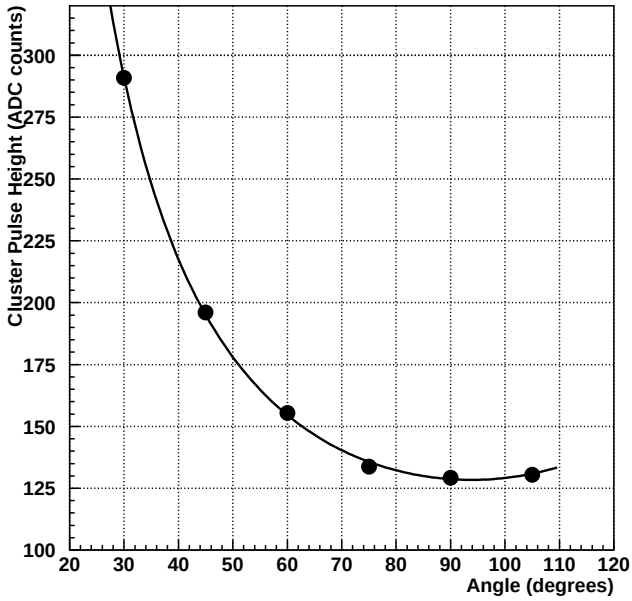

Figure 25: Cluster pulse height as a function of the incidence angle of the beam with respect to the strip plane. The fit has been performed with a 1/cosθ function.

noise ratio (SNR, lower plot) defined as:

$$\mathrm{SNR} = \frac{\sum_i \mathrm{PH_i}}{< \mathrm{noise} >}$$

where the sum is made over the strips of the cluster, PH_i is the pulse height of the i-th strip and $< noise >$ is the mean value of the cluster noise.
Both histograms have been obtained with a beam perpendicular to the detector and they have been fitted with a simplified Landau function (15):

$$F(\lambda) = \frac{1}{\sqrt{2\pi}} \exp^{-0.5(\lambda + \exp^{-\lambda})}$$

where $\lambda = \frac{\Delta E - \Delta E_{MP}}{\xi}$ and $\xi = FWHM/4.02$.

Fig. 27 shows the number of strips per cluster as a function of the incidence angle of the beam. Even for large angles with respect to the pointing direction of AGILE, the mean value is below 5, which is the maximum number of strips per cluster that can be transmitted to ground due to telemetry bandwidth limitations.

3.2.3 Position resolution

To evaluate the position resolution of the AGILE silicon detector, the track was reconstructed using the information of the silicon telescopes nearest to the ladder and the distribution of the residuals, that is the distribution of the difference of the extrapolated

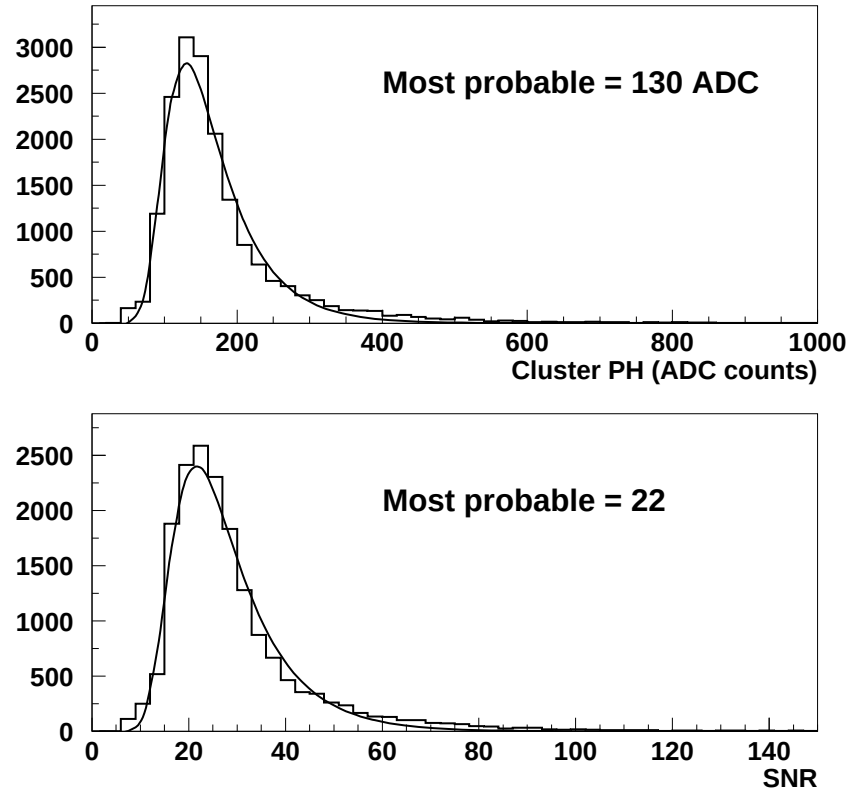

Figure 26: Cluster pulse height (upper plot) and SNR (lower plot) for an incident beam perpendicular to the detector plane. The fit has been done with a simplified Landau function described in the text.

position on the ladder and the one measured by the ladder itself, was plotted.
The ladder measured position is computed with a center of gravity method, weighting the position of each cluster strip with the pulse height of the strip itself.
Since the beam momentum is low (2 GeV/c), the multiple scattering due to the material between the two telescopes has to be taken into account. The multiple scattering contribution to the telescope position resolution has been measured replacing the ladder with the third telescope. The result has been compared with the theoretical calculation and the simulation.
Fig. 28 shows the residual distribution obtained with a normal incidence beam of 2 GeV/c. The position resolution can be evaluated from the sigma of the gaussian fit σ_{fit} as:

$$\sigma_{res} = \sqrt{\sigma_{fit}^2 - \sigma_{ext}^2}$$

where σ_{ext} is the uncertainty introduced by the track reconstruction of the silicon telescopes, which is due to the multiple scattering.

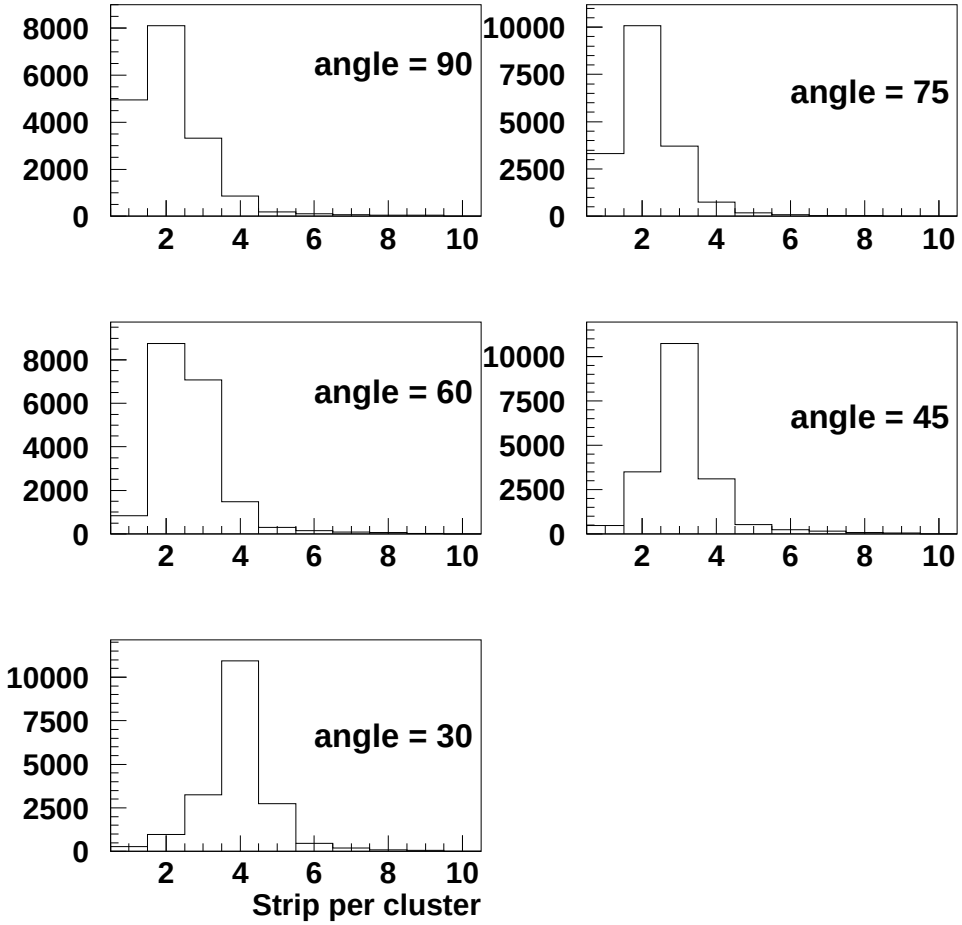

Figure 27: Number of strips per cluster as a function of the incidence angle of the beam.

Tab. 5 presents the position resolution of the AGILE detector as a function of the incidence angle of the beam.

Fig. 29 shows the advantage, in terms of spatial resolution, resulting from using the analog information on the charge collected by the silicon strips. As far as the digital evaluation is concerned, the cluster is identified by applying a 3σ cut to the strips and the hit position is the center of gravity of the cluster (in this case, all the strips in the cluster have the same weight).

3.2.4 Trigger efficiency

One of the most innovative features of the AGILE Tracker is represented by the autotrigger capability.

Dedicated runs have been performed in order to study the trigger efficiency of the sili-

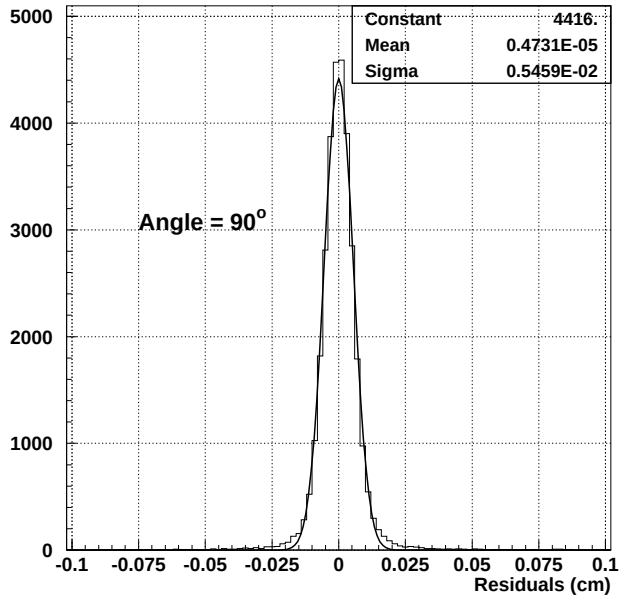

Figure 28: Position resolution at normal incidence of the beam. The value obtained with the fit is the convolution of the real position resolution of the ladder and of the error introduced by reconstructing the track with the telescopes.

Angle (degrees)	σ_{fit} (μm)	σ_{res} (μm)
90	55	47
75	47	37
60	51	41.3
45	67	59
30	116	110

Table 5: Position resolution of the AGILE detector as a function of the incidence angle of the beam.

con strips as a function of the incident angle of the beam. The efficiency is evaluated considering for each threshold the number of events with a high pulse height in the strip with the maximum and no trigger signal. The presence of a trigger signal is measured with a multihit TDC that follows the time development of the trigger signal itself since it samples up to 16 transitions.

Fig. 30 shows the time interval (y axis) in μs between the particle crossing and the trigger signal generation as a function of the signal amplitude (x axis) in the strip with the maximum. The plot has been obtained with a 2 GeV/c beam impinging orthogonally on the silicon detector. The TA1 threshold has been set to 50 keV (0.5 MIP).

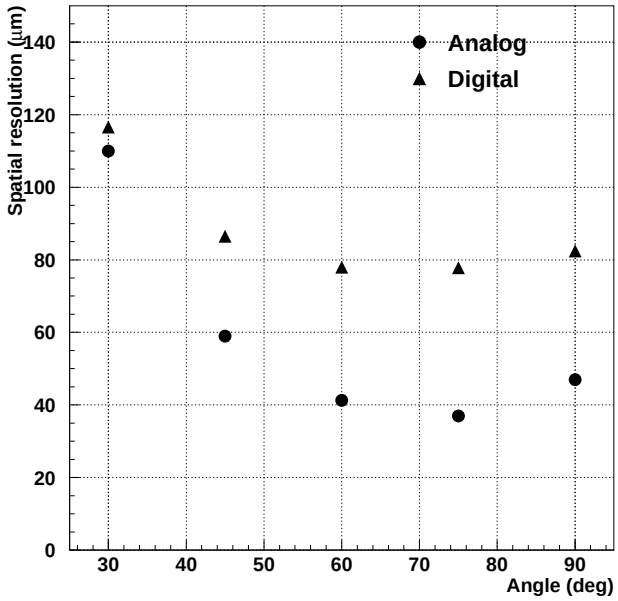

Figure 29: Comparison between the digital and the analog position resolution for the AGILE silicon detector.

The lower is the pulse height, the higher is the time needed to generate the trigger.

From the trigger efficiency point of view, the worst condition is represented by a particle crossing a floating strip, which corresponds to the minimum signal seen by the nearby readout ones. Fig. 31 shows the signal amplitude of the strip with the maximum as a function of the incidence angle of the beam for the two extreme cases of the particle crossing the center of a readout strip or of a floating strip. The line represents a threshold of 1/4 of a MIP. The signal amplitude corresponds to the most probable value of the Landau function (upper plot in fig. 26).
For all the angles the signal is higher than the threshold, ensuring the maximum trigger efficiency. If the detector noise increases, thus requiring an increase in the threshold value, the efficiency will decrease for tracks impinging orthogonally. Fig. 32 shows the efficiency as a function of the threshold value for two incident angles of the beam. The measured efficiency values are written in tab. 6.

3.3 Comparison between data and simulation

From the testbeam data, it is possible to evaluate a set of detector parameters which are fundamental for the simulation of the behaviour of the entire satellite.
The testbeam setup has been simulated using GEANT 3.21 (16).
The silicon strips are implemented by dividing the silicon itself in slices of 121 μm and the energy information of each of these sub-volumes is saved for each event.

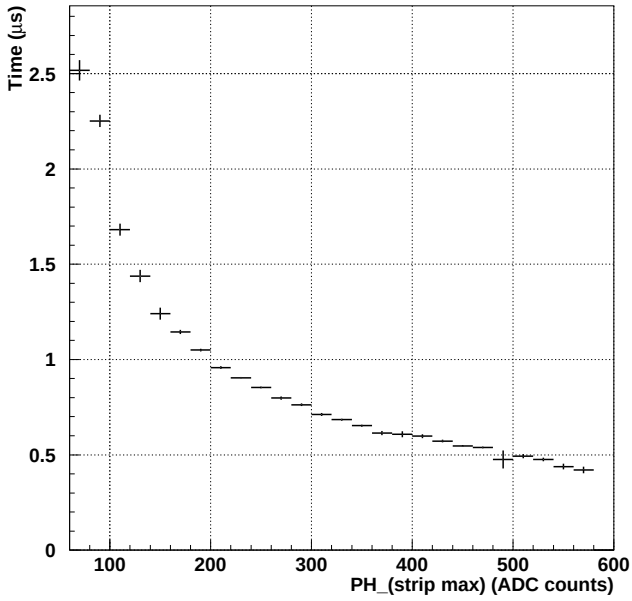

Figure 30: Time interval between the particle crossing and the trigger signal generation as a function of the signal amplitude in the strip with the maximum.

Threshold (keV)	ε (%) at 90°	ε (%) at 60°
25	99.46	
38	99.4	
51	99.13	99.25
64	98	99.57
76	85.1	99.55
89	68	98
102	58	91.4

Table 6: Trigger efficiency as a function of the threshold value for an incident angle of the beam of 60° and 90°.

The capacitive coupling between the strips is implemented as described in fig. 33: the energy realeased in each strip is multiplied by a factor and assigned to the nearby readout strips. This procedure is applied for each event and for all the strips, and the signal obtained has to be compared with the measured one.

Fig. 34 shows the comparison of the position resolution as a function of the incidence angle for data and simulation.

Fig. 35 shows the comparison data-simulation for the function η which represents the way the signal is divided between adjacent strips:

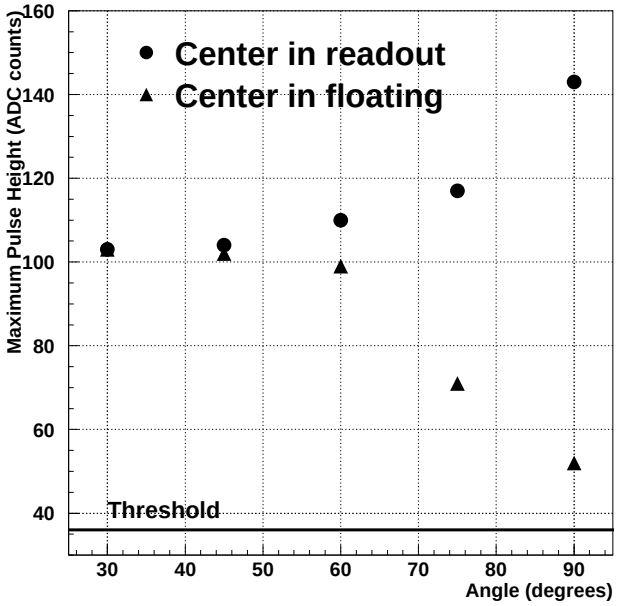

Figure 31: Signal amplitude of the strip with the maximum as a function of the incidence angle of the beam for the two extreme cases of a particle crossing the center of a readout strip or of a floating one.

$$\eta = \frac{PH_{max} - PH_{max-1}}{PH_{max} + PH_{max+1}} \quad \text{if} \quad \mathrm{PH_{max-1}} > \mathrm{PH_{max+1}}$$

$$= \frac{\mathrm{PH_{max+1}} - \mathrm{PH_{max}}}{\mathrm{PH_{max+1}} + \mathrm{PH_{max}}} \quad \text{if} \quad \mathrm{PH_{max+1}} > \mathrm{PH_{max-1}}$$

where PH_{max} is the signal of the strip with the maximum and $PH_{max\pm1}$ is the signal of the nearby strip with the higher signal.

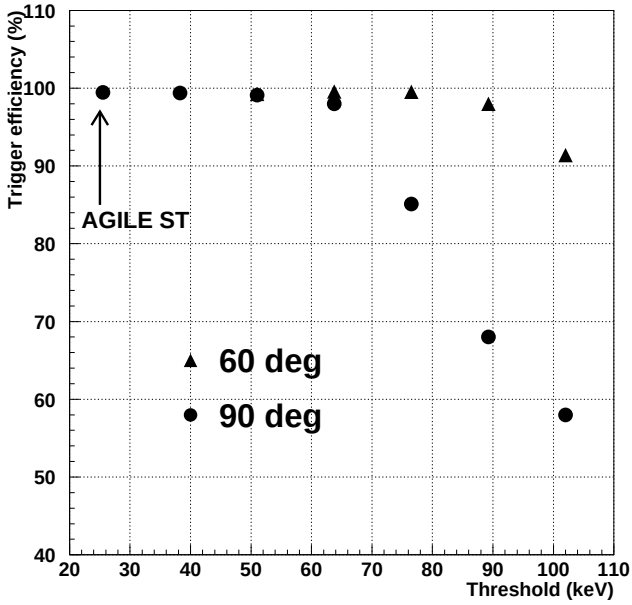

Figure 32: Trigger efficiency as a function of the threshold value for a 2 GeV/*c* beam impinging orthogonally and at 60° with respect to the detector plane.

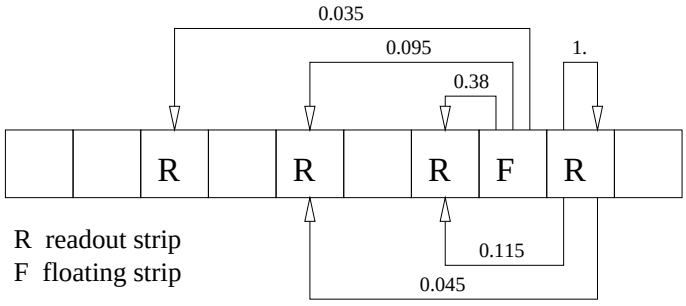

Figure 33: Schematic representation of the implementation of the capacitive coupling in the simulation. The simmetric couplings on the right are not represented.

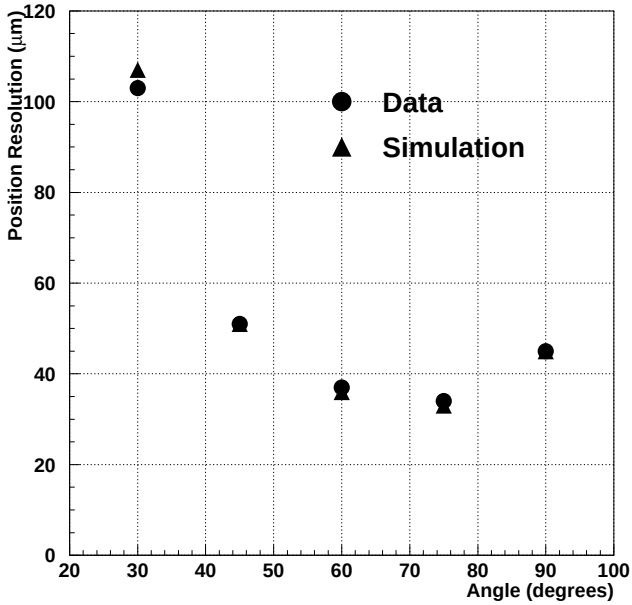

Figure 34: Comparison of the position resolution as a function of the incidence angle for data and simulation.

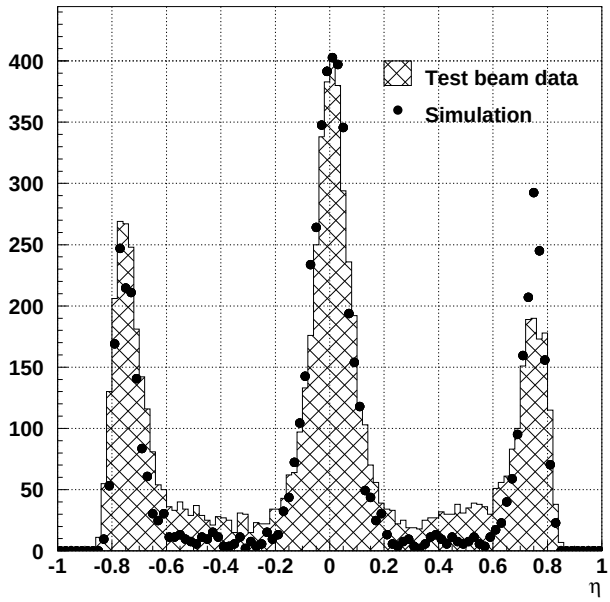

Figure 35: η function: comparison between data and simulation.

4 Conclusions

AGILE is a real step towards the future of γ astrophysics, both for the innovative technology it uses and for the performace it will reach being such an up-to-date instrument.
The AGILE heart is the Silicon Tracker. Around 43000 silicon channels will be launched in 2003 for a total of 4 m^2 of silicon detectors, which is the largest number of silicon strips as far as satellites are concerned up to now.
The silicon detector described in this paper is the largest ever built. The testbeam analysis has demonstrated the validity of the analog readout and of the floating strip principle even with a large pitch detector as this one. In this way, it has been possible to maintain under control the number of channels and thus the power needed by the instrument while at the same time obtaining a good spatial resolution.
No stability problems have arisen in the use of the ensemble detector-electronics, which is a fundamental aspect for a satellite experiment.
The final production of the AGILE silicon detectors is under way and will be completed before the middle of the year 2001.

5 Acknowledgments

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We would like to thank Thomas Ruf and the CERN EP and PS division staff for the support during the testbeam, Peter Weilhammer and Alan Rudge for the silicon telescopes and the Laben group for useful discussions.

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