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FRACTION DISCRIMINATOR SYSTEM FOR MEASURING TIME
INTERVALS UP TO 500 ns

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A BIASED TIME TO AMPLITUDE CONVERTER AND CONSTANT FRACTION
DISCRIMINATOR SYSTEM FOR MEASURING TIME INTERVALS UP TO 500 ns

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ABSTRACT

We have designed and built a compact system for measuring short time intervals, consisting of two constant fraction discriminators and one time to amplitude converter, with a biased amplifier as output stage.

1. - INTRODUCTION

The use of time of flight techniques in nuclear physics experiments is of great interest and its importance has been referred often in literature (see for example ref. (1) and the references here reported) to identify the mass of ions emitted in nuclear reactions.

The electronic chain required for this kind of experiments uses always constant fraction discriminators to generate accurate timing output pulses for Start and Stop signals and time to amplitude converter for measuring the time interval.

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As previously shown⁽²⁾, the building up different apparatus in the same module allows an improvement of the performances of the system. We have followed the same philosophy for building TOFMIS⁽³⁾, a compact system for mass identification using the time of flight technique. During its design, we have built an ad hoc time to amplitude converter (TAC), able to measure short time intervals, with four ranges (50, 150, 250, 500 ns f. s.).

Starting from the good experimental results obtained, we have assembled in a standard NIM single-width module (Fig. 1) the device described in the present report, consisting of one TAC, two constant fraction discriminators (CFDs) and one biased amplifier, as output stage.

In the next section we provide a general description of the present apparatus. In the third section the experimental results are described. The specifications are furnished in section four, while the conclusions are shown in the fifth section.

2. - GENERAL DESCRIPTION

The system described in present paper consists of different sections, each of ones, with proper controls, needs of correct inputs and provides the required outputs.

As first we begin describing the front and rear panels.

Principal BNC connectors and different controls are in the front panel (Fig. 1), and here in sequence described:

- two ten turn potentiometers to control the lower thresholds of the CFDs;
- two ten turn potentiometers to control the biased amplifier;
- two trimmer potentiometers for walk adjusting;
- BNC connectors for the Start and Stop inputs and for special purpose logical controls (coincidence and sampling inputs);
- BNC output connector for biased TAC signal;
- BNC connectors for walk inspection.

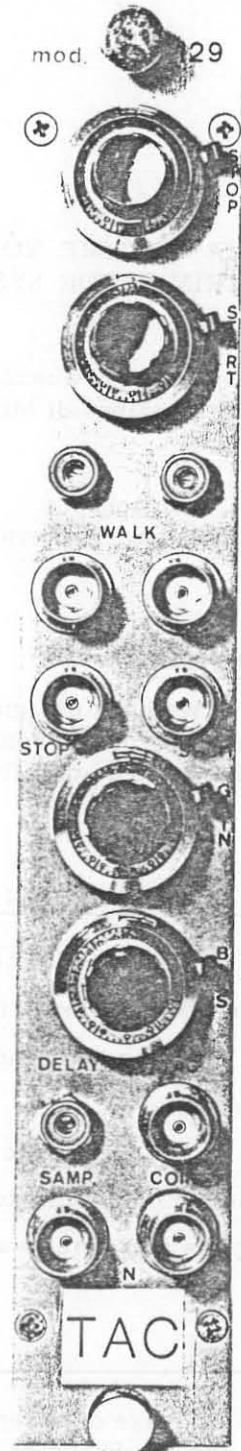


FIG. 1 - Photo of the front panel.

On the rear panel are also located:

- rotary switch for biased amplifier coarse gain adjustment;
- BNC connector for coincidence output signal;
- BNC connector for the direct TAC output signal.

The four position dip switch for different ranges is located on printed circuit board.

The present device, as previously indicated, consists of one TAC, two CFDs and a biased amplifier. The whole apparatus can be parted into four sections to describe it (Fig. 2):

- Constant fraction discriminator;
- Coincidence;
- Time to amplitude converter;
- Biased amplifier.

The detailed block diagram of the whole system is shown in Fig. 3.

2.1. - Constant fraction discriminator section

The two discriminators used allow an extremely accurate definition of the initial time of the two signals (start and stop).

In the constant fraction technique an input signal is delayed of a time T_0 , and a fraction of the undelayed pulse is subtracted from it. The output signal is generated only when the delayed signal will be greater than the fractionized one, which amplitude is about 25% of the delayed signal. T_0 is usually nearly equal to the pulse rise time (in our case about 4 ns).

The circuitry consists of two comparators: the first one is constant fraction type, the second one has a threshold variable from 0 to 1 V. An AND gate accomplishes the logical product between the two outputs of the comparators.

The two CFDs are built with ECL components, symmetrical in geometry and adjacent to avoid different thermal shifts between them.

The T_0 delay is obtained by means of a RG 178 cable, with an impedance $Z = 50 \Omega$, and an attenuation of only 0.9 db/m at 400 MHz. With these conditions the integration and attenuation of the signals is nearly completely avoided.

2.2. - Coincidence section

This section supervises the logic functions of the whole system. It also provides the coincidence output signal. This can be delayed by the coincidence input signal (2-6 μ s inside adjustable delay). Otherwise it is prompt. This output, with the two

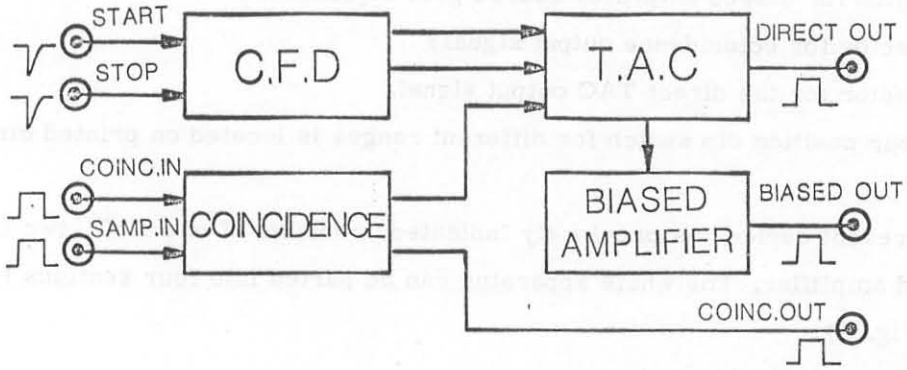


FIG. 2 - Simplified block diagram.

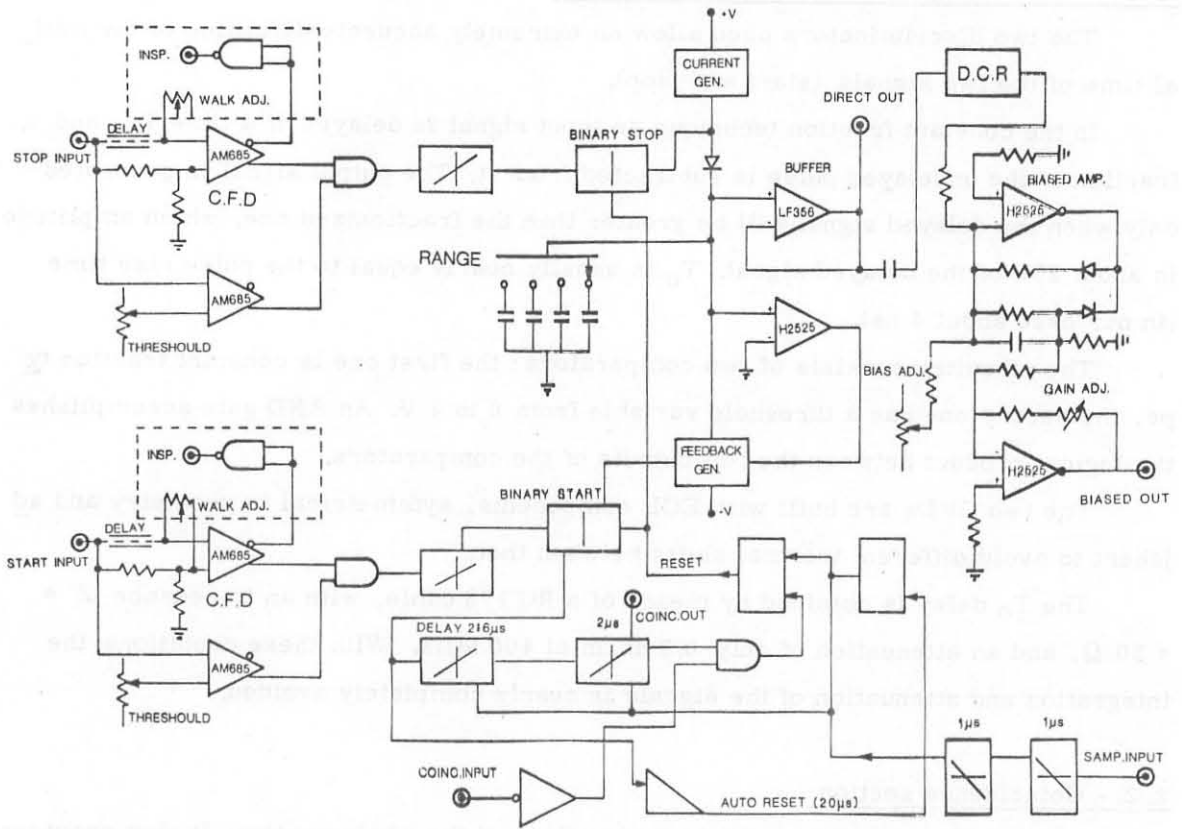


FIG. 3 - Detailed block diagram.

logical inputs, can be used in a multiparametric acquisition system for controlling different modules. In detail the two inputs can be used to control the TAC and CFD sections. In absence of these inputs, a general reset occurs and the analog output signal of the TAC will follow the capacitor charge.

2.3. - Time to amplitude conversion section

The start and stop signals reach the TAC section, coming from the two ECL memories used by the two CFDs to store the signals. A pair of start and stop signals can be processed in this section, unless the system is busy processing a previous information. The time interval between these two is converted into an analog pulse proportional to the measured interval, by means of the charge of the different capacitors corresponding to different ranges. The start input allows the constant current generator to charge the capacitor, while the stop one finishes the charging process.

Particular care has been taken of the constant current generator to assure an extreme precision and stability of the current value, and to minimize the effect due to the variations of the temperature and supply voltage.

High stability mica capacitors are also used to assure the best performances in temperature stability.

At rest, the feedback controlled discharge circuitry keeps the chosen capacitor at zero reference level. Its charge begins when is changed the logic state of the memory 2 and inhibited the T5 transistor (Fig. 4). In this way all the charging current flows into the capacitor.

The change of the logic state of memory 1 makes the T2 transistor conducting and absorbing the current of the generator.

The voltage developed across the tuning capacitor is applied to the operational amplifier LF356 with very high input impedance and the corresponding pulse presents itself to the direct output connector and to the biased amplifier section.

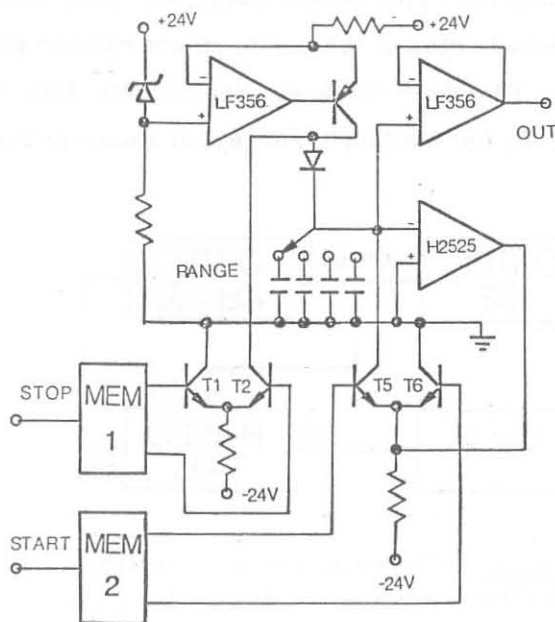


FIG. 4 - Particular of the TAC section.

2.4. - Biased amplifier section

This section accepts the signal from TAC section and provides expansion of the selected portion of the total time spectral range in order to reach maximum sensitivity in the analysis of a region of interest.

It consists of two operational amplifiers H2525 and biased voltage regulator (see Fig. 2). The bias level can be adjusted to any point from 0 to 2 V, corresponding to the whole TAC output range and its portion above the bias level can be expanded by a factor of 1 through 10. For example, if the TAC output range (0-2 V) corresponds to a time interval range (0-50 ns), the bias could be set at 1.0 V and the gain at 4. The output range of this section (0-4 V) would then correspond to a time spectral range of 25 to 50 ns, allowing a more accurate analysis of the selected region. In this case the sensitivity will be 6,25 ps/mV.

3. - EXPERIMENTAL RESULTS

We have tested the present apparatus by means of the Ortec 462 Time Calibrator and the Ortec DB463 Delay box (four delay sections each ranging from 0,5 up to 63,5 ns in step of 0,5 ns) to obtain random pulses.

For the three lower ranges (50, 150, 250 ns) we have used the chain shown in Fig. 5; for the fourth range that shown in Fig. 6.

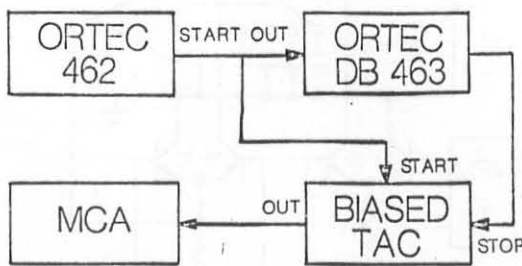


FIG. 5 - Electronic chain for testing the first three ranges (see text).

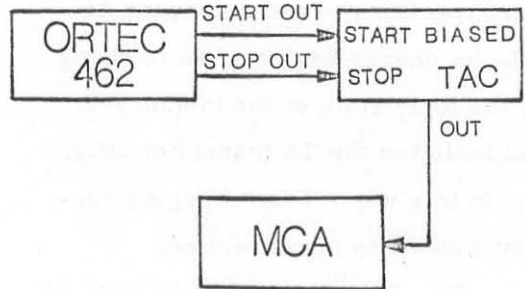


FIG. 6 - Electronic chain for testing the fourth range (see text).

In Table I are presented the results for the different full and partial ranges using the biased amplifier output.

With the above random generator we have tested the present module with a pulse rate ranging from a few cps up to about 25 kcps, with quite nice results for all ranges. For the 30-50 ns one we have obtained :

- maximum peak position shift : ± 3.75 ps (sensitivity 2.5 ps/mV), equal to $\pm 0.0075\%$
- FWHM resolution : without change
- Pile-up : no obvious presence.

TABLE I

RANGE (ns)	Linear regression coefficient	Sensitivity (ps/mV)	FWHM (ps) typical
0 - 50 ⁺	0.999970	11.35	✕
0 - 150 ⁺	0.999998	26.15	✕
0 - 250 ⁺	0.999998	66.13	✕
0 - 500 ⁺	0.999999	124.50	✕
30 - 50	0.999976	5.30	~ 13
100 - 150	0.999998	13.10	~ 26
170 - 250	0.999996	20.26	~ 40
324 - 500	0.999998	44.97	~ 67

(+) For proper minimum delay see text.

(✕) The resolution FWHM for the full scale ranges is less than or equal to the sensitivity.

We have also tested the apparatus with a standard repetitive pulser (BP4-BNC and Ortec 473A CFD to obtain a timing signal). In this case we have reached a frequency of 50 kHz, without obvious change of the performances and pile-up presence.

It is to note that the minimum measurable delay is 3 ns.

4. - SPECIFICATIONS

4.1. - Performance

- Time resolution : about 13 ps FWHM for the full 50 ns range;
< 0.03% of full range for all the other ranges.
- Temperature instability : < 20 ps/°C for the 50 ns range;
< 0.05%/°C for the other ranges.
- Integral nonlinearity : for all the ranges < 0.003% (see Table I).
- Maximum counting rate : 25 kcps for random pulses;
50 kHz for repetitive ones.
- Minimum measurable delay : 3 ns for all the ranges.
- Peak shift vs counting rate (random): $\pm 0.01\%$ for frequency range 0-25 kcps;
(repetitive): no obvious shift up to 50 kHz.

4. 2. - Controls

TAC range (ns)	: switch-selectable 4 f. s. (50, 150, 250, 500 ns).
Biased amplifier	gain: adjustable from 1 to 10; level: adjustable from 0 to 2 V.
CFD threshold	: adjustable from 0 to 1 V.
CFD walk	: adjustable to reach the best walk compensation.

4. 3. - Inputs

Start and Stop	amplitude: 300 mV minimum (negative); rise time: as short as possible (> 2 ns); pulse width: 4,5 ns.
Coincidence (logic)	: TTL logic level.
Sampling logic	: TTL logic level.

4. 4. - Outputs

TAC (direct)	amplitude: 0-2 V positive; rise time: 0.2 μ s; width: 2 μ s; impedance: 100 Ω .
TAC (biased)	amplitude: 0-8 V positive; rise time: 0.5 μ s; width: 2 μ s; impedance: 100 Ω .
Coincidence (logic)	: TTL logic level width 2 μ s.
Walk inspection	: amplitude 500 mV (negative) width 5 ns.

4. 5. - Electrical and Mechanical

Power required	: + 6 V 125 mA; - 6 V 245 mA; + 12 V 26 mA; - 12 V 30 mA; + 24 V 29 mA; - 24 V 40 mA.
Dimensions	: NIM-standard single-width module.

5. - CONCLUSIONS

There are the following main implications in the shown results :

- a) The resolution of the apparatus is very good: in fact it is practically the same of the commercial TACs, but in our system the resolution depends not only on the TAC, but also on CFDs and biased amplifier.
- b) The minimum measurable time interval (3 ns) is lower then that of other similar instruments.

- c) The compactness of the system (all the timing electronics in the same module) avoids the necessity to use cables of standard length to connect different modules and prevents the introduction of systematic errors and of additional noise in the timing measurements.
- d) The general performances of the apparatus are nice, specially regarding the different functions covered by it.

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